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A 3–8 GHz Low-Noise CMOS Amplifier

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Abstract—A wideband CMOS low-noise amplifier (LNA) is proposed by using the concept of mutual coupling technique implemented through a symmetric center-tap inductor. A frequency widening network is designed with a center-tap inductor at the input and the output of an LNA to achieve bandwidth extension with a single stage amplifier. The proposed wideband low noise amplifier is implemented in the 0.18 μm CMOS technology. This design obtains a bandwidth of 3–8 GHz with a power consumption of 3.77 mW from a 1.8 V supply.

Index Terms—Bandwidth extension, center-tap inductor, CMOS, filter, low-noise amplifier (LNA), passband.

I. INTRODUCTION

MANY low-noise amplifier (LNA) designs have been reported in the CMOS technology [1]–[3]. A wideband LNA should provide wideband impedance matching to the antenna, adequate gain, good linearity, gain flatness, and low power consumption over the band of interest. Among wideband designs, distributed and common-gate amplifiers suffer from high noise figure. Additionally, cascading several stages, which is widely used in the distributed LNAs, automatically degrades the linearity of the LNA. However, distributed amplifier benefits from high gain and maximum gain flatness compared to other techniques [1].

A typical input matching technique is implemented through the inductor-degeneration technique. This technique is feasible for narrowband LNA design. In this structure the degeneration inductor L_s is used to obtain the real part of input matching $\omega_T L_s$, where ω_T is the transistor cutoff frequency. However, this structure is impractical for wideband input matching. To achieve wideband input matching, a broadband filter is added at the input to resonate out the reactive components at the frequency of interest.

In this letter a wideband T-coil network is implemented at the input and the output of a single stage amplifier to realize the wideband amplifier. At the same time an active feedback scheme was applied in order to improve the circuit performance. Through this technique, wideband matching is achieved with a minimum number of components through a single stage amplifier. In addition this design obtains good gain and low noise figure performance.

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II. CIRCUIT DESIGN: THEORY AND PRACTICE

Fig. 1(a) shows the proposed wideband LNA circuit with the gate terminal biased with an off-chip bias-T source. A cascode stage is utilized to reduce reverse signal flow. In addition, transistors were carefully sized to decrease the gate parasitic resistance. The input impedance of Fig. 1(a) is simplified in the equivalent circuit shown in Fig. 1(b) and is calculated as

$$Z_{\text{IN}} = sL_X + \left[sL_Z + \left(\frac{R_F}{1 - A_v} \right) \right] \parallel \left(s(L_Y + L_s) + \frac{1}{sC_{\text{gs}}} + \omega_T L_s \right) \quad (1)$$

where $\omega_T = g_m/C_{\text{gs}}$, C_B & C_F are the blocking capacitors, and A_v is the open loop gain of the amplifier. It is clear that Z_{IN} is dependant on the feedback resistor R_F . By selecting a proper value of the R_F , input impedance matching is improved through the frequency range of interest. Basically a symmetric center-tap inductor is implemented as two coupled inductors to give a mutual inductance of M where $M = k\sqrt{L_3 L_4}$. The monolithic symmetric center-tap inductor is constructed using conductors overlaid as stacked metal. The mutual coupling plays an important role to exploit the concept of the wideband LNA. The input network, acts as a fifth-order band pass filter. This filter, Fig. 1(b), includes blocking capacitor C_B , L_X , $L_Z = -M = -k\sqrt{L_1 L_2}$, L_Y , C_{gs} , and L_s . A high order filter attenuates more out-of-band interferers and parasitic capacitors are resonated out by the filter. Note that this filter does not use any physical capacitor. The k -factor of the symmetric center-tap inductor add another degree of freedom to the input matching network. If the parasitic capacitance of the T-coil network is comparable to the C_{gs} , the performance of the input matching network will be degraded. So it is preferred to implement the inductors at the top-most metal level to reduce the substrate parasitic effect.

The Q -factor of the input T-coil network, is given as

$$Q_T = \frac{1/\omega_0 \cdot C_{\text{gs}}}{\left[R_s + \omega_T L_s + \frac{\omega_0^2 (L_X)^2}{R_P} \right]} \quad (2)$$

where ω_0 corresponds to the resonance frequency and

$$R_P = \left(\frac{R_F}{1 - A_v} \right) (1 + Q_{L_Z}^2) \quad (3)$$

A_v is the open loop gain of the amplifier and Q_{L_Z} is the quality factor of the L_Z . Through appropriate selection of the R_F value, parallel resistance R_P is affected and as a result Q_T of the network diminishes. Hence the bandwidth is increased.

To analyze the noise figure of the circuit, by solving the small signal noise model of Fig. 1(a) and applying the noise factor

Fig. 1. (a) Wideband LNA using symmetrical center-tap inductor (biasing circuitry not shown). (b) Input impedance equivalent circuit ($L_{Z'} \approx L_Z$).

Fig. 2. Die micrograph of the LNA.

scaling coefficient from [4], noise factor can be expressed as follows:

$$F \approx 1 + \frac{r_s}{R_s} + \left(\frac{\omega_0}{\omega_T} \right) \gamma \left(\frac{g_{d0}}{g_m} \right) \frac{1}{2Q_T} (1 - 2|c|\chi_d + (4Q_T^2 + 1)\chi_d^2) \quad (4)$$

Fig. 3. Simulated and measured S-parameters of the LNA.

Fig. 4. Tradeoff between NF of the LNA and Q-factor of the input inductor ($L_{3,4}$).

TABLE I
DESIGN VALUES OF THE LNA

$(W/L)_1$	$(W/L)_2$	$L_{1,2}^*$	$L_{3,4}^*$	L_L	L_s	R_F
120/0.18	40/0.18	6 nH	2.92 nH	1.31 nH	0.18 nH	1.14 k Ω

* $L_{1,2}$ and $L_{3,4}$ are the center-tap inductor.

where $\delta \approx 1.33-4$, $\gamma \approx 0.67-1.33$ are excess noise parameters, $c \approx j0.4$ [5], $\chi_d = (g_m/g_{d0})\sqrt{\delta/5\gamma}$, Q_T is the quality factor of the input matching circuit and g_{d0} is the channel conductance at $V_{DS} = 0$, respectively. Accordingly, R_F value should be increased to reduce the NF, however the tradeoff between NF and the input matching should be considered.

The circuit shown in the dotted-line loop at the output of Fig. 1(a) has three resonance frequencies. This triple resonance circuit helps to extend the bandwidth effectively. The capacitors C_1 and C_2 are the parasitic capacitances of the next stage and drain-bulk of the M_2 , respectively. The triple resonance is generated by three branches as; L_1-C_1 , L_1-C_1 & L_2-R_L , and the

TABLE II
WIDEBAND LNA PERFORMANCE SUMMARY AND COMPARISON

Reference	Technology	BW (GHz)	S ₁₁ (dB)	Gain _{max} (dB)	NF (dB)	IIP ₃ (dB)	Power (mW)	Area(mm ²)
This Work	0.18 μm CMOS	3–8	< –8	15.2	3.14_{min}–6.8_{max}	–6.63[†]	3.77	0.96
[3]	0.18 μ m CMOS	3.1–10.6	< –11	9.7	4.5–5.1	–6.2	20	0.59
[6]	0.18 μ m SiGe	3–10	< –10	21	2.5–4.2	< –1 [‡]	30	1.8
[7] STD	0.18 μ m CMOS	2.3–9.2	< –9.9	9.3	4.2–8	–	9	1.1

^{*} 3.14 dB is the minimum NF from 3.5–4 GHz and NF at 3 GHz is 4 dB. [†] at 5.3 GHz. [‡] at 5.4 GHz, 5.6 GHz.

overall circuit shown in the dotted-line loop. The mutual coupling should be considered as an extra term adding to L_1 and L_2 . Note that the conventional T-coil network has a bridging capacitor across L_1 and L_2 , where this capacitor is redundant here. It should be noted that R_L represents the built-in series resistance of the inductors and no physical resistor is used in the final circuit. This resistor is normally added to reduce the Q -factor of the output stage to improve the bandwidth, but at the cost of gain peaking. In addition an extra inductor L_L is implemented to improve gain-flatness at the output node V_{out} of the LNA.

III. EXPERIMENTAL RESULTS

The proposed wideband LNA with an off-chip bias-T was implemented in six-metal layers 0.18 μ m CMOS technology. A summary of the devices values are given in Table I. The die photograph is shown in Fig. 2. The total die area including the output buffer and pads is 1×0.96 mm². Table II indicates the performance comparison of the proposed LNA with the prior works [6], [7]. For this design, center-tap inductors with a coupling coefficient of $0.72 < k < 0.86$ is used. Fig. 3 shows the simulated and measured S-parameters which from measurement, –3 dB bandwidth is from 3–8 GHz and S_{11} is better than –8 dB for the entire range of frequencies. The maximum measured power gain is 15.2 dB between the frequency of 3.4–4 GHz and from the frequency of 4.2–8 GHz the gain flatness is better than 1.5 dB. The LNA core consumes only 3.77 mW power from a 1.8 V supply voltage, making it suitable for low-power applications. The simulated and measured noise figure of the LNA is shown in Fig. 4. This figure shows the Q -factor of the center-tap inductor used at the input matching network. The measurement results demonstrate that the noise figure is increasing with the frequency, which is mainly due to the Q -factor reduction of the tuning inductors. A remedy is to push the cutoff frequency (–3 dB) of the input matching network beyond 8 GHz by increasing the k -factor of the inductors to reduce the network attenuation. This helps to enhance the bandwidth without an increase in current, too. In addition, (4) suggests to use a transistor with higher unity gain frequency ω_T to lower the noise figure. The minimum noise figure is from 3–5 GHz between

3.14–5 dB with an average of 4 dB. The entire LNA was designed in single stage with minimum number of passive components. A good linearity with minimum bias current is achieved. The third-order input intercept point (IIP₃) was simulated with two tones, spaced at 1 MHz between them. The IIP₃ of the LNA was simulated at different frequencies, showing that the entire linearity is degraded by 3 dB due to the output buffer nonlinearity. The IIP₃ of the stand-alone wideband LNA is –6.63 dB at 5.3 GHz frequency.

IV. CONCLUSION

A wideband LNA that uses center-tapped inductor with a resistive feedback technique was implemented in 0.18 μ m CMOS technology for wideband and low power application. In the proposed wideband LNA minimum number of inductors were employed to save area. Using the proposed design methodology a wideband, high gain and low power LNA is obtained.

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REFERENCES

- [1] A. Yazdi, D. Lin, and P. Heydari, “A 1.8 V three-stage 25 GHz 3 dB-BW differential non-uniform downsized distributed amplifier,” in *IEEE ISSCC Tech. Dig.*, 2005, pp. 156–158.
- [2] S. Mohan, M. Hershenson, S. Boyd, and T. Lee, “Bandwidth extension in CMOS with optimized on-chip inductors,” *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.
- [3] C.-F. Liao and S.-I. Liu, “A broadband noise-canceling cmos lna for 3.1–10.6 ghz uwb receivers,” *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.
- [4] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge University Press, 1998.
- [5] A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, A. Z. Duijnhoven, and V. Venezia, “Noise modeling for RF CMOS circuit simulation,” *IEEE Trans. Electron. Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.
- [6] A. Ismail and A. Abidi, “A 3–10 GHz low-noise amplifier with wideband LC-ladder matching network,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.
- [7] A. Bevilacqua and A. Niknejad, “An ultrawideband CMOS low-noise amplifier for 3.1–10.6 GHz wireless receivers,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.