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Antenna-in-Package and Transmit–Receive Switch for Single-Chip Radio Transceivers of Differential Architecture

Yue Ping Zhang, Jun Jun Wang, Qiang Li, *Member, IEEE*, and Xue Jun Li

Abstract—A fully differential architecture from the antenna to the integrated circuit is proposed for radio transceivers in this paper. The physical implementation of the architecture into truly single-chip radio transceivers is described for the first time. Two key building blocks, the differential antenna and the differential transmit–receive (T–R) switch, were designed, fabricated, and tested. The differential antenna implemented in a package in low-temperature cofired-ceramic technology achieved impedance bandwidth of 2%, radiation efficiency of 84%, and gain of 3.2 dBi at 5.425 GHz in a size of $15 \times 15 \times 1.6 \text{ mm}^3$. The differential T–R switch in a standard complementary metal–oxide–semiconductor technology achieved 1.8-dB insertion loss, 15-dB isolation, and 15-dBm 1-dB power compression point ($P_{1\text{dB}}$) without using additional techniques to enhance the linearity at 5.425 GHz in a die area of $60 \times 40 \text{ }\mu\text{m}^2$.

Index Terms—Complementary metal–oxide–semiconductor (CMOS), low-temperature cofired ceramic (LTCC), microstrip patch antenna, single-chip radio, transmit–receive (T–R) switch.

I. INTRODUCTION

RECENTLY, highly integrated radio transceivers in complementary metal–oxide–semiconductor (CMOS) technology for wireless local area network (WLAN) applications at 5-GHz bands have been successfully demonstrated [1], [2]. The high level of integration has the benefit of cost reduction and system reliability and therefore represents the trend for implementing radio systems. Fig. 1 shows a simplified architecture from the current designs of integrated transceivers in CMOS technology [1], [2]. Note that the direct-conversion architecture is adopted to circumvent the difficulty of the integration of different high- Q analog bandpass filters in CMOS technology. Also, the differential signal paths are only employed in the integrated circuit (IC) to reduce local oscillator feedthrough and leakage and to achieve higher linearity, lower offset, and better immunity to common-mode noise due to power supply variations or substrate coupling. Furthermore, off-chip components such as one antenna, one transmit–receive (T–R) switch, and

Fig. 1. Simplified radio architecture.

Fig. 2. Improved radio architecture.

two baluns are required to construct a functional radio transceiver on a printed circuit board (PCB).

Fig. 2 shows an improved architecture with higher degree of integration of radio transceivers in CMOS technology. Note that a fully differential architecture from the antenna to the IC is proposed. The T–R switch that connects the antenna to the receiver and transmitter is integrated. Also, bulky and lossy baluns, as shown in Fig. 1, are not required anymore, which will not only translate into the reduction of bill of materials but also, more importantly, the improvement of the receiver noise performance

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Fig. 3. CBGA package: (a) Top view and (b) bottom view with encapsulant removed.

and transmitter power efficiency. Furthermore, the functional radio transceiver is suggested to realize in the IC package.

Fig. 3 shows the IC package in a cavity-down ceramic ball grid array (CBGA) format. It consists of three layers, with an open cavity formed in the middle. The top layer with the patch and guard ring printed on its surface is 0.8 mm thick, the middle layer is 0.4 mm thick, and the bottom layer where solder balls are attached is also 0.4 mm thick. There are two buried layers and one top-layer metallization in the construction. The lower buried layer provides the metallization for the signal traces, while the upper buried layer provides the metallization for the ground plane. The microstrip patch radiator of the differential antenna and the guard ring are realized with top-layer metallization.

Fig. 3 also shows a highly integrated radio transceiver die attached upside down to the meshed ground plane in the cavity. The chip die is connected to the external solder balls through the bond wires, the signal traces, and the vias. The differential T-R switch in the transceiver die is linked to the differential antenna through two identical packaging element networks. A packaging element network includes three bond wires, three signal traces, and three vias in the ground-signal-ground (GSG) fashion. The die is automatically shielded from the antenna by the ground plane and will be encapsulated in real implementation. The standard two-pack aliphatic epoxide glop-top material is suggested for encapsulation in a two-step process. First, the encapsulant of high viscosity is placed around the die edges. Then, the same encapsulant of low viscosity is placed to cover the whole die and the cavity. The encapsulants are done wet in wet, followed by a common curing operation. It should be mentioned that the glop-top material slightly degrades the interconnect performance from the die to the package. The shared ground plane has simplified the shielding design and realization

of the separate ground planes employed in [3] and [4]. The guard ring can further reduce the electromagnetic interference of the antenna on the carried radio transceiver.

The package offers the possibility to combine the antenna and a radio transceiver die into a truly surface-mounted single-chip device. Thus, the assembly cost and PCB area of a discrete antenna (e.g., a chip antenna) can be saved. In the following, we focus on the development of two key building blocks for the architecture. One is the differential antenna, and the other is the differential T-R switch. We design the differential antenna in low-temperature cofired ceramic (LTCC) in Section II and the differential T-R switch in CMOS in Section III. We do not attempt to design other circuits because they have already been designed for differential signal operation elsewhere. Finally, we summarize the conclusions in Section IV.

II. DIFFERENTIAL ANTENNA DESIGN

The differential antenna is implemented in a CBGA package to carry the highly integrated radio transceiver die. The design of the differential antenna must consider the package fabrication in large quantity, which requires novel manufacturing technologies. LTCC technology that uses noble metals and specific ceramic materials and has the flexibility in realizing an arbitrary number of metallic and ceramic layers is suitable for the mass production of the design [5]–[7]. The LTCC material system from DuPont is used in this demonstration [8]. The 951-AX ceramic type has a dielectric constant of 7.8 and a loss tangent of 0.002 at 5 GHz. The differential antenna is designed with the HFSS from Ansoft [9]. At 5-GHz bands, WLAN systems operate from 5.15 to 5.35 GHz or from 5.725 to 5.825 GHz. In this design, we target the frequency in between at 5.4 GHz. The differential antenna has the input impedance defined as

$$Z_d = \frac{V_d}{I} = 2(Z_{11} - Z_{21}) = 2(Z_{22} - Z_{12}) \quad (1)$$

where Z_{11} is the self-impedance of feed 1 and Z_{12} is the mutual impedance between feeds 1 and 2 [10]. The impedance value is required in the design of matching network between the antenna and the differential active circuitry in a radio system. A circuit model and impedance calculation of a microstrip patch antenna on a ceramic package for antenna-chip codesign of highly integrated RF transceivers can be found in [11]. The return loss calculated from Z_d is given by

$$RL = -20 \log_{10} \left(\left| \frac{Z_d - Z_c}{Z_d + Z_c} \right| \right) \quad (2)$$

where Z_c is 100 Ω . Fig. 4 shows the photograph of the fabricated differential antenna in the CBGA package format. It measures $15 \times 15 \times 16 \text{ mm}^3$. The microstrip patch radiator of size $9.5 \times 9.8 \text{ mm}^2$ is above the ground plane by 0.8 mm. The diameter of the antenna feeding vias is 0.2 mm. The size of the microstrip patch was first estimated with the CAD formula and then adjusted from the HFSS simulation. It was found that the grounded guard ring slightly shifts up the resonant frequency of the differential microstrip patch antenna, and more importantly, the feeding signal traces can be used for matching and bandwidth enhancement.

Fig. 4. Photograph of the fabricated differential antenna in the CBGA package.

Fig. 5. Differential antenna mounted on the PCB for testing.

Fig. 6. Return losses of the differential antenna.

The antenna was mounted on a PCB shown in Fig. 5 for testing. The size of the PCB was $60 \times 40 \times 0.8 \text{ mm}^3$ and fabricated with FR4. It was tested with a balun and an HP 8510C network analyzer in an anechoic chamber. For our simulation, an air box was used for the radiation boundary. The PCB and CPW lines are part of the HFSS simulation model, and the bond wires and the balun are not. Two wave ports of each with a $50\text{-}\Omega$ source were applied at the two edges of the two CPW line feeds on the PCB. The two sources had the same amplitude and an offset phase of 180° .

Fig. 6 compares the simulated and measured return losses of the differential antenna. It is seen that the simulated and measured return losses are in acceptable agreement. The measured resonant frequency shifts up from the designed 5.4–5.425-GHz range because the LTCC shrinkage was not accurately controlled in fabrication. The difference in the return loss values is caused by the balun. The amplitude and phase imbalance of the balun cannot be calibrated. The return loss above 10 dB at

Fig. 7. Radiation patterns of differential antenna. (a) E-plane. (b) H-plane.

the frequency of operation indicates that acceptable matching between the antenna and the $100\text{-}\Omega$ signal source is achieved. The measured impedance bandwidth of the differential antenna is 110 MHz ($0.11/5.425 = 2\%$). The 2% relative bandwidth is enough for the WLAN system operating at 5.775 GHz. However, it is not enough for the WLAN system operating at 5.25 GHz. The bandwidth of the differential microstrip patch antenna should be enhanced for more applications.

Fig. 7 compares the simulated and measured copolar radiation patterns of the differential antenna at 5.425 GHz. It can be observed that the simulated radiation patterns agree reasonably with the measured radiation patterns. There are some discrepancies, which, we believe, are caused by the existence of the balun and its amplitude and phase imbalance in the measurements. The radiation is stronger in the upper hemisphere, i.e., in the direction

Fig. 8. Differential T-R switch.

normal to the microstrip patch. It was found that the cross-polar radiation was at least 20 dB lower than the copolar radiation in the upper hemisphere. The lower cross-polar radiation is the result of the differential signal operation. The antenna efficiency was calculated to be 84%. The antenna peak gain was calculated to be 3.2 dBi, which matches well to our simulated values.

III. DIFFERENTIAL T-R SWITCH DESIGN

The schematic of the differential T-R switch [12] is shown in Fig. 8. Transistors M1, M2, M3, and M4 perform the main switching function. A high control voltage V_{ctrl} turns M1 and M3 on, which enables the differential path between the antenna and the receiver. Similarly, the differential transmit path is turned on when the control voltage is low. The control voltage is biased through a resistance R_G to reduce the effect due to capacitive coupling around the gate of the off-transistors. The differential nature results in an improved power-handling capability compared with single-ended configurations. From the power point of view, the differential output scheme is able to handle twice over the single-ended output power, i.e., 3-dB higher P_1 dB could be achieved in the differential switch. As the power-handling capability is the bottleneck of CMOS T-R switches, differential architecture is of great advantage in current silicon technology.

We design transistors M1, M2, M3, and M4 to have the same size. As a result, the differential T-R switch has the same equivalent circuit for both TX and RX modes. Using the half-circuit concept, the small-signal equivalent circuit for the differential T-R switch in the TX mode is shown in Fig. 9. R_{ON} is the on-resistance of the transistor which is operating in the linear region, R_B is the substrate resistance, R_C is the coupling resistance through the substrate between the two transistors of the differential T-R switch in the same signal path, R_{OFF} is the off-resistance of the transistor, C_{OFF} is the off-capacitance of the transistor, and C_{SB} and C_{DB} are the parasitic capacitances of the transistor. In the ideal case, the body currents of the differential transistors can compensate each other. This is similar with a typical differential pair, where the tail current source does not contribute to the small-signal paths. On the other hand, the substrate resistance R_B creates extra loss and degrades the complementary operation, which will eventually degrade the performance of the switch. For a differential architecture, R_C can be

Fig. 9. Small-signal equivalent circuit for the differential T-R switch.

designed as a very low resistance as compared to the substrate resistance R_B , and R_B can be designed slightly higher by reducing the number and density of substrate contacts. Therefore, the effect of substrate loss can be minimized, which improves the performance.

The insertion loss from the transmitter to the antenna can be calculated as the ratio of the power available at the transmitter P_T to the power delivered to the antenna P_A

$$IL = \frac{P_T}{P_A} = \frac{A^2 + B^2}{(2Z_0)^2 (E^2 + F^2)} \quad (3)$$

where

$$A = R_{OFF} R_{ON} Z_0 \omega^2 (3R_T + 2Z_0) \cdot [C_{OFF} (C_{DB} + C_{SB}) + 2C_{DB} + C_{SB}] - 3Z_0 (R_{OFF} + R_{ON}) - 2R_{OFF} R_{ON} \quad (4)$$

$$B = \omega Z_0 (C_{DB} + C_{SB}) (3R_T + 2Z_0) (R_{OFF} + R_{ON}) + 2\omega R_{OFF} R_{ON} [R_T (C_{DB} + C_{SB}) + Z_0 (C_{DB} + 2C_{SB})] + 3\omega R_{OFF} R_{ON} C_{OFF} Z_0 \quad (5)$$

$$E = R_{OFF} C_{OFF} R_T \omega^2 (C_{DB} + C_{SB}) + 2R_{OFF} R_{ON} R_T C_{DB} C_{SB} \omega^2 - (R_{OFF} + R_{ON}) \quad (6)$$

$$F = \omega R_T (C_{DB} + C_{SB}) (R_{OFF} + R_{ON}) + \omega C_{OFF} R_{OFF} R_{ON}. \quad (7)$$

In the aforementioned expressions, Z_0 is the characteristic impedance that the source and load are terminated with, ω is the operating radian frequency, and $R_T = R_B / (R_C / 2)$. The parasitic capacitances C_{SB} , C_{DB} , and C_{OFF} make the insertion loss frequency dependent. The insertion loss (3) increases with frequency and can be minimized by optimizing the values of R_T and R_{ON} .

Previous research shows that low substrate resistance is preferred in the high-frequency switch design and can be achieved by increasing the density of substrate contacts [13]. In the linear/triode region, R_{ON} can be expressed as

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})}. \quad (8)$$

Thus, R_{ON} can be minimized by increasing the W/L ratio of the switch transistors, where tradeoff occurs since a large transistor

leads to large parasitics, resulting in large C_{DB} and C_{SB} , and thus, the frequency-dependent term in (3) will be increased. An optimal W/L ratio exists to minimize the insertion loss.

The isolation from the transmitter to the receiver can be calculated as the ratio of the power available at the transmitter P_T to the power leaked to the receiver P_R

$$IS = \frac{1}{|S_{21}|^2} = \frac{M^2 + N^2}{(2\omega Z_0)^2(P^2 + Q^2)} \quad (9)$$

where

$$M = R_T Z_0 \omega^3 (3R_T + 2Z_0) \times [C_{OFF}(C_{DB}^2 + C_{SB}^2) + C_{DB}C_{SB}(C_{DB} + C_{SB} + 2C_{OFF})] - 2\omega [2R_T(C_{DB} + C_{SB}) + C_{DB}Z_0] \quad (10)$$

$$N = 2 + \omega^2 Z_0 [R_T C_{DB}^2 - Z_0 C_{SB}^2 - 2C_{OFF}(C_{DB} + C_{SB})(3R_T + Z_0)] - \omega^2 R_T (C_{DB}^2 + C_{SB}^2)(2R_T + 3Z_0) - 3\omega Z_0 (C_{OFF} + C_{SB}) - 2C_{DB}C_{SB}\omega^2 (Z_0^2 + 4R_T Z_0 + 2R_T^2) \quad (11)$$

$$P = R_T^2 \omega^2 (C_{DB} + C_{SB}) \cdot [C_{OFF}(C_{DB} + C_{SB}) + C_{DB}C_{SB}] - C_{OFF} \quad (12)$$

$$Q = R_T \omega [2C_{OFF}(C_{DB} + C_{SB}) + C_{DB}C_{SB}]. \quad (13)$$

It is found that the isolation is mainly determined by the parasitic capacitance C_{OFF} between the drain and the source, and increasing the gate width leads to the degradation of isolation performance. Our calculation shows that the trend is monotonous, and transistor size can be optimized to provide the minimum insertion loss while maintaining a reasonable isolation.

The linearity, or power-handling capability, is directly related to the bias condition of the MOS transistors. A large signal at the drain/source may cause the junction diodes to be forward biased and to clip the signal. The unintentional turn on of the off-transistors can also distort the signal. As a result, the dc bias of the T-R nodes affects the linearity significantly [14], [15]. High dc bias and high control voltages are often used in the CMOS T-R switch for better linearity. However, reliability problems may exist potentially with a large gate-source voltage. In this design, the differential architecture is employed that improves the linearity fundamentally, rather than over stresses the CMOS transistors, and the P_{1dB} can be calculated in dBm by

$$P_{1dB} = 10 \log \left(\frac{4V_{th}^2}{50} \right) + 30. \quad (14)$$

The control voltage is provided by the built-in inverter with 1.8-V standard supply voltage. Note that, in (8), R_{ON} can also be reduced by simply increasing the term $(V_{GS} - V_{th})$ with the transistor size unchanged, which improves the insertion loss intuitively. In fact, the performance of the T-R switch depends significantly on the working condition. Assuming that the T-R nodes are biased at 0.8 V, and the control voltage is 1.8/0 V, numerical calculation shows that a 105- $\mu\text{m}/0.18\text{-}\mu\text{m}$ transistor should be chosen to achieve the lowest insertion loss. In this design, however, 100 $\mu\text{m}/0.18\text{ }\mu\text{m}$ is used due to the scale limit of RF CMOS transistors provided by the foundry. R_{G1} – R_{G4}

Fig. 10. Die photograph of the fabricated differential T-R switch.

should be chosen large enough to create a floating-gate terminal at RF. Considering that large bias resistance will lower the switch speed, 3.9-k Ω bias resistance is chosen.

Practical problems in the single-ended T-R switch include substrate resistance, source/drain parasitics, dc biasing, and transistor sizing [13]–[16]. In the differential T-R switch design, issues on cross-coupling and transistor matching between the two signal paths should also be considered carefully. Tradeoff exists among these issues, e.g., good matching of transistors requires a close placement, whereas crosstalk increases when transistors are placed near to others. Choose the layout strategy depends on the application and system requirement. In general, crosstalk and coupling increase the nonlinearity in the circuits, resulting in degradation on the insertion loss performance and power-handling capability. On the other hand, mismatch is a signal-independent process, which does not produce other signal-dependent problems as cross-coupling does, e.g., cross-coupling may affect dc biasing conditions. Therefore, considerations are focused on reducing the effect of cross-coupling at the price of matching degradation. The matching transistors in the same signal path (e.g., M1 and M3, and M2 and M4) are placed together to improve the matching. The transistors in the different on/off status are placed far away to avoid cross-coupling.

The differential T-R switch was fabricated in a 1.8-V one-poly six-metal 0.18- μm standard CMOS technology. The active area of the switch is 60 $\mu\text{m} \times 40\text{ }\mu\text{m}$. Fig. 10 is the die photograph of the fabricated switch. Four GSSG pads were designed for on-chip measurement purposes. All measurements at I/O pads were carried out using Cascade Microtech's 100- μm differential GSSG probes. A four-port network analyzer was used in the experiment, which avoids the complicated on-chip balun design for testability. The control voltage is 1.8/0 V, and the T-R nodes are biased at 0.8 V. Note that the differential impedance at each port is 100 Ω .

Fig. 11. Measured insertion loss and isolation parameters for the differential-mode small signals.

Consider only the small differential signal applied to each port. The measured and calculated insertion losses and isolation from (3)–(13) are shown in Fig. 11. The measured insertion loss is from 1.6 dB to 2.0 dB over the range of 5–6 GHz. The results indicate that the on-resistance R_{ON} of the switch transistor is extremely small with large W/L ratio, whereas C_{DB} and C_{SB} are increased, and the frequency-dependent component in (3) has obvious effect on the insertion loss when the operating frequency is increased. The isolation is above 15 dB from 5 to 6 GHz. Although, in the differential case, cross-coupling and mismatch further degrade the insertion loss and isolation, these results are comparable with other single-ended CMOS T-R switches [14].

The linearity of the switch determines the maximum power that it can handle. Power 1-dB compression point (P_{1dB}) is used to measure the linearity. Since the switch is fully symmetric, the linearity in the transmitted mode and receive mode is identical. Fig. 12 compares the calculated and measured large-signal results. A 15-dBm input P_{1dB} is obtained. As mentioned earlier, the differential switch should have 3-dB higher P_{1dB} than the single-ended switch in theory. This is proved by other single-ended CMOS T-R switches where maximum 11–12-dBm power-handling capability is reported without tuning the substrate bias [15].

As can be seen from Figs. 11 and 12, both the simulated and measured characteristics are in acceptable agreement, proving that (3)–(14) are useful for predicting the performance of the differential T-R switch.

Finally, it should be mentioned that, for the implementation of this highly integrated differential transceiver front end, one has to consider issues such as bonding wires, pads, and ESD protection circuitry. These issues are actually the same as for the conventional RFIC transceivers [17]–[20]. The bond wires can be used not only for interconnection but also for compensation of parasitic capacitance from the pads. It is known that a typical gold bond wire with a diameter of 25 μm exhibits inductance of about 1 nH/mm. ESD is a major reliability concern. As the T-R switch becomes the first block of the transceiver chip, the challenge of ESD protection is shifted from the low-noise amplifier to the T-R switch. A simple ESD protection circuit using a shunt inductor has been proved quite effective for the

Fig. 12. Linearity of the differential T-R switch at different frequencies. The T-R nodes are biased at 0.8-V with 1.8/0-V control voltage.

single-ended T-R switch [20] and should be the same operative for our differential T-R switch.

IV. CONCLUSION

We have proposed a fully differential architecture from the antenna to the IC for radio transceivers in this paper. We have described the physical implementation of the architecture into truly single-chip radio transceivers for the first time. Two key building blocks, the differential antenna and the differential T-R switch, were designed, fabricated, and tested. The differential antenna in LTCC technology achieved impedance bandwidth of 2%, radiation efficiency of 84%, and gain of 3.2 dBi at 5.425 GHz in a size of $15 \times 15 \times 1.6 \text{ mm}^3$. The differential T-R switch in CMOS technology achieved 1.8-dB insertion loss, 15-dB isolation, and 15-dBm P_{1dB} without using additional techniques to enhance the linearity at 5.425 GHz in a die area of $60 \times 40 \mu\text{m}^2$. The challenges to further integration include the implementation of ESD, packaging, assembly, etc. Nevertheless, the validation of these key functional blocks will eventually enable the implementation of truly-differential transceivers.

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