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Theng, A. L.; Goh, Wang Ling; Ng, C. M.; Chan, L.; Lo, Guo-Qiang

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Dual Nanowire Silicon MOSFET With Silicon Bridge and TaN Gate

A. L. Theng, W. L. Goh, *Member, IEEE*, G. Q. Lo, *Senior Member, IEEE*, L. Chan, and C. M. Ng

Abstract—This paper demonstrates a high performance silicon nanowire mosfet built on silicon-on-insulator (SOI) platform. Stress-limiting oxidation technique was exploited for dual nanowire channel formation. To further improve the performance of the device, TaN metal gate is used instead of the conventional polysilicon gate. The thin silicon bridge between the two nanowires provides a small boost in the drive current, without degrading the short channel performance. The novel structures are able to achieve excellent electrical performances, high drive current of $927 \mu\text{A}/\mu\text{m}$ for p-channel and $554 \mu\text{A}/\mu\text{m}$ for n-channel, near ideal subthreshold slope (SS), and low drain-induced barrier lowering (DIBL).

Index Terms—Silicon nanowire transistor, silicon-on-insulator (SOI) technology.

I. INTRODUCTION

TRANSISTOR scaling has led to the exploration of various nonclassical devices for the delivery of high performance devices. Double-gate FinFET [1], tri-gate [2], gate-all-around (GAA) [3], and the nanowire FinFETs [4]–[6] are some well-known structures reported. These devices are innate with good suppression of short-channel-effects (SCEs), high drive current and excellent $I_{\text{on}}/I_{\text{off}}$ ratio. Silicon nanowire transistors have been attracting the attention of researchers mainly for their improvement in the transport property [7] and their compatibility with CMOS process [5], [6]. The published results on polysilicon gate nanowire transistors [5], [6] have been well covered. Nevertheless, the performance of nanowire transistors can be further enhanced using high- k dielectric and metal gate [4].

In this paper, we present the dual nanowire field effect transistor (DNWFET) devices that are fabricated using HfO_2 and TaN as the gate dielectric and gate material, respectively. TaN metal gate is engaged to improve the work function of the nanowire transistors. Not only a suitable threshold voltage (V_T) can be

attained, but also the leakage current is reduced. The top and bottom nanowires are bridged by a thin silicon layer to enhance the drive current without much degradation in the short channel performance. The nanowire channel is wrapped around by a TaN gate to provide optimum electrostatic control.

II. FABRICATION OF NANOWIRE MOSFET

The SOI wafers with 70 nm p -type ($\sim 10^{15}/\text{cm}^3$) top silicon and 150 nm buried oxide (BOX) are used as starting materials. Lithography and resist trimming are performed to achieve a fin width of around 50 nm. The wafers are etched and sent for dry oxidation at 875°C for 5 h. With well-controlled self-limiting oxidation process, dual nanowire channels that are connected by a thin silicon bridge can be established. The oxidation process makes use of the different oxidation rates of the various silicon planes to form the two nanowires. The sides of the fins that are at 1 1 0 plane oxidize two times faster than the top of the fin (at 1 0 0 plane). With the close proximity of the two nanowires, and the precisely controlled oxidation parameters and timings, a thin silicon bridge can be formed. The oxidized structure is later released with a dilute hydrofluoric acid (DHF) dip. The hydrofluoric acid (HF) dip also undercuts the BOX layer to facilitate the development of the wrap around gate.

Fig. 1(a) shows the dual nanowire upon oxide removal. A high quality gate oxide of 20 Å is then grown, followed by a 30 Å HfO_2 deposition to complete the gate dielectric stack. The 800 Å of TaN that wraps around the nanowire channel is then deposited using physical vapor deposition (PVD), for improving the electrostatic control of the device [see Fig. 1(b)]. The TaN gate electrode is patterned with a triple-layered hardmask (oxide–nitride–oxide) process. Two hardmask etching steps with additional wet processes in between are required to provide a clean TaN etch [see Fig. 1(c)]. BF_3 and As of dose $4 \times 10^{15} \text{ cm}^{-2}$ with 10 and 20 keV energy for the p - and n -DNWFETs are engaged for the implantation step. To form the source and drain, the device is given a short 10 s source/drain (S/D) activation anneal prior to contact formation and metallization for the device. The process finally ended with a sintering at 430°C . Fig. 1(d) is the TEM cross section of a 5-nm diameter dual nanowire channel with a 1 nm silicon bridge, surrounded by gate dielectric and TaN gate. An overview of the processing steps is listed in Fig. 1(e). Fig. 2 provides the schematic views of the DNWFET structure.

III. RESULTS AND DISCUSSIONS

The I_d vs V_d and I_d vs V_g characteristics of the 350-nm long nanowire MOSFET devices are given in Fig. 3. At an operating

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A. L. Theng and W. L. Goh are with the Department of Electrical and Electronics, Nanyang Technological University, Singapore 639798, Singapore (e-mail: then0003@ntu.edu.sg; ewlgoh@ntu.edu.sg).

G. Q. Lo is with the Institute of Microelectronics, Singapore 117685, Singapore (e-mail: logq@ime.a-star.edu.sg).

L. Chan and C. M. Ng are with the Chartered Semiconductor Manufacturing Limited, Singapore 738406, Singapore (e-mail: chanlap@charteredsemi.com; ngcm@charteredsemi.com).

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Fig. 1. SEM pictures of the device after various processing steps. (a) Nanowires released after DHF dip. (b) TaN deposition causing deformation of nanowire channel. (c) TaN gate etch. (d) TEM image of dual 5-nm diameter nanowire with 1 nm silicon bridge wrapped around by TaN gate. (e) Summary of processing steps for DNWFET.

voltage of 1.5 V, the *p*-DNWFET exhibits a drive current of 927 $\mu\text{A}/\mu\text{m}$, while the *n*-DNWFET achieving 554 $\mu\text{A}/\mu\text{m}$. The *p*- and *n*-DNWFET exhibits comparable leakage currents of 0.9 and 1.8 nA/ μm , respectively, both taken at zero gate voltage. All currents are normalized with the nanowire diameters and silicon

Fig. 2. Several views of the dual nanowire device. (a) 3-D view. (b) Cross-sectional view across channel at *x*-*z* plane. (c) Cross-sectional view on *y*-*z* plane. (d) 3-D view of the channel region.

bridge width. This gives a spread of $I_{\text{ON}}/I_{\text{OFF}}$ ratio between 10^5 and 10^6 . The high drive current is attributed to the volume inversions of the two silicon nanowires. Strain generated from the thermal oxidation process [8] and stress from the TaN deposition process provide mobility enhancement in the devices. The thin 1 nm silicon bridge is believed to contribute only a small current boost. The higher ON current observed in *p*-DNWFET as compared to that in *n*-DNWFET is mainly attributed to the difference in V_T , the higher total on resistance of *n*-DNWFET as compared to that of *p*-DNWFET, and also variation in the effective carrier mass between the two. These observations are also reported in [9]. Note that for DNWFET devices, this difference in ON current is made more severe by the large difference in the two V_T . Measurements show the *p*-DNWFET achieved a V_T of -0.29 V, while the *n*-DNWFET has a high V_T of

(a)

(b)

Fig. 3. (a) I_d vs V_g plots. (b) I_d vs V_d plot of 350 nm dual nanowire MOSFET devices. Note that the currents have each been normalized to the diameters of the nanowires.

0.56 V. Fixing an operating voltage of 1.5 V would indicate a lower overdrive ($V_g - V_T$) for n -DNWFET, and hence, yielding a lower drive current.

We should also note that after the gate etch, the expose portions of the nanowire [see Fig. 2(a) and (b)] is subjected to high dose S/D implantation. This may lead to amorphization of the exposed portions of the nanowire.

Without a template for subsequent recrystallization via solid phase epitaxy, the expose portions of the nanowire is unlikely to recrystallize after the S/D activation anneal. Thanks to the used of boron splices in p -DNWFET, which have a higher threshold for amorphization, the expose nanowire portions of the p -DNWFET are able to remain crystalline. This results in a higher relative total resistance in n -DNWFET than p -DNWFET. The lower effective mass of hole as compared to electron of the [1 1 0] direction [9] shows that hole mobility is enhanced.

The wrap-around gate electrode provides a shield to block the drain field, yielding good immunity to the short channel

Fig. 4. G_m plot of 500 nm nanowire devices, with TaN gate device having higher transconductance in comparison to polysilicon device.

(a)

(b)

Fig. 5. I_d vs V_g graph of polysilicon and TaN gate devices. (a) For NMOS. (b) For PMOS. The implementation of TaN gate shift the plot to the right for NMOS and to the left for PMOS, therefore reducing the OFF-state leakage current, measure at $V_g = 0$.

Fig. 6. Substrate bias (V_{BS}) sweep illustrating the immunity of substrate bias effect on both nanowire and reference devices fabricated on the same wafer.

effects (SCEs). The immunity is reflected in the 65 mV/dec subthreshold slope (SS) and 25 mV/V drain-induced barrier lowering (DIBL) achieved by the PMOS. The NMOS also shows low SS of 66 mV/dec and DIBL of 28 mV/dec. Both the I_d against V_g characteristics of n - and p -DNWFET are presented earlier in Fig. 3(a).

The midgap TaN gate elevates the V_T to solve the low V_T and high OFF-state leakage issues seen in polysilicon gate nanowire devices. The elevation of the V_T shifts the PMOS I_d vs V_g curve to the left and NMOS curve to the right, as indicate in Fig. 5(a) and (b). This shift allows the TaN gate device to obtain lower leakages for as much as one order of magnitude as compared to the polysilicon gate device while maintaining high drive current. Although the use of TaN metal gate further increases the V_T of the n -DNWFET, this issue can be moderated with a V_T adjustment implant or an n -type SOI substrate.

The G_m as a function of the V_g plot of Fig. 4 illustrates the fast response of the transconductance to gate voltage. The transconductance saturates after peaking, and this indicates that these devices are enjoying low field mobility even at high gate voltages. This is attributed to the cylindrical channel morphology [10] and the undoped channel. The DNWFET devices are also immune to the substrate bias, whereby the V_T remains constant when the substrate bias is swept from -6 to 6 V for both the n - and p -DNWFET. This immunity is further verified with the reference planar SOI devices that are built on the same wafer. The V_T of the reference devices change with substrate bias swept from positive to negative for PMOS and vice versa for NMOS. The substrate bias immunity is a result of the wrapped around gate shielding the channel from unwanted signals. This is illustrated in Fig. 6.

IV. CONCLUSION

We have successfully fabricated TaN gate DNWFET structures. A high drive current is achieved along with excellent SS

and DIBL. The p -DNWFET surpassed the performance of the n -DNWFET due to the higher total resistance of n -DNWFET and the lower effective hole mass. The TaN gate is clearly able to improve the gate work function to attain a higher V_T , thereby achieving a lower leakage current.

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A. L. Theng is a Technology Development Engineer with Chartered Semiconductor Manufacturing Ltd, Singapore. He received the B.S. and M.S. degree in Electrical and Electronic Engineering (EEE) from Nanyang Technological University (NTU), Singapore, in 2004 and 2008. His research interest focuses mainly on advanced sub-micron semiconductor devices and structures.

low-power application. Dr. Goh has to-date co-authored 1 book, filed 16 patents (granted), and published more than 70 research papers in international journals and conferences.

W. L. Goh is an Associate Professor at the School of Electrical and Electronic Engineering (EEE) at the Nanyang Technological University (NTU) in Singapore. She obtained both her B.Eng and Ph.D. degrees from the department of Electrical and Electronic Engineering at the Queen's University of Belfast (QUB) in United Kingdom. She is also the Assistant Head of Division at the Division of Circuits and Systems. Dr. Goh's research interests are on silicon device process technology, Nanowire SOI devices, and digital and mixed-signal IC designs for

G. Q. Lo, photograph and biography not available at the time publication.

L. Chan is a Fellow with Chartered Semiconductor Manufacturing Ltd., Singapore. He received his Ph.D. degree in Chemical Engineering from the University of Minnesota in 1985. Previously, he has held various engineering positions with Perkin-Elmer, Honeywell and Hewlett-Packard. He joined Chartered in 1993 and led a team of R&D engineers to work on 0.8 to 0.13 μm technologies, which included process module development, test chip design, and the fabrication of RF passive components. Currently, he is directly and indirectly supervising a team of fifty postgraduate students to work on advanced CMOS processes. His research interests include ultra shallow junction, next generation lithography, source/drain engineering, gate dielectric reliability, modeling/simulation, strained Si MOS device fabrication. Published more than 120 journal publications in various areas of IC device fabrication. More than 140 US patents awarded, all in the area of semiconductor IC manufacturing.

C. M. Ng, photograph and biography not available at the time publication.