An 8-bit 200-MSample/s pipelined ADC with mixed-mode front-end S/H circuit

Jiang, Shan; Do, Manh Anh; Yeo, Kiat Seng; Lim, Wei Meng

2008

Jiang, S., Do, M. A., Yeo, K. S., & Lim, W. M. (2008). An 8-bit 200-MSample/s Pipelined ADC With Mixed-Mode Front-End S/H Circuit. *IEEE Transactions on Circuits and Systems—I*. 55(6), 1430-1440.

<https://hdl.handle.net/10356/92397>

<https://doi.org/10.1109/TCSI.2008.916613>

© 2008 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder. <http://www.ieee.org/portal/site> This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

An 8-bit 200-MSample/s Pipelined ADC With Mixed-Mode Front-End S/H Circuit

Shan Jiang, Manh Anh Do, *Senior Member, IEEE*, Kiat Seng Yeo, and Wei Meng Lim

Abstract—This paper describes an 8-bit pipelined analog-to-digital converter (ADC) using a mixed-mode sample-and-hold (S/H) circuit at the front-end. The mixed-mode sampling technique reduces signal swings in pipelined ADCs while maintaining the signal-to-noise ratio. The reduction of signal swings relaxes the operational amplifier (opamp) gain, slew rate, bandwidth, and capacitor-matching requirements in pipelined ADCs. Due to the mixed-mode S/H technique, the single-stage opamps and small capacitor sizes can be used in this pipelined ADC, leading to a high speed and low-power consumption. Fabricated in a 0.18- μm CMOS process, the 8-bit pipelined ADC consumes 22 mW with 1.8-V supply voltage. When sampling at 200 MSample/s, the prototype ADC achieves 54-dB spurious free dynamic range and 45-dB signal-to-noise and distortion ratio. The measured integral nonlinearity and differential nonlinearity are 0.34 LSB and 0.3 LSB, respectively.

Index Terms—Analog-to-digital converters (ADCs), digital receiver, high-speed, operational amplifier (opamp), pipelined ADCs, sample-and-hold (S/H).

I. INTRODUCTION

THE fast growing demands on high-data-rate applications such as multimedia service are driving the bandwidth of wired and wireless communication standards upwards. For example, the data rate of the next generation of the IEEE 802.11 standard is expected to reach 540 Mb/s, and the signal bandwidth is expected to extend to 40 MHz [1].

Analog-to-digital converters (ADCs) are key components in digital communication receivers. For wideband applications such as 1000BASE-T and IEEE 802.11, an ADC resolution of 8 or 9 bits is sufficient to meet the system signal-to-noise ratio (SNR) requirement [2]–[5]. However, a sampling rate of hundreds of Msample/s is required to support the increasing signal bandwidth and to relax the anti-alias filter design. In addition, the power consumption of ADCs has to be minimized for the portable operation powered by battery.

The pipelined ADC architecture is a popular candidate for wideband receivers due to its high speed and power efficiency [6]–[9]. Most of the pipelined ADCs are implemented in

switched-capacitor (SC) circuits [10][11][12][13]. The performance of an SC implemented pipelined ADC is determined by the operational amplifier (opamp) and the capacitor size. The opamp must have high dc gain, high slew rate, and wide bandwidth to meet the accuracy and speed requirements. The opamp performance also has effects on the linearity of the sample-and-hold (S/H) circuit and pipeline stages and thus, consequently, on the overall ADC dynamic performance. The capacitor size is another impact factor that limits the pipelined ADC performance. In a medium-resolution pipelined ADC, the capacitor size is limited by matching instead of thermal noise. A large capacitor size translates to higher power consumption and lower speed.

In order to achieve a desirable SNR, a large-signal swing is required in pipelined ADCs. However, a large-signal swing has significant effects on the SC circuit performance. It increases the opamp gain and capacitor matching requirements, leading to high power consumption and slow conversion speed. A large-signal swing also deteriorates the pipelined ADC's dynamic performance. As the device size and supply voltage decrease, the effects of signal swing on opamp gain and linearity become significant. A detailed analysis of these effects is described in the next section. Thus, although single-stage cascode opamps are fast and consume less power, they are not commonly used in pipelined ADCs due to the poor gain and linearity performance at the large-signal swing [10], [12].

This paper presents a pipelined ADC with a mixed-mode S/H circuit at the front-end that reduces the signal swing. The mixed-mode sampling technique mitigates the opamp and capacitor-matching requirements both in the S/H circuit and pipeline stages. The relaxation on performance requirements enables the use of a single-stage cascode opamp and small capacitor size in a pipelined ADC without degrading the system performance. A single-stage opamp and small capacitor enable low power and high speed operation. The decrease of the signal swing also improves the whole ADC linearity.

II. IMPACT OF SIGNAL SWING ON S/H AND PIPELINED STAGES

Most pipelined ADCs include an S/H circuit at the front-end to minimize the conversion errors at high frequencies and to improve the overall system performance. The performance of the S/H circuit dominates the overall ADC dynamic characteristics and plays a major role in determining the spurious free dynamic range (SFDR) and the signal-to-noise and distortion ratio (SNDR) of the system [14].

The effects of signal swing on the performance of the S/H circuit can be illustrated by the simplified schematic of a conventional SC S/H circuit shown in Fig. 1 [15]. If the mismatch

Manuscript received March 8, 2007; revised August 1, 2007. First published February 2, 2008; last published July 10, 2008 (projected). This paper was recommended by Associate Editor T. B. Tarim.

S. Jiang was with the Center for Integrated Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technologies University, Singapore 639798. He is now with Avago Technologies, Singapore 768923 (e-mail: shanjiang@pmail.ntu.edu.sg).

M. A. Do, K. S. Yeo, and W. M. Lim are with the Center for Integrated Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technologies University, Singapore 639798.

Digital Object Identifier 10.1109/TCSI.2008.916613

Fig. 1. Conventional S/H circuit.

between C_S and C_F is ΔC , as shown in Fig. 1, the S/H output can be expressed as

$$V_{out} = \left(1 - \frac{1}{\beta \cdot A_0} - \frac{\Delta C}{C}\right) \cdot V_{in} \quad (1)$$

where A_0 is the opamp dc gain, $\beta = C/(2C + \Delta C + C_{in})$ denotes the feedback factor in the holding mode, and C_{in} is the input capacitance of the opamp. Equation (2) below shows that the S/H output has a error of $[(\Delta C/C) + (1/\beta \cdot A_0)] \cdot V_{in}$ due to the finite opamp gain and capacitor mismatch. This error is signal-dependent and aggravates as the input signal V_{in} increases.

If this S/H circuit is used in an N -bit ADC, for a full-scale step input, the error due to the finite opamp dc gain and capacitor mismatch must be less than half of the least significant bit (LSB) in order to avoid introducing any error to the following pipelined stages. Thus, the opamp gain and capacitor matching requirements have to satisfy the following condition:

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^{N+1}}. \quad (2)$$

Although an S/H gain error can be tolerated in some applications, the gain error drift must be minimized, which requires a high-opamp dc gain across temperature and process corners.

In addition, the opamp dc gain also depends on signal swing. This dependence is derived in the Appendix and can be expressed as

$$A \approx A_0 \left(1 - \frac{V_{in}^2}{8V_{eff1}^2}\right) \quad (3)$$

where A_0 is the opamp dc gain when the output is zero. $V_{eff1} = (V_{GS} - V_{TH})_1$ is the overdrive voltage of the opamp input transistor. Because the opamp dc gain varies with signal swing, the gain requirement in (2) should be the gain when a largest output swing is applied. At this condition, the required zero output opamp dc gain is usually much larger than that given by (2).

The variation of the opamp gain during its operation in turn introduces nonlinearity in the S/H output. Including the opamp gain variation, the output of the S/H circuit in Fig. 1 is derived in the Appendix as

$$V_{out} = \left(1 - \frac{1}{\beta \cdot A_0} - \frac{\Delta C}{C}\right) V_{in} + \frac{(2C + \Delta C)^3}{\beta \cdot A_0^3} V_{in}^3. \quad (4)$$

Equation (4) indicates the dependence of the S/H nonlinearity on the input signal. The above analysis does not take into account the nonlinearity due to the device transconductance g_m and output impedance r_o variations with the output swing.

Fig. 2. Opamp gain variation with output swing.

Fig. 3. MDAC in a 1.5-bit stage.

These two factors also contribute a large amount of nonlinearity with the device size and supply voltage decreases [16], [17]. An opamp gain variation with the output swing is shown in Fig. 2.

The speed of an S/H circuit is determined by the settling time of the opamp that can be categorized into the nonlinear slewing time and the quasilinear settling time. The requirement of opamp unity-gain bandwidth ω_u in an N -bit S/H circuit ignoring the slew time is given by

$$\omega_u > \frac{2 \cdot (N + 1) \cdot f_s \cdot \ln 2}{\beta} \quad (5)$$

where f_s is the ADC sampling frequency and β is the feedback factor. The opamp unity-gain bandwidth is directly related to the capacitive load. The larger the load capacitance, the higher the power is required to achieve a given bandwidth.

In practice, the opamp bandwidth needs to be larger than the value given by (5) to take into account the slewing time and nonoverlapping clock phases. For speed consideration, the slewing time should be minimized, which requires a high opamp slew rate. The opamp with a high slew rate settles to the final value in the linear settling phase. Therefore, even if the opamp is not fully settled at the end of the hold mode, there is only a linear error, and an improvement of the dynamic performance can be expected. Since the slew rate of the opamp is determined by the output swing, the capacitive load, and the sampling frequency, a reduced output swing and smaller capacitive load can improve the S/H speed and accuracy.

Fig. 4. Detailed diagram of the proposed 8-bit pipelined ADC.

The first stage of the pipeline also has the most stringent performance requirement. It has been proved that, for a pipelined ADC with medium resolution, the resolution of 1.5 bits per stage will give the optimized implementation [19]. The simplified schematic of the multiplexing DAC (MDAC) in a 1.5-bit stage is shown in Fig. 3. In an N -bit ADC, for the output error to be less than half LSB of the remaining resolution, the opamp gain and capacitor matching requirement is

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C} \right) < \frac{1}{2^N} \quad (6)$$

and the opamp bandwidth requirement is

$$\omega_u > \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta}. \quad (7)$$

Similar to the S/H circuit, the signal swing also has significant effects on the performance of the first stage as shown in (6) and (7).

III. PROPOSED ADC ARCHITECTURE

The above discussions show that the signal swing has a significant influence on the whole ADC performance. In order to reduce the signal swing, we propose a pipelined ADC with a mixed-mode S/H circuit at the front-end as shown in Fig. 4. The mixed-mode S/H circuit decreases the input signal swing and has 1-bit digital output [18]. Following the S/H circuit are six modified 1.5-bit stages. The S/H reduces the input signal swing and maintains it within the range of $-3V_{\text{ref}}/4 + 3V_{\text{ref}}/4$. Hence, the input of the 1.5-bit stage is limited within the same range. Therefore, all of the pipelined stage outputs do not need a full-scale swing, and the opamp and capacitor matching requirement are relaxed. The last stage is implemented in a 2-bit flash ADC. The digital output of the pipeline stages and the 1-bit output from the S/H circuit are sent to the digital error correction logic to remove the comparator offset errors and generate the 8-bit digital output. Since the prototype ADC is going to be tested on-wafer, a decimation circuit decimates the output data by eight and the 8-bit output data are serialized by the serialization circuit, becoming 1-bit output so that we do not need eight high-speed probes to tap the data out. The biasing block supplies the biasing currents to the S/H and pipeline stages. The nonoverlapping clocks are generated by the clock generator.

Fig. 5. Mixed-mode S/H circuit.

IV. CIRCUIT IMPLEMENTATION

A. Mixed-Mode S/H Circuit

The schematic of the mixed-mode S/H circuit is shown in Fig. 5. Although shown in single-end configuration, the S/H circuit is implemented in the fully differential configuration in our circuit. One comparator is added to the conventional S/H circuit. The S/H operation is controlled by two nonoverlapping clock phases, namely sampling phase ϕ_1 and holding phase ϕ_2 . ϕ_{1a} is a copy of ϕ_1 but with an earlier falling edge. During the sampling phase, switches controlled by ϕ_1 and ϕ_{1a} are on, and the sampling capacitor C_S is charged to $V_{\text{in}} - V_{\text{os}}$ with the aid of the virtual ground formed by the opamp in the unity-gain configuration. V_{os} presents the offset voltage of opamp. Meanwhile, the feedback capacitor C_F is charged to V_{os} . The sampling phase ends at the falling edge of ϕ_{1a} . At the same clock edge, the comparator quantizes the input signal and generates the digital output D_{out} . Subsequently, ϕ_1 turns off the input switches and the bottom plate of C_S is connected to either $+V_{\text{ref}}/2$ or $-V_{\text{ref}}/2$, determined by the value of D_{out} . The S/H circuit is in the holding mode and the opamp offset is eliminated by the auto-zero technique [23]. As a result, the transfer function of the mixed-mode S/H circuit is given as

$$V_{\text{out}} = \left(1 - \frac{1}{\beta \cdot A_0} - \frac{\Delta C}{C} \right) [V_{\text{in}} + (-1)^{D_{\text{out}}} \times V_{\text{ref}}/2] \quad (8)$$

Fig. 6. Transfer curve of the mixed-mode S/H circuit.

where

$$D_{OUT} = \begin{cases} 1, & \text{for } V_{in} \geq 0 \\ 0, & \text{for } V_{in} < 0 \end{cases} \quad (9)$$

$$\beta = C/(2C + \Delta C + C_{in}). \quad (10)$$

The sampled data are represented both in analog and digital forms. The transfer curve of this mixed-mode S/H circuit is illustrated in Fig. 6. Also shown is the 1-bit digital output sent to the digital error correction logic. The dashed line shows the transfer curve of the conversional S/H circuit in Fig. 1. As expected, the output swing of the proposed S/H circuit is reduced and does not exceed the range $-3V_{ref}/4$ to $+3V_{ref}/4$ as long as the comparator offset error is smaller than $\pm V_{ref}/4$. The effective gain of the proposed S/H circuit equals 1, which is the same as in [15]. The reduced analog signal swing does not degrade the SNR or stress the following pipelined stage since now the information is stored both in analog and digital forms and the full scale range is maintained.

Although the full-scale input is unchanged, the effective input signal to the opamp is reduced by $V_{ref}/2$, as can be seen in (8). Therefore, the maximum error introduced by finite opamp dc gain and capacitor mismatch is $[(\Delta C/C) + (1/\beta \cdot A_0)] \cdot FS/2$ in the mixed-mode S/H circuit. If this S/H circuit is used in an N -bit ADC, for the error to be less than $LSB/2$, the opamp gain and capacitor matching requirements become

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C} \right) < \frac{1}{2^N} \quad (11)$$

which is 6 dB lower than the requirement for the conventional S/H circuit as expressed in (2). The mixed-mode S/H circuit also reduces the opamp bandwidth requirement which is now given by

$$\omega_u > \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta}. \quad (12)$$

Although this configuration increases the gain error when the input is in the vicinity of zero, as shown in Fig. 6, this error is still within the range of $LSB/2$ of the full scale. Due to the reduced signal swing, the capacitors C_S and C_F have a very small value of 200 fF. In addition, since the output swing is reduced, the

Fig. 7. Two signal paths in the sampling mode.

opamp dc gain is more stable, and therefore an improvement of the S/H circuit linearity is expected.

Although a dedicated front-end S/H circuit can be removed and the sampling function is performed in the first stage of a pipelined ADC, the input capacitance of the pipelined ADC in such an implementation is significantly increased due to the multibit first-stage configuration [20], [21]. A large input capacitance stresses the driving circuit of the ADC, such as a variable gain amplifier (VGA) in digital receiver applications. In some solutions, the full-scale input range of the ADC is reduced and so is the achievable dynamic range [22]. The time constant matching is another concern in a pipelined ADC without a front-end S/H circuit. Although the aperture errors due to the time constant mismatch can be treated as comparator offset errors and removed by the digital error correction logic, due to the high gain of the multibit first stage, it is easy for the aperture errors to saturate the S/H circuit output swing. This sets a limit on the highest working frequency of the pipelined ADC without a front-end S/H circuit. Therefore, a dedicated front-end S/H is necessary in these considerations.

Due to the additional comparator, in the sampling mode, there are two signal paths in the mixed-mode S/H circuit. One is formed by the sampling switch, the sampling capacitor C_S , and the opamp. The other goes through the comparator. Because of the time-constant difference between these two paths, there exists an aperture error which is increased with the input frequency. However, it is possible to minimize this error by matching the two signal paths in terms of topology and time constant [24]. Fig. 7 shows the two signal paths during the sampling period. Instead of connecting the comparator directly to the input signal, it is connected to the output of the sampling switch. Thus, the two paths see the same delay caused by the sampling switch. In addition, the opamp and the comparator both use the falling edge of ϕ_{1a} to sample and quantize the input signal.

In actual implementation, it is difficult to match these two signal paths particularly at high frequency due to parasitic components and second-order effects. However, based on the characteristic of pipelined ADCs, the aperture error due to time constant mismatch can be treated as comparator offset error and eliminated by the digital error correction logic. Although this error can be tolerated in a pipelined ADC, the errors caused by opamp offset and comparator offset will increase the output swing, occupy a large offset correction range, and degrade the efficiency of the mixed-mode sampling technique. Therefore, in

Fig. 8. Modified 1.5-bit stage.

this design, the auto-zero technique is used for the opamp in the sampling mode to eliminate its offset error. This is realized by connecting the opamp in the unity-gain configuration during the sampling mode. The comparator does not employ the auto-zero configuration because of the speed consideration. Otherwise, the comparator has to quantize the input signal during the hold mode, which leads to a higher opamp speed requirement or complicates the timing scheme that uses a shorter sampling phase to increase the time slot for amplifying. In addition, the low gain of the S/H circuit (equals to 1) also minimize the aperture error. In the worst case simulation, the aperture error is less than 20 mV when a 99-MHz input is sampled at 200 MS/s in the presence of 7-mV comparator offset error.

B. Modified 1.5-bit Pipeline Stage

In the mixed-mode S/H circuit, the sampling capacitor C_S is connected to either $+V_{\text{ref}}/2$ or $-V_{\text{ref}}/2$ during the holding mode. Although two additional reference voltages $+V_{\text{ref}}$ and $-V_{\text{ref}}$ can be used to implement conventional 1.5-bit pipeline stages, the implementation of additional reference voltage circuits will increase the overall circuit complexity, power consumption, and die size. Therefore, in this design, all of the pipelined stages will use the same reference $\pm V_{\text{ref}}/2$ employed in the mixed-mode S/H circuit.

The pipelined stages 2–6 in this ADC are implemented in the modified 1.5-bit stage as illustrated in Fig. 8. It has similar configuration as that of the mixed-mode S/H circuit. Because the half reference is used, the capacitor C_S is twice the size of C_F , as shown in Fig. 8. In the sampling phase ϕ_1 , the input signal is sampled by capacitor C_S . At the end of ϕ_1 , the two comparators, which have threshold voltages at $-V_{\text{ref}}/4$ and $+V_{\text{ref}}/4$, respectively, quantize the input signal and generate the digital output 00, 01, or 10. During the amplifying phase ϕ_2 , C_S

is connected to $+V_{\text{ref}}/2$, 0, or $-V_{\text{ref}}/2$ according to the comparator outputs. The feedback capacitor C_F is reset at the sampling phase and connected around the opamp during the amplifying phases. The auto-zero implementation eliminates the opamp offset error. The transfer function of the modified 1.5-bit stage is the same as the conventional 1.5-bit stage, which is

$$V_{\text{out}} = \left(1 - \frac{1}{A_0 \cdot \beta} - \frac{\Delta C}{C}\right) (2 \cdot V_{\text{in}} + D \cdot V_{\text{ref}}) \quad (13)$$

where $\beta = C/(3C + \Delta C + C_{\text{in}})$ is the feedback factor. C_{in} denotes the opamp parasitic input capacitance. D has the value of -1 , 0 , or 1 .

The transfer curve of the modified 1.5-bit stage ignoring the opamp finite gain and capacitor mismatch is shown in Fig. 9. Since the mixed-mode S/H circuit limits its output within $-3V_{\text{ref}}/4$ to $+3V_{\text{ref}}/4$, the output of the 1.5-bit stage will not exceed $\pm V_{\text{ref}}/2$ theoretically. To guarantee that all of the pipeline stages work in half signal swing, the maximum comparator offset error in the modified 1.5-bit stage should be smaller than $V_{\text{ref}}/8$.

With the output swing reduced, the opamp gain and capacitor matching requirements in pipelined stages are also relaxed for the same reasons discussed on the mixed-mode S/H circuit. For the first 1.5-bit stage with 1-bit effective resolution, the remaining resolution for the following stages is $N - 1$ bits. The opamp gain and capacitor matching requirements are reduced to

$$\left(\frac{1}{\beta \cdot A_0} + \frac{\Delta C}{C}\right) < \frac{1}{2^{N-1}} \quad (14)$$

which is 6 dB lower than the requirement for the conventional 1.5-bit stage as expressed in (6).

Assume the opamp parasitic input capacitance size is half of C_F and the feedback factor of the modified 1.5-bit stage is $\beta = C_F/(C_F + 2C_S + C_{\text{in}}) = 2/7$. The feedback factor of the modified 1.5-bit stage is smaller than that of conventional 1.5-bit

Fig. 9. Tcurve of the modified 1.5-bit stage.

stage, which is $\beta = C_F / (C_F + C_F + C_F/2) = 2/5$. Due to the half output swing, however, the opamp gain requirement in the modified 1.5-bit stage is reduced by

$$\Delta A_0 = 20 \log \left(\frac{5}{2} \times 2^N \right) - 20 \log \left(\frac{7}{2} \times 2^{N-1} \right) = 3 \text{ dB}. \quad (15)$$

Since in the medium-resolution pipelined ADC, the opamp can be designed at a relatively low gain, a smaller capacitor can be chosen to take the advantage of signal swing reduce. In this design, the value of C_F was chosen to be 100 fF which is the minimum capacitor size supported by the process chosen. The foundry design guide shows that the 100-fF capacitance has a 3σ mismatch smaller than 0.6%. For an 8-bit pipelined ADC in a conventional implementation, the mismatch should be less than 0.39%.

Since the output amplitude is less than half of the full scale, the opamp bandwidth requirement in the modified 1.5-bit stage is

$$\omega_u > \frac{2 \cdot (N-1) \cdot f_s \cdot \ln 2}{\beta}. \quad (16)$$

Assuming the capacitive load of the modified 1.5-bit stage is C_L , the input transistor transconductance of the opamp can be express as

$$\begin{aligned} g_m &= \omega_u \cdot C_L \\ &= \frac{2 \cdot (N-1) \cdot f_s \cdot \ln 2}{\beta} \cdot C_L \\ &= 7(N-1) \cdot f_s \cdot \ln 2 \cdot C_L. \end{aligned} \quad (17)$$

In the conventional 1.5-bit stage, the signal swing equals the full scale. Therefore, a better capacitor matching is required, and consequently a larger capacitor is needed. For the conventional 1.5-bit stage to achieve the same accuracy as the modified 1.5-bit stage which has a capacitive load of C_L and signal swing of $FS/2$, the capacitive load of the conventional 1.5-bit stage needs to be $2C_L$. Hence, the input transistor transconductance of the opamp in the conventional 1.5-bit stage is

$$\begin{aligned} g_m &= \omega_u \cdot 2C_L \\ &= \frac{2 \cdot N \cdot f_s \cdot \ln 2}{\beta} \cdot 2C_L \\ &= 10N \cdot f_s \cdot \ln 2 \cdot C_L. \end{aligned} \quad (18)$$

Fig. 10. Telescopic opamp with gain boosting.

The opamp power consumption is proportional to the g_m of the input transistor. Therefore, although the modified 1.5-bit stage has a smaller feedback factor compared with that of the conventional design, the power consumption of the modified stage is lower due to the smaller capacitive load. Moreover, the reduced signal swing and capacitor size reduce the opamp slew rate requirement as well, and, thus, an improved speed is expected.

C. Opamp

The gain-boosted single-stage telescopic opamp used in the S/H circuit and the pipelined stages is shown in Fig. 10. Transistors M_1 - M_9 form the main telescopic opamp. To improve the opamp gain, transistors M_{10} , M_{12} , and M_{11} , M_{13} form two common-source amplifiers and introduce negative feedback loops that make the source voltages of the common-gate transistors M_3 and M_4 less sensitive to the output signal. The gain boosting is only applied to the nMOS cascode transistors. The output impedance of the pMOS active load are increased by increasing the channel length of M_7 and M_8 , since the size of these two devices have less effect on the opamp frequency response. Since the opamp output swing requirement was reduced, the gate voltages of M_3 and M_5 are modified to increase the V_{ds} of M_1 M_2 M_7 M_8 for a higher dc gain. The same opamps used in the S/H circuit and the first 1.5-bit stage have a simulated dc gain of 64 dB. The opamps in other pipeline stages have the same architecture as Fig. 10 but with the biasing current scaled down along the pipeline.

D. Comparators

To reduce the static power consumption, the dynamic comparator is used in the mixed-mode S/H circuit as shown in Fig. 11. The differential pair M_1 and M_2 amplify the input signal and transistors M_4 M_7 form a regeneration latch. When ϕ_{1a} is high, V_{out+} and V_{out-} are reset to VDD via M_8 and M_9 . When ϕ_{1a} goes low, the differential pair M_1 and M_2 compare the input V_{in+} and V_{in-} and generate voltage difference at the drain of transistors M_4 and M_5 . This voltage difference is amplified by the positive feedback of the latch therefore V_{out+}

Fig. 11. Dynamic comparator used in S/H.

and V_{out-} goes to VDD or ground according to the input voltages. The offset of this comparator can be expressed as [25]

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2} \left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R} \right) \quad (19)$$

where $V_{TH1,2}$ is the threshold voltage mismatch of transistor M_1 and M_2 . $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2 . ΔR is the load resistance mismatch, which is contributed by transistors $M_4 \sim M_7$. The offset voltage in this comparator is dominated by the mismatch between transistor M_1 and M_2 . Mismatch caused by other transistors is reduced by the gain of M_1 and M_2 . The offset can be reduced by decreasing $(V_{GS} - V_{TH})_{1,2}$, which is controlled by the tail current of the differential pair. Therefore, the gate of M_3 is connected to V_{BIAS} instead of clock ϕ_{1a} to reduce the offset error. For a 20% device dimension mismatch manually introduced, this comparator has an offset error of less than 7 mV in the worst case simulation.

The comparator used in pipelined stages is shown in Fig. 12. The two threshold voltages $+V_{ref}/4$ and $-V_{ref}/4$ are generated by the dimension ratio between M_1 , M_2 , M_3 and M_{1a} , M_{2a} , M_{3a} [25]. The gates of M_3 and M_{3a} are connected to a constant biasing voltage V_{BIAS} to reduce offset error. In the worst case simulation, this comparator has an offset error of less than 22 mV.

E. CMOS Switches

The size of switches used in a pipelined ADC usually is limited by the time constant and linearity. Since the signal swing is reduced, a smaller switch size is employed in the prototype ADC to reduce the capacitive load of the opamp and improve speed. The input sampling switches of the mixed-mode S/H are implemented in a bootstrapped configuration to minimize the nonlinearity introduced by signal-dependent switch-on resistance [26]. Other switches are implemented in CMOS transmission gate with a W/L ratio of $8 \mu\text{m}/0.18 \mu\text{m}$ which has been proved to be sufficient to 8-bit application in simulation with 300-mV_{pp} voltage swing.

Fig. 12. Differential dynamic comparator in pipeline stages.

F. Decimation and Serialization Blocks

In order to make the prototype ADC testable on-wafer, the 8-bit digital output are decimated by 8 and serialized. Therefore, only one output pad is needed to test the prototype ADC. The decimation and serialization blocks are shown in Fig. 13. Also shown is the timing diagram of the decimation and serialization blocks. First, the sampling clock is divided by 8. The CLK/8 triggers eight D-Flip-Flops to store the output every eight sampling clock cycles. The serialize block outputs 1-bit output every sampling clock cycle, and it takes eight clock cycles to output the whole 8-bit output.

V. MEASURED RESULTS

The pipelined ADC has been fabricated using the chartered 0.18- μm 2P6M CMOS process. The microphotograph of the die is shown in Fig. 14. This chip occupies $0.8 \times 1.2 \text{ mm}^2$ and the active area is $0.4 \times 0.8 \text{ mm}^2$. The measured power consumption is 22 mW excluding the decimation, serialization, and output buffer with 1.8-V supply voltage.

The ADC is tested on-wafer. The differential input signals, the reference voltages, and analog supply and ground are applied to the ADC through a Cascade multicontact Eye-Pass 10-pin probe. This probe also has a 450-nF built-in decoupling capacitor between power line and ground. The differential clock signals are injected through a Cascade Infinity GSSG probe. The digital supply and ground are brought in by a Cascade dc probe. The analog supply and digital supply are connected together outside the chip. The output data are tapped out by a Cascade Infinity GSG probe, stored in an oscilloscope and analyzed using MATLAB.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.3 LSB and 0.34 LSB when sampling at 200 MSample/s, as plotted in Figs. 15 and 16, respectively. The INL curve has three jumps and is similar to the INL of a pipelined ADC with 2-bit first stage. This is due to the combination of the 1-bit S/H digital output and the 1.5-bit first stage

Fig. 13. Decimation and serialization blocks and timing.

Fig. 14. Microphotograph of the pipelined ADC.

Fig. 17. FFT plot of 90-MHz input at 200 MSample/s.

Fig. 15. Measured DNL plot.

Fig. 16. Measured INL plot.

output, which makes this ADC have a similar INL plot as that of a 2-bit first stage.

Fig. 17 shows the measured fast Fourier transform (FFT) plot of a 90.723-MHz input with 200 MSample/s, where about 54.5 dB SFDR and 44.8 dB SNDR are observed. The distortion

Fig. 18. SNDR and SFDR versus input frequency at 200 MSample/s.

is dominated by the third harmonic with the frequency of $|1 \times 200 \text{ MHz} - 3 \times 90.723 \text{ MHz}| = 72.169 \text{ MHz}$. Plotted in Fig. 18 are the measured SNDR versus the SFDR as functions of the input signal frequency while the ADC samples at 200 MSample/s. The SFDR drops at high input frequency due to the increasing of aperture error in the mixed-mode S/H circuit, which increases the signal swing in pipeline stages. The measured SNDR and SFDR as functions of sampling frequency are plotted in Fig. 19 with a 40-MHz input signal. The SNDR and SFDR are approximately constant for low

Fig. 19. SNDR and SFDR versus sampling frequency with 40-MHz input.

TABLE I
PERFORMANCE SUMMARY

Technology	0.18 μ m 2P6M CMOS
Resolution	8-bit
Sampling Rate	200 MS/s
Supply Voltage	1.8 V
Input Range	0.8 V _{pp}
DNL / INL	0.3 LSB / 0.34 LSB
SNDR (f_{in} =40 MHz)	45.2 dB
SNDR (f_{in} =99 MHz)	44.2 dB
SFDR (f_{in} =40 MHz)	60.4 dB
SFDR (f_{in} =99 MHz)	53.4 dB
Active Area	0.8mm $\times$ 0.4mm
Power Consumption	22 mW

sampling rate and start to drop as the sampling rate gets larger than 180 MHz. The effective number of bits (ENOB) when sampling a 40-MHz signal at 200 MSample/s is 7.2 bits, drops to 7 bits at 220 MSample/s, and further down to 6.5 bits at 250 MSample/s.

The measured ADC results are summarized in Table I. The reported performance of 8-bit high speed pipelined ADCs are compared in Table II in which the figure of merit (FOM) is defined as

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} \cdot f_s} \quad (20)$$

where P is power consumption and f_s is sampling frequency. The FOM of this work is 0.74 pJ/conversion, which is comparable with other reports in similar technologies.

VI. CONCLUSION

This paper presents the mixed-mode sampling technique that reduces the signal swing in a pipelined ADC. The reduced signal swing relaxes the opamp gain, bandwidth, slew rate, and capacitor-matching requirements, which leads to high speed and low power consumption. A modified 1.5-bit stage is proposed to cooperate with the mixed-mode S/H circuit. Small capacitor sizes are used in the prototype ADC to verify the mixed-mode sampling technique. Fabricated in an 0.18- μ m CMOS process, the

TABLE II
PERFORMANCE COMPARISON

8-b ADC	Tech.(μ m)	ENOB	f_s (MHz)	Power(mW)	FOM
[2]	0.18	7.25	150	71	3.1
[28]	0.13	7.6	125	21	0.87
[27]	0.18	7.68	200	30	0.73
This work	0.18	7.2	200	22	0.74

Fig. 20. Differential amplifier.

proposed pipelined ADC shows 7.2 ENOB at 200 MSample/s with only 22-mW power consumption.

APPENDIX

The opamp dc gain depends on input and output signal swing, which can be illustrated by the differential amplifier shown in Fig. 20. In this amplifier, the current difference $\Delta I = I^+ - I^-$ can be expressed as

$$\begin{aligned} \Delta I &= \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} V_{in} \sqrt{\frac{I}{\mu_n C_{ox} \frac{W_1}{L_1}} - V_{in}^2} \\ &= \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} V_{in} \sqrt{4(V_{GS} - V_{TH})_1^2 - V_{in}^2} \\ &= \mu_n C_{ox} \frac{W_1}{L_1} (V_{GS} - V_{TH})_1 V_{in} \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \\ &= g_{m1} V_{in} \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \end{aligned} \quad (21)$$

where L_1 , W_1 , and g_{m1} are the channel length, width, and transconductance of M_1 , respectively. The output impedance of the amplifier is $r_{o1} || r_{o3}$. Assuming $r_{o1} = r_{o3}$, the gain of the amplifier equals

$$\begin{aligned} A &= \Delta I \frac{r_{o1}}{2} / V_{in} \\ &= g_m \frac{r_{o1}}{2} \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})_1^2}} \\ &\approx A_0 \left(1 - \frac{V_{in}^2}{8V_{eff}^2} \right) \end{aligned} \quad (22)$$

where $A_0 = g_m r_{o1} / 2$ is the amplifier dc gain when the output is zero. $V_{eff} = (V_{GS} - V_{TH})_1$ is the input transistor overdrive voltage.

In a short-channel device, r_o varies significantly with the drain–source voltage V_{DS} . In the saturation region, this dependence can be approximated as

$$r_o = \frac{2L}{1 - \frac{\Delta F}{L}} \frac{1}{I} \sqrt{\frac{qN_B}{2\epsilon_{si}}} (V_{DS} - V_{dsat}). \quad (23)$$

The variation of r_o gives rise to the nonlinearity in an opamp. The amount of nonlinearity is heavily dependent on how much the output signal swing, i.e., how much the V_{DS} changes. In addition, the transistor transconductance g_m also varies with V_{DS} , which further exacerbates the opamp nonlinearity since the voltage gain is determined by $g_m \cdot r_o$.

The nonlinear opamp dc gain is an important source of nonlinearity error in the S/H circuit. This harmonic distortion can be analyzed via charge conservation in SC circuits. If we replace the A_0 in (1) with A in (22) and ignore the capacitor mismatch, the transfer function of the S/H circuit in Fig. 1 can be rewritten as

$$\begin{aligned} V_{out} &\approx V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A} \right) \\ &\approx V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A_0} \cdot \frac{1}{1 - \frac{V'^2}{8V_{eff}^2}} \right) \end{aligned} \quad (24)$$

where V' is the voltage at the opamp input, which can be approximated as

$$V' \approx -\frac{V_{out}}{A_0} \approx -\frac{V_{in} \cdot \frac{C_S}{C_F}}{A_0}. \quad (25)$$

Therefore

$$\begin{aligned} V_{out} &\approx V_{in} \frac{C_S}{C_F} \left[1 - \frac{1}{\beta \cdot A_0} \cdot \frac{1}{1 + \frac{V_{in}^2 \cdot (C_S/C_F)^2}{A_0^2}} \right] \\ &\approx V_{in} \frac{C_S}{C_F} \left[1 - \frac{1}{\beta \cdot A_0} \cdot \left(1 - \frac{V_{in}^2 \cdot (C_S/C_F)^2}{A_0^2} \right) \right] \\ &= V_{in} \frac{C_S}{C_F} \left(1 - \frac{1}{\beta \cdot A_0} \right) + \frac{(C_S + C_F)^3}{\beta \cdot A_0^3} V_{in}^3. \end{aligned} \quad (26)$$

REFERENCES

- [1] J. M. Wilson, "The next generation of wireless LAN emerges with 802.11n," *Technol. Intel Mag.*, pp. 1–8, Aug. 2004.
- [2] S. Limotyrakis, S. D. Kulchayki, D. K. Su, and B. A. Wooley, "A 150-MS/s 8-bit 71-mW CMOS time-interleaved ADC," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1057–1067, May 2005.
- [3] J. Huang and R. R. Spencer, "The design of analog front ends for 1000BASE-T receivers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 10, pp. 675–684, Oct. 2003.
- [4] "Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications High-Speed Physical Layer in the 5 GHz Band," Sep. 1999.
- [5] "Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band," Jun. 2003.
- [6] T. H. Meng, B. McFarland, D. Su, and J. Thomson, "Design and implementation of an all-CMOS 802.11a wireless LAN chipset," *IEEE Commun. Mag.*, pp. 160–168, Aug. 2003.
- [7] M. Zargari, M. Terrovitis, S. H.-M. Jen, B. J. Kaczynski, D. K. Su, and B. A. Wooley, "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2239–2249, Dec. 2004.
- [8] S. S. Mehta, D. Weber, M. Terrovitis, K. Onodera, T. H. Meng, and B. A. Wooley, "An 802.11g WLAN SoC," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2483–2491, Dec. 2004.
- [9] S. Khorram, H. Darabi, Z. Zhou, Q. Li, T. F. J. Trachewsky, and A. Rofougaran, "A fully integrated SoC for 802.11b in 0.18- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2492–2501, Dec. 2005.
- [10] J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla, "Low-power pipeline ADC for wireless LANs," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1338–1340, Aug. 2004.
- [11] J. Li and U.-K. Moon, "A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1468–1476, Sep. 2004.
- [12] I. Ahmed and D. A. Johns, "A 50-MS/s (35 mW) to 1-KS/s (15 μ W) power scalable 10-bit pipelined ADC using rapid power-in opamps and minimal bias current variation," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2446–2455, Dec. 2005.
- [13] B. Xia, A. V. Garcia, and E. S. Sinencio, "A 10-bit 44-MS/s 20-mW configurable time-interleaved pipeline ADC for a dual-mode 802.11b/bluetooth receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 530–539, Mar. 2006.
- [14] W. Kester, *Data Conversion Handbook*. Amsterdam, The Netherlands: Elsevier, 2005.
- [15] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, Mar. 2000.
- [16] K. Lee and R. G. Meyer, "Low-distortion switched-capacitor filter design techniques," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1103–1113, Dec. 1985.
- [17] W. M. Sansen, H. Qiuting, and K. A. I. Halonen, "Transient analysis of charge transfer in SC filters—gain error and distortion," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 268–276, Apr. 1987.
- [18] S. Jiang, M. A. Do, and K. S. Yeo, "A 200-MHz CMOS mixed-mode sample-and-hold circuit for pipelined ADCs," in *Proc. IFIP Int. Conf. Very Large-Scale Integr.*, Nice, France, Oct. 2006, pp. 352–365.
- [19] S. H. Lewis, "Optimizing the stage resolution in pipelined, multistage analog-to-digital converter for video-rate applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, Aug. 1992.
- [20] S. Bardsley, C. Dillon, R. Kummarguntla, C. Lane, A. M. A. Ali, B. Rigsbee, and D. Combs, "A 100-dB SFDR 80-MSPS 14-bit 0.35- μ m BiCMOS pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2144–2153, Sep. 2006.
- [21] T. N. Andersen, B. Hernes, A. Briskemyr, F. Telstø, J. Bjørnsen, T. E. Bonnerud, and Ø. Moldsvor, "A cost-efficient high-speed 12-bit pipeline ADC in 0.18- μ m digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1506–1513, Jul. 2005.
- [22] M. Yoshioka, M. Kudo, K. Gocho, and Y. Watanabe, "A 10b 125 MS/s 40 mW pipelined ADC in 0.18 μ m CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 282–283.
- [23] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effect of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.
- [24] D.-Y. Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 11, pp. 2123–2132, Nov. 2004.
- [25] L. Sumanen, M. Waltari, and K. A. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1048–1055, Jul. 2001.
- [26] M. Dessouky and A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits," *Electron. Lett.*, vol. 35, pp. 8–10, Jan. 1999.
- [27] H.-C. Kim, D.-K. Jeong, and W. Kim, "A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 4, pp. 795–801, Apr. 2006.
- [28] J. Mulder, C. M. Ward, C.-H. Lin, D. Kruse, K. Bult, and F. M. L. van der Goes, "A 21-mW 8-bit 125-MSample/s ADC in 0.09- μ m² 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2116–2125, Dec. 2004.

Shan Jiang received the B.S. degree (with honors) in microelectronics from Peking University, Peking, China, in 1998. He is currently working toward the Ph.D. degree at the School of Electrical and Electronic Engineering, Nanyang Technologies University, Singapore.

From 1998 to 2003, he was a System Engineer with Motorola, Beijing, China. He is currently a Design Engineer with Avago Technologies, Singapore. His current work focuses on data conversion and optical sensor technologies.

Manh Anh Do (SM'05) received the B.Sc. degree in physics from the University of Saigon, Saigon, Vietnam, in 1969 and the B.E. and Ph.D. degrees from the University of Canterbury, Canterbury, New Zealand, in 1973 and 1977, respectively, both in electronics.

Between 1977 and 1989, he held various positions, including Design Engineer, Production Manager, and Research Scientist in New Zealand and Senior Lecturer with National University of Singapore.

He joined the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, as a Senior Lecturer in 1989 and became an Associate Professor in 1996 and Professor in 2001. He has been a consultant for many projects in the electronic industry and was a key consultant for the implementation of the \$200 million Electronic Road Pricing (ERP) project in Singapore from 1990 to 2001. His current research is on mobile communications, RF IC design, mixed-signal circuits, and intelligent transport systems. Before that, he specialized in sonar designing and biomedical signal processing. He has authored and coauthored over 200 papers in the areas of electronic circuits and systems. Between 1995 and 2005, he was Head of Division of Circuits and Systems, NTU. Currently, he is the Director of Centre for Integrated Circuits and Systems, NTU.

Dr. Do is a Fellow of IET and is a Chartered Engineer. He was a council member of IET, U.K., from 2001 to 2004 and an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES in 2005 and 2006.

Kiat Seng Yeo received the B.Eng. degree in electronics (Hons) and the Ph.D. degree in electrical engineering from Nanyang Technological University, Singapore, in 1993 and 1996, respectively.

He began his academic career as a Lecturer in 1996 and was promoted to Assistant Professor in 1999 and then to Associate Professor in 2002. He was Sub-Dean (Student Affairs) from 2001 to 2005. During this period, he held several concurrent appointments as Program Manager of the System-on-Chip flagship project, Coordinator of the Integrated Circuit Design

research group and Principal Investigator of the Integrated Circuit Technology research group at NTU. He is a member of the advisory committee of the Centre for Science Research & Talent Development of Hwa Chong Junior College and acts as consultant/advisor to statutory boards and multinational corporations in the areas of semiconductor devices, electronics, and integrated circuit design. He has authored three books, *Low-Voltage, Low-Power VLSI Subsystems* (McGraw-Hill, 2005), *Low-Voltage Low-Power Digital BiCMOS Circuits: Circuit Design, Comparative Study, and Sensitivity Analysis* (Prentice-Hall, 2000), and *CMOS/BiCMOS ULSI: Low-Voltage, Low-Power* (Prentice-Hall, 2002). The latter was translated to Chinese version and is currently a superior foreign textbooks in China. He has filed and/or been granted more than six patents and has published over 200 articles on CMOS/BiCMOS technology and integrated circuit design in leading technical journals and conferences worldwide.

Prof. Yeo was the Technical Chair of the 8th and 9th International Symposium on Integrated Circuits, Devices and Systems (ISIC-1999 and ISIC-2001, respectively), and he also served on the program committee of the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) in Taiwan and the International Symposium on Low-Power and High-Speed Chips (COOL Chips) in Japan in 1999 and 2002, respectively. He has been appointed Head of Circuits and Systems for a period of three years starting July 2005. He is a technical reviewer for several prestigious international journals and was listed in *Marquis Who's Who in the World* and *Marquis Who's Who in Science and Engineering*.

Wei Meng Lim received the B.E. (Hons.) and M.E. degrees from Nanyang Technology University (NTU), Singapore, in 2002 and 2004, respectively.

Upon graduation, he joined NTU as a Research Staff Member. His research interests include RF circuit design, RF device characterization, and modeling.