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N-type behavior of ferroelectric-gate carbon nanotube network transistor

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Carbon nanotube field effect transistor has attracted much attention recently and is a promising candidate for next generation nanoelectronics. Here, we report our study on a transistor using single wall carbon nanotube network as the channel and a ferroelectric film as the gate dielectric. The spontaneous polarization of ferroelectric materials offers nonvolatility and controllability of the surface charges. Modulation of $>10^2$ in the channel conductivity has been observed in the network-based transistor. Voltage pulses are used to control the transistor states; no continuous gate bias is needed. Furthermore, *n*-type behavior of the network channel is observed, which is attributed to a change in the Schottky barrier at the carbon nanotube-metal interface. © 2008 American Institute of Physics. [DOI: 10.1063/1.2975158]

Significant improvements in our understanding of single wall carbon nanotube field effect transistor (SWNT FET) have been achieved over the past decade.^{1–4} It is widely accepted that the Schottky barrier at the metal-SWNT interface affects the transistor characteristics significantly. Many applications in areas such as gas sensing, biomolecular detection, light emitting diode, and logic circuits have been studied. However, hysteresis in the transfer characteristics exists in majority of the reported devices and is problematic for achieving high performance logic devices. While this behavior has been suggested to serve for nonvolatile memory applications,⁵ operation of such a device is highly susceptible to environmental changes since the hysteresis is likely due to mobile charges trapped at the SWNT-dielectric (typically SiO₂) interface where a water layer exists in ambient environment.^{6,7} For practical applications, a proper control of the surface charges is necessary. Ferroelectric materials have spontaneous polarization inherent to their crystal structures. The polarization can be switched within a nanosecond by a voltage pulse.⁸ It can reach a value as high as 100 $\mu\text{C}/\text{cm}^2$ as compared to the surface charges of $\sim 2.4 \mu\text{C}/\text{cm}^2$ produced by SiO₂ under an electric field of 10 MV/cm (above which, the dielectric breaks down). It is thus interesting to study the effect of such large spontaneous polarizations on the performance of SWNT FET.

Replacing the SiO₂ in a conventional metal-oxide-semiconductor FET with ferroelectric materials has been studied since 1950s.^{9–12} However, the Pb-based ferroelectrics are not compatible with a traditional Si channel due to the diffusion of Pb and Ti into silicon and the formation of an intermediate silicate layer at the interface. These interface imperfections form high-density electron or hole traps, which seriously degrade device performance. To overcome these problems, alternative designs have been suggested and tested. For example, an insulating buffer layer can be introduced between the ferroelectric-gate and semiconductor channel, forming a so-called metal-ferroelectric-(metal)-insulator-semiconductor FET.¹³ All-perovskite FETs have also been studied by using perovskite oxides such as SrRu_xTi_{1-x}O₃, SrRuO₃, SrCuO₃, La_{1-x}Sr_xCuO₃,

LaNdSrMnO₃, and La_{1-x}Ca_xMnO₃ as channels.^{14–18} The on/off ratio of such devices is relatively low.

Here we report our study of a ferroelectric-gate transistor using SWNT network as the channel. The device structure is shown schematically in Fig. 1(a). A 400 nm ferroelectric film, Pb(Zr_{0.52}Ti_{0.48})O₃, is deposited on a commercial Pt coated Si substrate (Silicon Quest International) using sol-gel technique. The SWNTs (from Carbon Nanotechnologies, Inc.) treated with surfactants in an aqueous solution are drop casted on the ferroelectric film, followed by rinsing with de-ionized water and drying. An image of the network channel taken by using electrostatic force microscopy is shown in the inset of Fig. 1(a), uniform SWNT network is observed. The ferroelectric property of the Pb(Zr_{0.52}Ti_{0.48})O₃ layer is characterized from room temperature to 150 °C by using a commercial FE tester (Radiant Technology, Precision Premier). The remanent polarization is $\sim 20 \mu\text{C}/\text{cm}^2$, which does not change significantly at 150 °C [Fig. 1(b)].

Figure 2(a) shows the source-drain current as a function of gate bias. The gate voltage is applied to the bottom Pt layer while the source is grounded. Note that voltage pulses of 1 s are used instead of continuous bias. After every pulse, the transistor is left to relax for 10 s to allow any switching transients to die down before source-drain current (I_{ds}) is measured. The same procedure is adopted throughout this study; no continuous gate bias is used. A sharp transition between on/off states appears around the coercive field of the Pb(Zr_{0.52}Ti_{0.48})O₃ film. The on-state I_{ds} shows almost linear dependence on source-drain bias (V_{ds}), indicating low barri-

FIG. 1. (Color online) (a) Schematic illustration of the SWNT network-based transistor. Inset shows an EFM image of the SWNT network in one of the tested samples. (b) The ferroelectric hysteresis loops of the Pb(Zr_{0.52}Ti_{0.48})O₃ thin film measured at 27 and 150 °C.

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FIG. 2. (Color online) (a) I_{ds} vs V_{ds} curves at various gate voltages ranging from +15 V to -15 V. The gate bias is applied in 1 s pulse. The inset is a blow up the off-state I_{ds} - V_{ds} curve; (b) I_{ds} vs V_{gs} behavior at $V_{ds}=+2$ V. Again, the gate bias is applied for 1 s. I_{ds} is measured after the device is relaxed for 30 s.

ers at the metal-SWNT interfaces. On the other hand, rectifying behavior is observed in the off-state I_{ds} - V_{ds} characteristics [Fig. 2(a) inset], evidence of Schottky barriers at the interfaces. I_{ds} - V_{gs} plot for $V_{ds}=2$ V [Fig. 2(b)] shows a hysteresis loop, which resembles that of the ferroelectric polarization hysteresis in both the direction and coercive field value. The cause for the observed hysteresis is different from that for typical SWNT FET using SiO_2 or other nonferroelectric-gate dielectrics. In those cases, hysteresis is induced by surface charges injected into and trapped by the water layer at the SWNT-dielectric interface⁶ or by the silanol groups on SiO_2 surface.⁷ These trapped charges would induce an advancing hysteresis as reported in literature. We instead observe a retarding hysteresis, suggesting that it is due to ferroelectric polarization rather than injected charges.

Another interesting feature is that the channel shows *n*-type behavior where positive gate pulse leads to high channel conductivity. This is opposite to the usual *p*-type behavior of SWNT in ambient environment.^{19,20} (Similar devices prepared in our laboratory on SiO_2/Si substrate under the same condition do show *p*-type behavior, data not shown.) It is known that oxygen molecules attached to the SWNT surface act as acceptors and introduce holes into CNT.²¹ Surface contamination of the sol-gel derived film could also affect the device performance. To understand if the observed *n*-type characteristic is due to an unknown doping effect of the ferroelectric surface, we prepare a top gate on another network transistor using a nonferroelectric dielectric material, polymethyl methacrylate (PMMA). Tests with gate bias applied to the bottom Pt electrode show no change in the *n*-type characteristic of the channel before and after the PMMA deposition. A decrease in the channel conductivity is observed (data not shown), probably due to extra scattering centers introduced by the PMMA layer. However, the I_{ds} versus V'_{gs} measurement, where V'_{gs} is the continuous bias applied through the top gate, confirms that the SWNT is still *p*-type, as shown in Fig. 3. The observed *n*-type behavior is likely due to effects of ferroelectric polarization on the metal-SWNT interfaces.

We have measured the source-drain current at temperatures ranging from room temperature to 120 °C in ambient. The results are shown in Fig. 4(a) for the case where the ferroelectric layer is polarized upward toward the channel; and in Fig. 4(b) for the opposite case. At every temperature, a pulse of 15 or -15 V is applied to the bottom Pt electrode for 1 s. The system is then made to relax for 30 s before the I_{ds} is measured. The results are analyzed using the following

FIG. 3. (Color online) I_{ds} - V'_{gs} and I_{gs} - V'_{gs} curves with continuous gate bias applied to the top gate.

equation for current through a Schottky barrier:²²

$$J = A * T^2 \exp\left(-\frac{E_a}{k_B T}\right) \exp\left[\frac{e}{k_B T} \left(\frac{eE}{4\pi\epsilon}\right)^{1/2}\right],$$

where A^* is the effective Richardson constant, T is the temperature, E_a is the Schottky barrier height, k_B is the Boltzmann constant, and E is the electric field across the barrier. Through linear fitting of the $\ln(I_{ds}/T^2)$ versus $1/T$ plots, the barrier heights at different V_{ds} can be obtained. The results are summarized in Fig. 4(c). A barrier height of ~300 meV is obtained for the low current off state at $V_{ds}=0$ V. For the on state, the barrier is negligible. It has been reported that heating causes oxygen desorption from CNT surface. Moisture has also been suggested to affect the conduction of SWNT FET when studied in ambient.²³⁻²⁵ Nevertheless, the effect of ferroelectric polarization switching is evident and the difference in the measured activation energies between the two states is more than 300 meV, suggesting a strong modification in the metal-SWNT interface. The details of this modification are not understood yet. One possibility is that when a pulse of +15 V/-15 V is applied between the gate and source electrodes, ferroelectric dipoles are switched with positive/negative gate appear on the top surface. The

FIG. 4. (Color online) $\ln(I_{ds}/T^2)$ vs $1/T$ plots at various V_{ds} for (a) on-state (polarization pulled upward toward the channel); and (b) off state (polarization pulled downward). (c) Barrier heights obtained from the slopes of the $\ln(I_{ds}/T^2)$ vs $1/T$ plots. E_a of ~0 and ~300 meV are obtained for the on and off states.

ferroelectric film underneath the SWNTs in the channel area may also be switched but the nanosize domain (limited by the SWNT diameter) may not be stable and relaxes immediately. The surface charges at the Pt–Pb(Zr_{0.52}Ti_{0.48})O₃ interface effectively decreases/increases the electrode potential. When the electrode Fermi level moves into the energy gap of SWNT, a barrier appears for hole transport and the transistor is turned off. Further study is underway.

In conclusion, we have studied a ferroelectric-gate SWNT network transistor. The Schottky barrier height at the Pt-SWNT interface is affected by the ferroelectric polarization, leading to modulation of the channel conductivity. We cannot rule out effects from other sources, such as dielectric surface contamination, at the moment. However, the unique switching characteristics observed in this study may provide another strategy for making *n*-type SWNT transistors without using low work function metals.

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