A 4.06 mW 10-bit 150 MS/s SAR ADC with 1.5-bit/cycle Operation for Medical Imaging Applications

Sharma Sunny, *Student Member, IEEE*, Yong Chen, *Member, IEEE*, and Chirn Chye Boon, *Senior Member, IEEE*

***Abstract*—This paper reports a 10-bit 150 MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with binary-scaled redundancy-facilitated error correction technique. The proposed 1.5-bit/cycle technique with built-in capacitive digital-to-analog converter (CDAC) redundancy, corrects multiple erroneous decisions in a total of nine conversion cycles. The proposed binary-scaled redundancy provides a 12.5% error tolerance range for the incomplete CDAC voltage settling. The digital error-correction logic circuit presented uses a bit-overlap-and-add technique. The prototype chip was fabricated in 65-nm CMOS technology and occupies chip area of 0.038 mm^2. It consumes 4.06 mW from a 1.2 V supply, achieving the Nyquist signal-to-noise-and-distortion ratio (SNDR) of 57.81 dB and the effective number of bits of 9.31-bit at an operating frequency of 150 MS/s, corresponding to the figure-of-merit of 42.6 fJ/ conversion-step.**

***Index Terms*— 1.5-bit/cycle, ADC, capacitive digital-to-analog converter (CDAC), CMOS, error correction, low power, medical imaging, redundancy, SAR, successive approximation register.**

I. Introduction

Increasing demand for portable, low-cost medical imaging systems, such as X-rays, computed tomography scan, ultra-sound [1], positron emission tomography [2] and wireless capsule endoscopy, has resulted in integrated multifunction system on chip (SoC), generally consisting of analog, digital, and radio-frequency circuits. This development places stringent requirements on power dissipation, chip area, and performance of key subsystem such as analog-to-digital converter (ADC), operating in the signal acquisition chain under a noisy SoC environment with a typical resolution between 9 and 12-bit and speeds exceeding 100 MS/s.

The successive approximation register (SAR) ADC topology has seen several advances in digital-to-analog converter (DAC) switching schemes [3–6], high-speed dynamic latch comparator [7], asynchronous-timing logic [2, 7, 8], SAR logic and redundancy techniques [7–21] that further improves the single-channel speed while achieving low figure-of-merit (FOM) [22]. For high-speed operation, the capacitive DAC (CDAC) becomes a significant speed bottleneck, affecting

Manuscript received March 10, 2018; revised April 6, 2018; accepted xxxxx xx, 2018. Date of publication xxxxxx xx, 2018; date of current version xxxxxx xx, 2018. This work was supported by the National Research Foundation, Prime Minister's Office, Singapore under its Campus for Research Excellence and Technological Enterprise (CREATE) program.

S. Sharma and C. C. Boon are with VIRTUS, School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798 (e-mail: sunny004@e.ntu.edu.sg).

Y. Chen is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: ychen@umac.mo).

Digital Objective Identifier XXXXXXXXX.

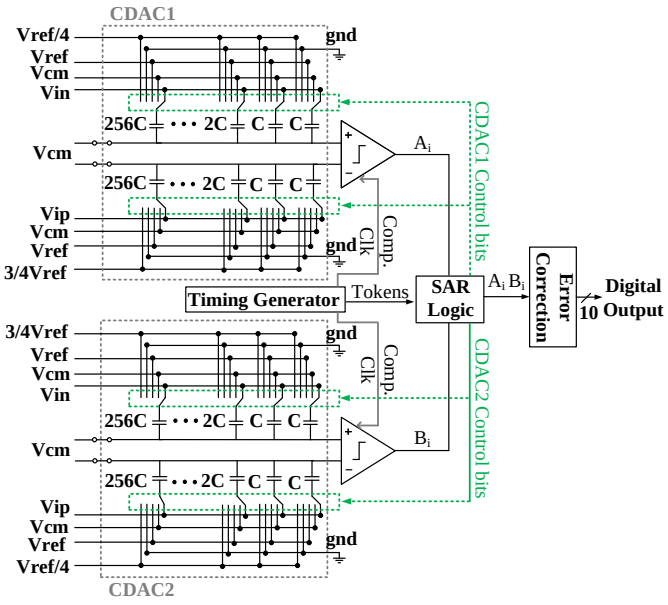


Fig. 1. Top-level architecture of the proposed 1.5-bit/cycle SAR ADC.

voltage settling behavior, which may result in the erroneous conversion. A 2-bit/cycle technique for SAR ADCs is widely used [2, 14, 21] to achieve high sampling frequency. The 2-bit/cycle technique reported in [21] suffers from degraded dynamic performance, which may be partly due to the non-linearity of the top-plate sampling switch and the input signal coupling to the top-plate of the CDAC. A bootstrap switch circuit architecture is proposed in [23] that increases the top-plate sampling precision above 12-bits. Introducing redundancy and error-correction capabilities is beneficial to preserve the dynamic performance of the data converter. Several binary [9, 10] and non-binary [12, 14] redundancy techniques have been introduced to relax the CDAC voltage settling time and facilitate error correction. However, these techniques have limitations such as decrease in conversion speed due to the additional multiplexer (MUX) delay [10] or arithmetic unit [12] in the control logic path, decrease in bandwidth due to the additional compensation capacitors used in the CDAC [9], and large error-correction logic [9, 12] required to convert the output of additional redundancy-induced conversion cycles.

This paper presents a 10-bit 150-MS/s SAR ADC employing an unmodified binary-scaled CDAC with in-built redundancy to implement an initial 1-bit followed by eight cycles of 1.5-bit/cycle conversion. The redundancy-facilitated error- correction technique can correct multiple erroneous decisions without requiring any additional conversion cycle. The proposed 1.5-bit/cycle architecture reduces CDAC size, relaxes CDAC

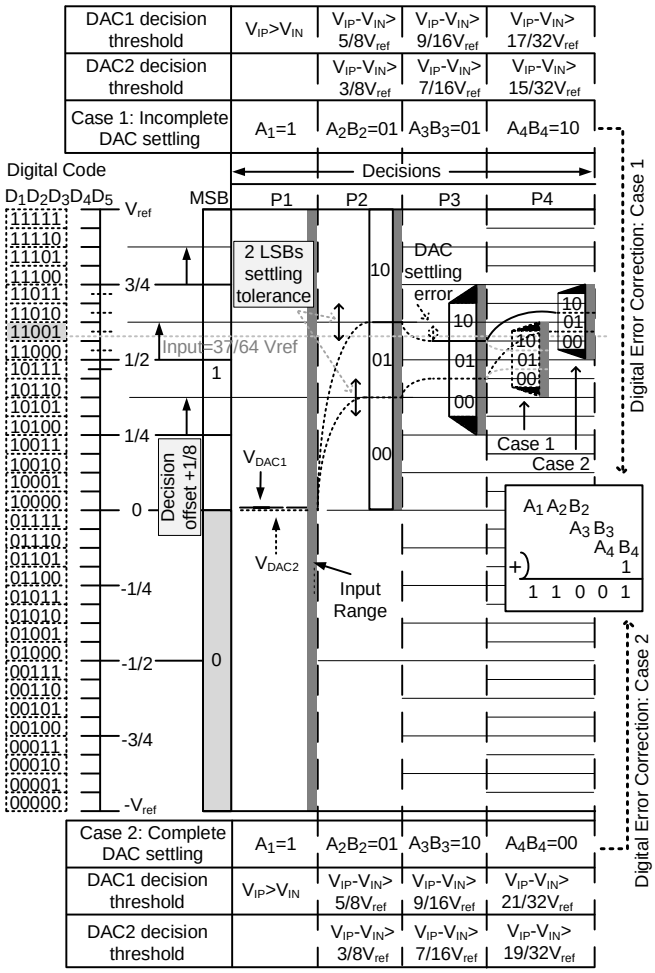


Fig. 2. Example of 5-bit SAR ADC using the proposed 1.5-bit/cycle technique.

voltage settling process, simplifies error- correction logic, and maintains constant common-mode CDAC operation.

This paper is organized as follows. Section II introduces the overall ADC architecture. Section III details the proposed techniques and design of the key sub-blocks in the proposed ADC with the circuits design considerations, followed by measurement results in Section IV. Finally, Section V concludes the work.

II. Overall ADC Architecture

The top-level architecture of the proposed ADC is shown in Fig. 1. The 1.5-bit conversion requires two CDACs to generate the two comparator thresholds. The input signal is sampled on the bottom plate of the binary-scaled CDAC in order to prevent transistor charge injection and input signal coupling to the top plate, which is connected to the input of the comparator. An event-based asynchronous-timing generator is used to generate the high-frequency (9×150 MHz) clock signals for the comparator, which enable an off-chip-generated 150 MHz clock signal to initiate the ADC operation. After comparator regeneration, the ready signals of the two comparators flag an event, which is then used to generate the comparator clocks for the subsequent conversion cycles. An extra transistor input pair is used to calibrate the input offset of the comparator. The thermometer coded comparators' outputs along with the control logic drives the CDAC transistor switches. The SAR logic employs a 3-bit counter to keep track of the conversion cycles. Irrespective of the comparators output, the SAR logic reuses the counter generated signal to drive the CDAC switches for generating the redundancy margin. The dynamic control logic is implemented to increase its speed. Thermometer-to-binary conversion occurs for the comparators' outputs from the 1.5-bit/cycle operation before these outputs are stored in the memory for digital error-correction operation.

III. Proposed Techniques & Design of the Key Sub-Blocks

A. Proposed 1.5-bit/cycle technique

Redundancy can be used to relax certain circuit nonlinearities, such as different comparator offsets for the 1-bit per conversion-cycle SAR ADC using two comparators to reduce the power consumption [17]. A tradeoff exists between selecting the redundancy margin and the penalty in terms of additional conversion cycles. Redundancy, expressed in either percentage or number of LSBs, relaxes the time available for the CDAC voltage to settle by a predetermined margin of error. The following equation can be used to calculate the time required for an N-bit CDAC voltage to settle within a precision of ½ of the LSB:

$$T = \tau \cdot \ln(\delta \cdot \frac{1}{2^N}) \qquad (1)$$

where τ is the time constant, T is the total DAC settling time, δ is the voltage settling precision in LSBs and 2^N is the conversion cycle input range in LSBs.

Similar to the work reported in [7], there is no redundancy used in the MSB decision cycle because the input voltage and transient CDAC reference voltage has settled to the required ½LSB before the conversion starts. Cycles 2–9 implement binary redundancy using an unmodified binary-scaled CDAC. The proposed 1.5-bit/cycle technique provides a 12.5% redundancy or error tolerance margin, which permits correction of multiple erroneous decisions without using any additional conversion cycles. Using (1), a 10-bit SAR ADC using 1-bit/cycle non-redundancy conversion will need 45.05τ (excluding sampling time) to complete ten cycles. Whereas, the proposed technique only requires 29.11τ (excluding sampling time) to complete the required nine cycles. Thus, the proposed 1.5-bit/cycle technique exhibits a speed advantage of 35.38%.

Fig. 2 gives an example of a 5-bit SAR ADC operation using the proposed 1.5-bit/cycle technique. A differential full scale is used. The binary-coded decision regions are 0, 1 for the initial 1-bit cycle (P1) and 00, 01, 10 for the 1.5-bit cycles (P2–P4). The input range is denoted by a grey bar and the black triangles denote the extra input range available for the decision regions 00 and 10. In this example, after P1, the upper decision region is divided in four regions which are then offset by 1/8Vref in order to obtain the two decision thresholds (3/8Vref, and 5/8 Vref) for 1.5-bit/cycle operation. The CDACs are switched appropriately to generate voltages V_{DAC1} and V_{DAC2}, which

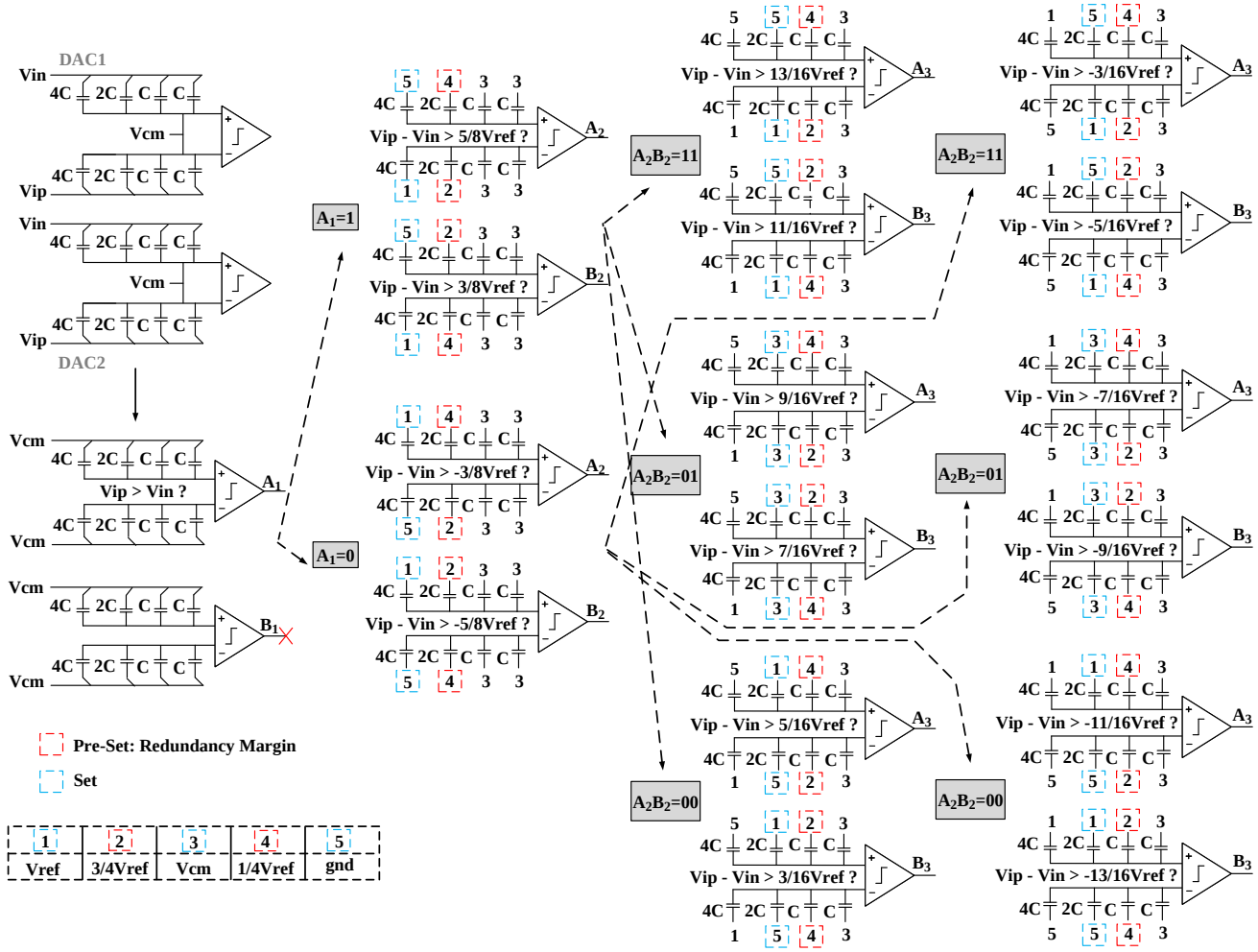


Fig. 3. Proposed 1.5-bit/cycle CDAC switching procedures for a 4-bit SAR ADC.

represent these two decision thresholds. The offset for generating the two decision thresholds is scaled by two, cycle by cycle from P2. The usefulness of the proposed technique is clearly shown for an incomplete CDAC voltage settling in P3, which is corrected in P4. A single analog input value can be represented by different digital codes, enabling different CDAC switching procedures and providing a chance for the error to propagate to the next conversion cycle where it can be corrected. The final digital output ($D_1D_2D_3D_4D_5$) remains the same if there is an error in P2. A "bit overlap and add" error-correction technique, which is similar to the 1.5-bit/stage pipeline ADC topology is used.

B. Proposed CDAC switching for 1.5-bit/cycle conversion

Fig. 3 shows the proposed differential switching procedures for a 4-bit SAR ADC employing the proposed 1.5-bit/cycle technique in Section II-A. The switching scheme uses an unmodified binary-scaled CDAC and maintains a constant common-mode operation. Each conversion cycle follows the sequence of switching the CDAC according to the output of the previous conversion cycle, waiting for the CDAC reference voltage to settle within the redundancy range and then waiting for the regeneration of the comparator. Depending on the decision region, the charge-redistribution-based switching scheme switches the appropriate capacitor within the CDAC to one of three reference voltages, such as common-mode voltage (Vcm; 0.6 V), positive reference voltage (Vref; 1.2 V), or negative reference voltage (gnd; 0 V), through the SAR control logic. The required offset to the decision region is generated by switching the appropriate capacitor to either 1/4Vref or 3/4Vref reference voltages, which in-turn creates the 12.5% redundancy margin.

The accuracy of the reference voltages 1/4Vref and 3/4Vref, together with the CDAC voltage settling time, would determine the effective redundancy margin. Ten-bit accuracy and sufficient CDAC voltage settling time result in a full 12.5% redundancy margin. The capacitors responsible for the redundancy margin are pre-set (based on token signals generated after the comparator finishes regeneration), and are pre-determinedly switched to the appropriate reference voltages. This pre-set technique allows sufficient CDAC settling time in order to create the redundancy margin in advance. Therefore, this approach allows the CDAC settling time for the capacitors "set" to reference voltages Vref, Vcm, and gnd to be relaxed within the created redundancy margin.

The two thresholds generated for the proposed 1.5-bit/cycle technique are independent of each other's CDAC switching pattern. Irrespective of erroneous decisions, the switching scheme enables the CDAC-generated comparator thresholds to converge to the normalized analog input voltage at the end of

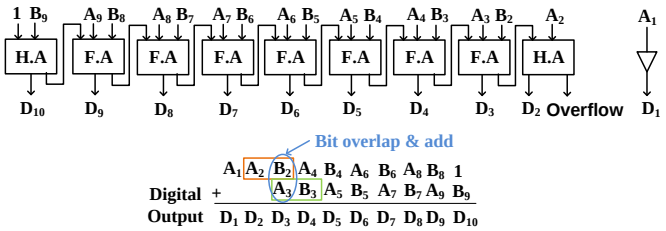


Fig. 4. Error-correction logic and its implementation.

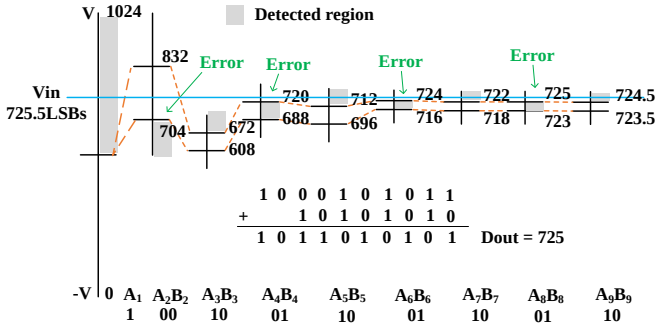


Fig. 5. Example of the proposed error-correction technique for a 10-bit ADC.

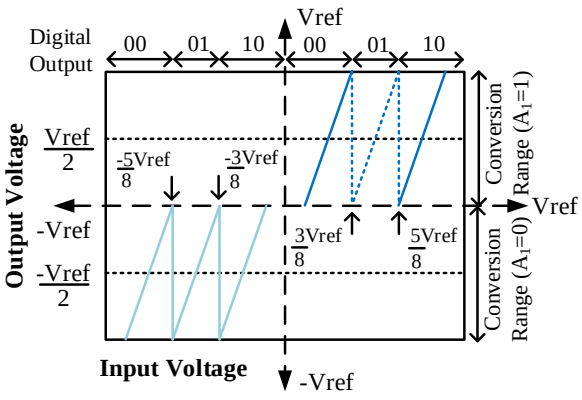


Fig. 6. 1.5-bit/cycle transfer function of the second conversion cycle.

the ninth cycle for a 10-bit SAR ADC. A mismatch between the capacitor ratios leads to a small variation in the CDAC-generated comparator threshold. We assume that up to a quarter of the redundancy margin (i.e., 3.125%) is used because of post-fabrication capacitor mismatch. Several layout techniques, such as symmetric layout for CDAC, reference-voltage routing and common-centroid CDAC with dummy capacitors, help to minimize the mismatch between the two CDACs.

C. Error correction

The proposed 1.5-bit/cycle technique shows multiple error-correction capabilities. As long as the CDAC voltage settling error is within the redundancy range, any erroneous decision can be corrected in the subsequent conversion cycle. The effective error tolerance range remains constant and does not depend on where the erroneous conversion cycle occurs. An error in the last conversion cycle will result in a degradation of the signal-to-noise ratio because there is no subsequent conversion cycle to correct it.

Fig. 4 shows the proposed digital error-correction logic implemented by a ripple carry adder circuit comprising seven full adders and two half adders. Theoretically, an overflow from the half adder, adding bit A_2 and carry from the previous full adder, should not occur. However, to indicate any abnormal SAR operation post-fabrication that may lead to an overflow, the overflow pin is routed to an output pad. The logic analyzer detected no overflow during measurements of the test chip.

Fig. 5 illustrates an example of a normalized analog input voltage of 725.5LSBs with four errors made during conversion cycles 2, 4, 6, and 8 that are corrected in a total of nine conversion cycles. Not every analog input voltage conversion would have four erroneous decisions. Irrespective of the number of errors or in which conversion cycle the errors occur, the proposed switching scheme appropriately switches the two CDACs such that the two comparator thresholds can converge to a precision of ½LSB of the input analog voltage.

Fig. 6 shows the 1.5-bit/cycle transfer function of the second conversion cycle. The two decision thresholds for 1.5-bit output are obtained by adding 1/8Vref offset to the three decision thresholds for a 2-bit output and neglecting the last (third) decision threshold. The absence of decision thresholds at 1/8Vref and 7/8Vref results in the digital outputs '00' and '10' covering larger input voltage range than that of digital output '01'. Since, the proposed design does not have a residue amplifier (available in 1.5-bit/stage pipeline ADCs), the transfer function for each cycle changes and depends on all the previous cycles' decisions. A_1 is the output of the 1st cycle.

D. Capacitive DAC

A 0.74-fF unit capacitor is obtained by sandwiching metal5 between metal4 and metal6 layers. The unit capacitor occupies an area of 1.38×1.74 μm^2. A total of 512 unit capacitors are laid out using a common-centroid layout technique and dummy unit capacitors are placed on all sides of CDAC. The following equation [24] provides a lower bound for a mismatch-limited unit capacitor based on foundry parameters for a maximum differential nonlinearity (DNL) of 1/3LSB for a differential CDAC

$$C_U = 9 \cdot 2^{N-1} \cdot K_\sigma^2 \cdot K_c \qquad (2)$$

where, K_c is the capacitor-density parameter, K_σ is the matching coefficient, and N is the CDAC resolution. These parameters take the values K_σ = 0.86% μm and K_c = 2 fF/μm^2 for the 65-nm CMOS technology.

The proposed switching scheme maintains a constant CDAC common mode voltage, which allows a fixed parasitic capacitance on the CDAC top plate. The fixed parasitic capacitance results in a fixed gain error and does not affect the dynamic performance of the ADC [25, 26].

E. Control logic

Fig. 7 shows the control logic for the 1.5-bit/cycle implementation. The initial 1-bit conversion uses a similar control logic where only one comparator output is utilized and the pre-set CDAC reference-voltage-switches are absent. The

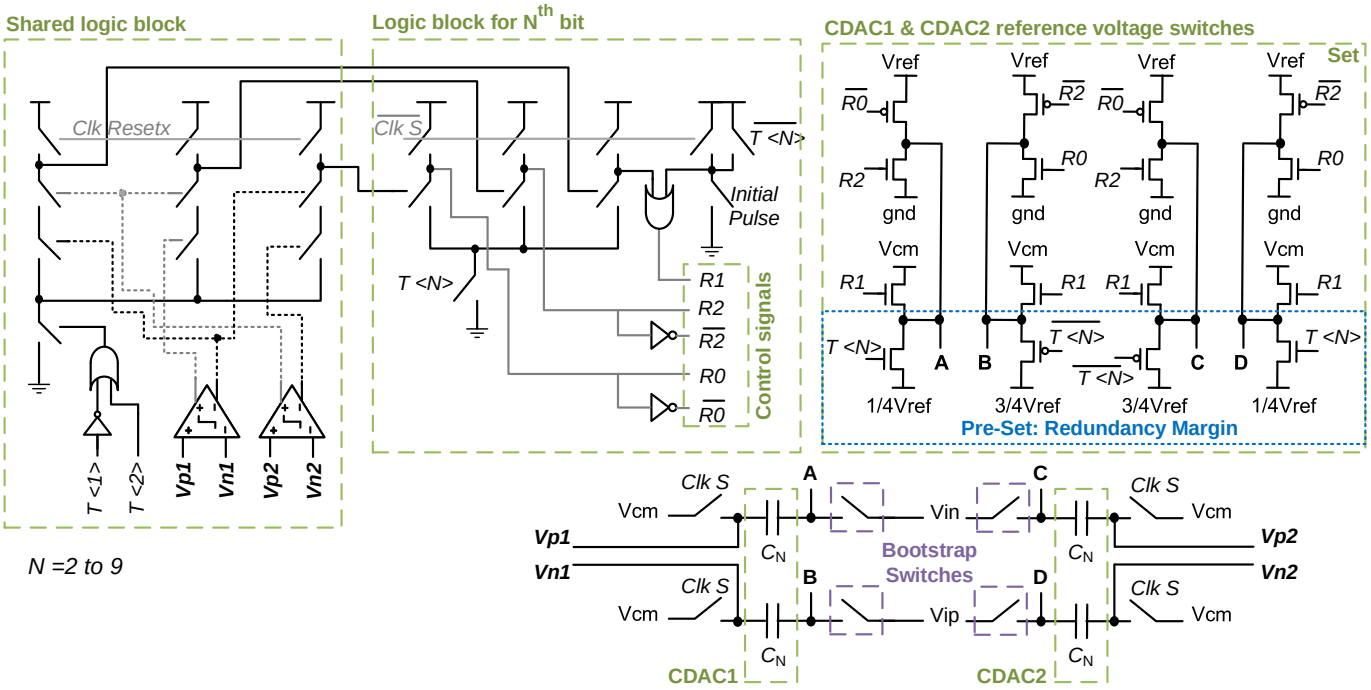


Fig. 7. SAR control logic for implementation of the 1.5-bit/cycle technique.

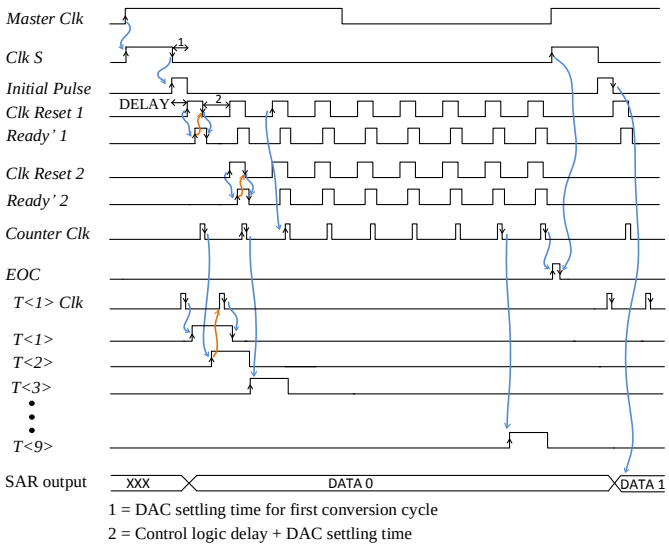


Fig. 8. Event-based asynchronous-timing diagram.

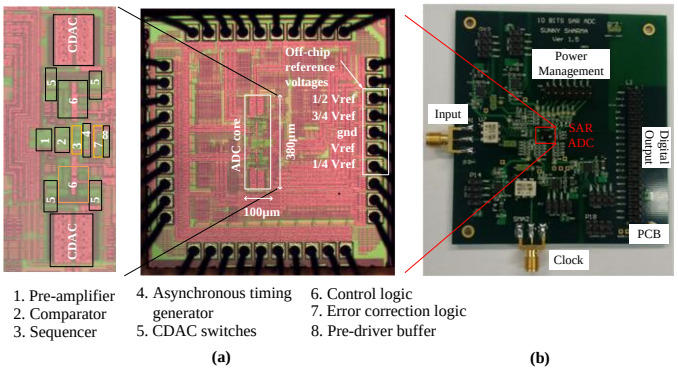


Fig. 9. (a) Die micrograph and its details. (b) Testing PCB.

token signal based-dynamic logic implementation of control logic serves to lower the control-logic delay and reduce static-current consumption. Fig. 8 shows the asynchronous timing diagram, where the arrows show the corresponding signal trigger based on the rising- or falling-edge signal. Here, signal *Master Clk* is the off-chip 150MHz clock signal, *Clk S* is the ADC sampling clock, *Initial Pulse* is used for control logic operation, and *EOC* is the end of conversion signal. *Clk Reset 1/2* and *Ready' 1/2* are the dynamic comparators clock and regeneration completion signal. A 3-bit counter implemented using master-slave latches that generate the token signals *T<N>*, where N is the conversion cycle number. The memory to store the comparator output is implemented using a differential topology modified from Ref. [27]. At the end of the conversion signal *EOC*, the memory values are temporarily stored in D flip-flops for error correction, and the memory is reset for the next cycle.

Generally, the SAR control logic affects attainable speed, power consumption, and chip area. The switching scheme determines complexity of the control logic, CDAC size, number of switches and switching energy. In the proposed 1.5-bit/cycle switching procedure, two additional reference voltages appear (i.e., 1/4Vref and 3/4Vref), which are used solely to generate the redundancy margin. It is possible to implement a three-reference-voltage system based on Vcm, Vref, and gnd with the same functionality. Such a system could reduce the number of CDAC switches from 88 to 80 for a single ended implementation. However, to maintain the built-in CDAC redundancy for a three-reference-voltage design and guarantee no shift to the CDAC common mode voltage, the CDAC resolution increases by 1-bit (a 100% increase in CDAC size), which would increase the chip area significantly. The proposed architecture corrects multiple errors without requiring any additional conversion cycle and also simplifying the error-correction logic. Yet, the 1.5-bit/cycle technique and error-correction capability comes at a cost of having two CDACs, two comparators, and twice the number of CDAC

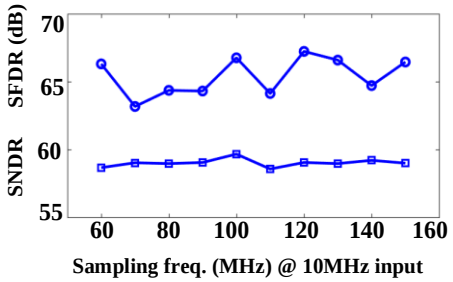


Fig. 10. Measured SNDR and SFDR versus sampling frequency.

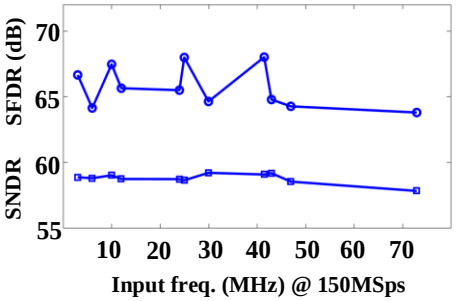


Fig. 11. Measured SNDR and SFDR versus input frequency.

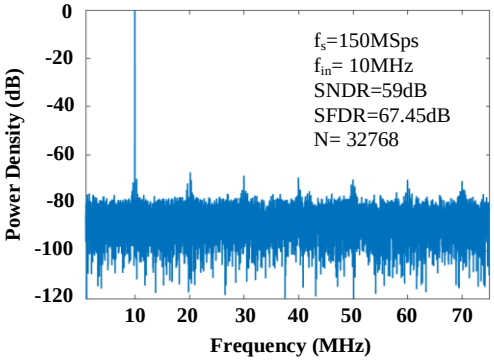


Fig. 12. Measured FFT results with 10 MHz input at 150 MS/s.

Fig. 13. Measured INL.

Fig. 14. Measured DNL.

switches. The area penalty for having two CDACs is mitigated by the proposed CDAC switching procedure because of the 50% reduction in CDAC size when compared to a conventional CDAC [28]. If extra CDAC switches are involved, then, similar to Ref. [12], the additional CDAC switches could be laid out underneath the CDAC with a shielding metal layer.

TABLE I.
PERFORMANCE SUMMARY AND COMPARISON.

Parameters	This Work	[21]	[23]	[29]	[30]
Architecture	1.5-bit/cycle SAR	2-bit/cycle SAR	1-bit/cycle SAR	1-bit/cycle SAR	Pipeline-SAR
CMOS (nm)	65	40	180	65	40
Supply (V)	1.2	1.2	1.8	1.2	1.1
Resolution / # Cycles	10 bit / 9	10 bit / 8	10 bit / 10	10 bit / 11	12 bit / 12
Redundancy	Bin. 12.5%	1-bit Bin.	No	Non-Bin. 1-bit	Non-Bin.
Digital Error-Correction	7 F. A, 2 H. A	Yes	No	8 F. A	N/A
Sampling (MS/s)	150	300	80	150	160
ENOB (bit)	9.31	7.51	9.13	8.2	10.85
Power (mW)	4.06	2.1	2.61	1.4	4.96
FOM (fJ/conv-step)	42.6	38.4	74.4	31.8	20.6
Area (mm^2)	0.038	0.008	1.61	0.079	0.042
$V_{in,pp,diff}$ (V)	2.4	N/A	1.6	2.1	2

IV. MEASUREMENT RESULTS

The prototype of the proposed ADC was fabricated in a 65-nm 1P9M CMOS technology. The die photo and its details are given in Fig. 9(a), in which the ADC core occupies an active area of 0.038 mm^2 including clock buffers, and a pre-driver buffer. Particularly, the digital error-correction circuit and the asynchronous-timing block merely occupy 38×7 μm^2 and 47×14 μm^2, respectively. Fig. 9(b) shows the testing printed circuit board (PCB) used for chip measurements. The off-chip calibration using a 12-bit DAC is conducted to solve the comparator-offset mismatch through an additional input pairs in the comparators. The step size (LSB) of the off-chip calibration DAC is ¼LSB of the ADC under test. The small step size enables the comparator offset mismatch to be much less than ½LSB and does not degrade the dynamic performance. The performance was measured at 1.2 V power supply and the ADC consumes 4.06 mW at 150 MS/s, leading to a FOM of 42.6 fJ/conversion-step at the Nyquist frequency. The total power is divided among the blocks, such as CDAC reference voltage, comparators (including analog pre-amplifiers), asynchronous clock generator (excluding clock buffer to correct signal amplitude), and digital domain as 0.29, 1.23, 0.3, and 2.24 mW, respectively.

Figs. 10 and 11 plot the signal-to-noise-and-distortion ratio (SNDR) and the spurious free dynamic range (SFDR) versus sampling frequency for an input frequency of 10 MHz and an input frequency at 150 MS/s, respectively. Fig. 12 shows the output FFT spectrum for a 10 MHz input frequency with a measured SNDR of 59 dB and an SFDR of 67.45 dB. For an input close to the Nyquist frequency of 73.03 MHz, an SNDR

of 57.81 dB and an SFDR of 64.78 dB are measured resulting in an effective number of bits (ENOB) of 9.31-bit. The off-chip center-tap balun used at the input causes a frequency dependent phase and amplitude imbalance in the input differential signals. Together with the phase imbalance due to the mismatch in the on-chip input signal path to the two CDACs, the even-order harmonics are noticeable in the FFT plot. Additionally, the frequency dependent imbalances of the off-chip balun results in variations in the SFDR (Fig. 11).

Figs. 13 and 14 show the measured static performance with a peak integral nonlinearity (INL) of +0.96/−0.86LSB and a peak DNL of +0.97/−0.83LSB, respectively.

Table 1 summarizes the performance of the proposed ADC and compares it with published SAR ADCs [21, 23, 29, 30]. Advantages of our proposed ADC include no additional conversion cycles, simple error-correction logic, and CDAC simplicity maintained by using unmodified binary-scaled architecture. The pipeline-SAR ADC [30] uses a high-resolution first stage to relax the linearity and noise requirement of the residue amplifier. Additionally, it uses a sub-binary DAC in the first SAR stage, which helps it attain high conversion speed and reduce the power consumption. Although the work [21] achieves higher sampling speed, the ENOB is less. The SAR ADC [29] uses redundancy in the first five decision bits and requires one additional conversion cycle to achieve same sampling frequency as this work.

V. Conclusion

This paper presents a 10-bit, 150 MS/s SAR ADC with the proposed binary-scaled redundancy-facilitated error correction technique. The proposed CDAC switching procedure for 1.5-bit/cycle technique maintains a constant common mode operation while reducing the total CDAC size. The built-in CDAC redundancy margin of 12.5% relaxes the CDAC settling time, which increases the conversion-cycle frequency. Multiple erroneous decisions can be corrected without requiring additional conversion cycle. The digital error-correction uses a bit-overlap-and-add technique consisting of seven full adders and two half adders. The measured static performance is achieved with a peak INL of +0.96/−0.86LSB and a peak DNL of +0.97/−0.83LSB. For an input close to Nyquist frequency, a SNDR of 57.81 dB and an SFDR of 64.78 dB are measured, resulting in 9.31-bit ENOB, when supplying a 1.2 V with a power consumption of 4.06 mW.

ACKNOWLEDGEMENT

The authors would like to thank Associate Professor Siek Liter, Arya Balachandran, and Dr. Pilsoon Choi for technical discussions.

References

[1] T. C. Chen, and T. H. Tsai, "CMOS ultrasound receiver with on-chip analog-to-digital front end for high-resolution ultrasound imaging Systems," *IEEE Sensors Journal*, vol. 16, no. 20, pp. 7454–7463, Dec. 2016.

[2] L. Qiu, K. Wang, K. Tang, L. Siek, and Y. Zheng, "A 10-bit 300MS/s 5.8mW SAR ADC with two-stage interpolation for PET imaging," *IEEE Sensors Journal*, vol. 18, no. 5, pp. 2006–2014, Mar. 2018.

[3] J. H. Tsai, H. H. Wang, Y. C. Yen, C. M. Lai, Y. J. Chen, P. C. Huang, P. H. Hsieh, H. Chen, and C. C. Lee, "A 0.003 mm^2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.

[4] Y. Zhu, C.H. Chan, U. F. Chio, S. W. Sin, S. Pan U, R. P. Martins, and F. Maloberti, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[5] Y. H. Chung, M. H. Wu, and H. S. Li, "A 12-bit 8.47-fJ/conversion-step capacitor-swapping SAR ADC in 110-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 10–18, Jan. 2015.

[6] E. Rahimi and M. Yavari, "Energy-efficient high-accuracy switching method for SAR ADCs," *Electronics Letters*, vol. 50, no. 7, pp. 499–501, Mar. 2014.

[7] L. Kull, T. Toifl, M. Schmatz,P.A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 3.1mW 8b 1.2GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32nm digital SOI CMOS," *in ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 468–469.

[8] H. K. Hong, H. W. Kang, D. S. Jo, D. S. Lee, Y. S You, Y. H. Lee, H. J. Park, and S. T. Ryu, "A 2.6b/cycle-architecture-based 10b 1.7GS/s 15.4mW 4×-time-interleaved SAR ADC with a multistep hardware-retirement technique," *in ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[9] C. C. Liu, S. J. Chang, G. Y. Huang, Y. Z. Lin, C. M. Huang, C. H. Huang, and C. C. Tsai, "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," *in ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386–388.

[10] S. H. Cho, C. K. Lee, J. K. Kwon, and S. T. Ryu, "A 550μW 10-b 40-MS/s SAR ADC with multistep addition-only digital error correction," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1881–1892, Aug. 2011.

[11] M. Ding, P. Harpe, Y. H. Liu, B. Busze, K. Philips, and H. de Groot, "A 5.5fJ/conv-step 6.4MS/s 13b SAR ADC utilizing a redundancy-facilitated background error-detection-and-correction scheme," *in ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 460–461.

[12] F. Kuttner, "A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13μm CMOS," *in ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 176–177.

[13] Z. Boyacigiller, B. Weir, and P. Bradshaw, "An error-correcting 14b/20 μs CMOS A/D converter," in ISSCC Dig. Tech. Papers, Feb. 1981, pp. 62–63.

[14] H. K. Hong, W. Kim, S. J. Park, M. Choi, H. J. Park, and S. T. Ryu, "A 7b 1GS/s 7.2mW nonbinary 2b/cycle SAR ADC with register-to-DAC direct control," *in Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2012, pp. 1–4.

[15] K. L. Chan, A. A. Lee, X. Yuan, K. R. Krishna, and M. Je, "A 8.9-ENOB 2.5-uW 150-KS/s non-binary redundant successive approximate-on ADC in 0.18-μm CMOS for bio-implanted devices," *in IEEE Int. Conf. Engineering in Medicine and Biology Society (EMBC)*, Aug. 2010, pp. 650–653.

[16] T. Okazaki, D. Kanemoto, P. Ramesh, K. Yoshida, and H. Kanaya, "A design technique for a high-speed SAR ADC using non-binary search algorithm and redundancy," *in Proc. IEEE Asia-Pacific Microwave Conference (APMC)*, Nov. 2013, pp.506–508.

[17] T. Ogawa, T. Matsuura, H. Kobayashi, N. Takai, M. Hotta, H. San, A. Abe, K. Yagi, and T. Mori, "Non-binary SAR ADC with digital error correction for low power applications," *in Proc. IEEE Asia Pacific Conf. Circuits and Systems (APCCAS)*, Dec. 2010, pp.196–199.

[18] T. Ogawa, H. Kobayashi, M. Hotta, Y. Takahashi, H. San, and N. Takai, "SAR ADC algorithm with redundancy," *in Proc. IEEE Asia Pacific Conf. Circuits and Systems (APCCAS)*, Nov. 2008, pp. 268–271.

[19] T. Ogawa, H. Kobayashi, Y. Tan, S. Ito, S. Uemori, N. Takai, K. Niitsu, T. J. Yamaguchi, T. Matsuura, and N. Ishikawa, "SAR ADC that is configurable to optimize yield," *in Proc. IEEE Asia Pacific Conf. Circuits and Systems (APCCAS)*, Dec. 2010, pp. 374–377.

[20] R. Vitek, E. Gordon, S. Maerkovich, and A. Beidas, "A 0.015mm^2 63fJ/ conversion-step 10-bit 220MS/s SAR ADC with 1.5b/step redundancy and digital metastability correction," *in Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2012, pp. 1–4.

[21] J. Song, X. Tang, and N. Sun, "A 10-b 2b/cycle 300MS/s SAR ADC with a single differential DAC in 40nm CMOS," *in Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2017, pp. 1–4.

[22] B. Murmann, "ADC performance survey 1997-2017," [Online]. Available:http://web.stanford.edu/~murmann/adcsurvey.html.

[23] Y. Shen, Z. Zhu, S. Liu, and Y. Yang, "A reconfigurable 10-to-12-b 80-to-20-MS/s bandwidth scalable SAR ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 51–60, Jan. 2018.
[24] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13μm CMOS for medical implant devices," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.
[25] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "10-bit 30-MS/s SAR ADC using a switchback switching method," *IEEE Transactions Very Large Scale Integrated Systems (TVLSI)*, vol. 21, no. 3, pp. 584–588, Mar. 2013.
[26] J. Wang, S. Liu, Y. Shen, and Z. Zhu, "Low-power single-ended SAR ADC using symmetrical DAC switching for image sensors with passive CDS and PGA technique ," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Jan. 2018, doi: 10.1109/TCSI.2018.2794465.
[27] V. Tripathi, and B. Murmann, "An 8-bit 450-MS/s single-bit/cycle SAR ADC in 65-nm CMOS," *in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2013, pp. 117–120.
[28] B. P. Ginsburg, and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *in IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 2005, pp. 184–187.
[29] D. Li, Z. Zhu, R. Ding, and Y. Yang, "A 1.4-mW 10-bit 150-MS/s SAR ADC with nonbinary split capacitive DAC in 65nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Sep. 2017, doi: 10.1109/TCSII.2017.2756036.
[30] Y. Zhou, B. Xu, and Y. Chiu, "A 12-bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 920–931, Apr. 2015.

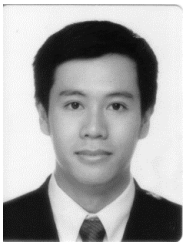
Sharma Sunny (S'13) received the B.Eng in electronics and communication engineering in 2012 from College of Engineering, Anna University, India. He attended University of Illinois, Urbana Champaign during his undergraduate studies in 2009. He received his MSc in Integrated Circuit Design in 2014 from Technical University of Munich and Nanyang Technological University (NTU), Singapore. He is currently working on his PhD in Electrical Engineering at NTU, Singapore under the Singapore-MIT Alliance for Research and Technology (SMART).

In 2012, he won second place at the Texas Instruments India analog design contest. In 2013, he was an intern at Infineon Technologies, Singapore in the analog and mixed signal department where he developed and patented a high-speed error-correcting SAR ADC. His research interests include low power analog, and mixed-signal circuit design and biomedical sensor circuits.

Yong Chen (S'10-M'11) received the B.Eng. degree in electronic and information engineering, Communication University of China (CUC), Beijing, China, in 2005, and the Ph.D. in Engineering degree in microelectronics and solid-state electronics, Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), Beijing, China, in 2010.

From 2010 to 2013, He worked as Post-Doctoral Researcher in Institute of Microelectronics, Tsinghua University, Beijing, China. From 2013 to 2016, he was Research Fellow responsible for high-speed (40+Gb/s) wireline communication and Low Energy Electronic Systems (LEES) project under the Singapore-MIT Alliance for Research and Technology (SMART) on RF CMOS transceiver in VIRTUS/EEE, Nanyang Technological University (NTU), Singapore. He has been an Assistant Professor of the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV) of University of Macau, Macao, China, since March 2016.

His research interests include analog/biomedical detection and RF integrated circuit, mm-wave system and circuit, high-speed on-chip and chip-to-chip Electrical/Optical Interconnects.



Chirn Chye Boon (M'09-SM'10) received the B.Eng (Hons.) (Elect.) in 2000 and the PhD (Elect. Eng.) in 2004 from NTU, Singapore. Since 2005, he has been with NTU where he is currently an Associate Professor. Before that, he was with Advanced RFIC, where he worked as a Senior Engineer. He specializes in the areas of radio-frequency (RF) & MM-wave circuits and systems design for biomedical and communications applications. He has conceptualized, designed, and silicon-verified 80 circuits/chips for biomedical and communications applications. Chirn Chye has published over 100 refereed publications in the fields of RF and MM-wave. He is an author of the book "Design of CMOS RF Integrated Circuits and Systems".

Dr. Boon serves as a committee member for various conferences. He is an Associate Editor for the IEEE Transactions on Very Large Scale Integration Systems and the IEEE Electron Devices Letters Golden Reviewer. Since March 2010, he is the Programme Director for RF and MM-wave research in the S$50million research centre of excellence, VIRTUS (NTU). He is the Principal Investigator for industry/government research grants of S$8,646,178.22. He is the recipient of the Year-2 Teaching Excellence Award and Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU.