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A Low-Power Switched-Capacitor Capacitive Transducer With High Resolution

Xiaoling Zhang and P. K. Chan

Abstract—A new capacitive transducer using a pseudodifferential-input–single-ended output topology for low-power portable applications is presented. This is based on a switched-capacitor chopper-stabilized pseudodifferential integrator structure that is cascaded with a chopper-stabilized differential difference amplifier, consisting of a single output and a bandpass ac output. The measured results have shown that the transducer integrated circuit, with a sampling rate of 64 kHz in a 0.6- μm CMOS technology, dissipates 820 μA at a 3.3-V supply and exhibits a low noise characteristic. For a 100-Hz bandwidth, the input-referred minimum detectable capacitances are 57.24 and 33.82 aF with reference to the single output and the bandpass output, respectively.

Index Terms—Accelerometer, capacitive measuring circuit, capacitive transducer, chopper stabilization (CHS), differential difference amplifier (DDA), integrated sensor, switched-capacitor circuit.

I. INTRODUCTION

IN MEASURING acceleration or other relevant physical parameters, the capacitive sensing interface offers greater stability, good sensitivity, and lower temperature dependence. There are several different ways of measuring capacitance, such as alternating current bridge excitation [1], oscillator techniques [2], and charge/discharge [2], [3] techniques. The charge/discharge method can be implemented by a switched-capacitor (SC) technique, which is amenable to integration using a CMOS process. The overall performance of the sensing interface system is limited by the offset and $1/f$ noise of the input amplifier, as well as the charge injection of the switches in SC circuits. This is particularly significant when implementing in the CMOS process. Nevertheless, the $1/f$ noise in an op-amp can be reduced by a number of methods. Examples of the offset-cancellation techniques are correlated double sampling (CDS) [4] and chopper stabilization (CHS) [5]. The CDS technique can significantly cancel the $1/f$ noise and the dc offset; however, it is usually associated with a

complicated switch arrangement and a clocking scheme. On the other hand, the CHS technique has significant advantages of simple design and low-power consumption if the signal bandwidth is not significantly high, which benefits fully differential implementation.

Capacitive transducers have been found on a broad range of applications such as capacitive accelerometers [6]–[10] and capacitive measuring circuits [3], [7]. However, when the specifications are targeted for low-power applications, such as motion sensors for portable personal computers and acceleration-sensing devices that are capable of operating under a weak battery during automotive crashing, power and resolution become the conflicting design parameters. To achieve an optimum tradeoff in performance, the circuit architecture becomes the most critical issue. This raises the motivation for the research of a new transducer architecture as well as circuit techniques to meet the ultimate goal of having low power while maintaining reasonably good resolution and low drift characteristics (through the removal of the amplifier offset and the effective suppression of the charge injection effect).

In this paper, a new low-power pseudodifferential-input–single-ended output (PDISO) capacitive transducer is proposed. This includes 1) the chopper-stabilized pseudodifferential-input–differential-ended output (PDIDO) structure [8], which is advantageous in reducing the number of critical capacitors in a differential sensor network as well as minimizing the switch charge injection, noise, and offset, and 2) the chopper-stabilized differential difference amplifier (CHSDDA) with a bandpass filter (BPF) function, which ensures signal integrity in terms of a precision and dynamic range, performs natural differential-to-single-ended conversion with reduced component sensitivity, and provides dual outputs in the form of one single output and one bandpass signal-conditioning ac output for back-end signal processing of the transducer system.

II. REVIEW OF HIGH-RESOLUTION CAPACITIVE TRANSDUCERS

A. SISO Structure

The single-input–single-ended output (SISO) interface is a simple topology. However, it suffers from circuit offset, switch charge injection, and reset noise [11]. The improved circuit [9], as shown in Fig. 1, using a cascaded resettable-gain structure, could significantly reduce the charge injection effect and offset. The measurement sequence of this circuit consists of four successive operations, as depicted in Fig. 1(b). When Φ_1 is

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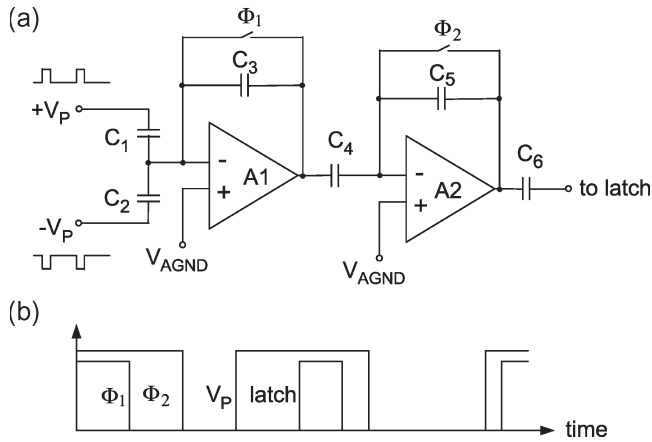


Fig. 1. Two-stage SC charge amplifier used for capacitive detection. (a) Simplified schematics. (b) Associated control signals for Φ_1 and Φ_2 , readout pulse V_P , and latch.

open, amplifier A1 charge injection and offset are precharged in C_4 . When Φ_2 is open, amplifier A2 clock charge injection and offset are precharged in C_6 . It is noted that opposite pulsed $+V_P$ and $-V_P$ are applied for the differential sensor fixed electrodes. The amplified signal is latched after settling of the signal. The reset feature in op-amps A1 and A2 demands substantial slew rate performance, thus leading to higher power consumption. Furthermore, the reset noise together with the common-mode rejection ratio or power supply rejection ratio issues would increase the circuit noise floor in a single-ended structure. Hence, they increase the difficulty to achieve good resolution.

B. DISO Structure

A precision SC transducer based on a differential-input-single-ended output (DISO) structure [10] is shown in Fig. 2. This circuit adopts the CDS technique combined with the auxiliary amplifier structure to cancel the $1/f$ noise and to minimize the systematic offset and errors arising from charge injection. There are three operating phases for the circuit operation—the Zerocap Phase, the Autozero Phase, and the Sense Phase. The Zerocap Phase is in association with the Autozero Phase to reset all the capacitors to the artificial analog ground. The differential-input structure in the auxiliary amplifier cancels the charge injection that is caused by opening switches $S6-$ and $S6+$ at the end of the Autozero Phase. The input-referred offset can be reduced by keeping the values of gain A1, gain A2, and ratio A1/A2 as large as possible. This structure can effectively reduce the amplifier offset and charge injection at the expense of complexity. The substantial number of switches would increase the switch sampling noise. Due to the reset action and the slew-rate issue, the special op-amp is hard to optimize with very low power.

C. Differential-Input-Differential-Ended Output Structure

The transducer [12] using a lossy integrator structure offers distinct advantages of simplicity with a low-pass filtering func-

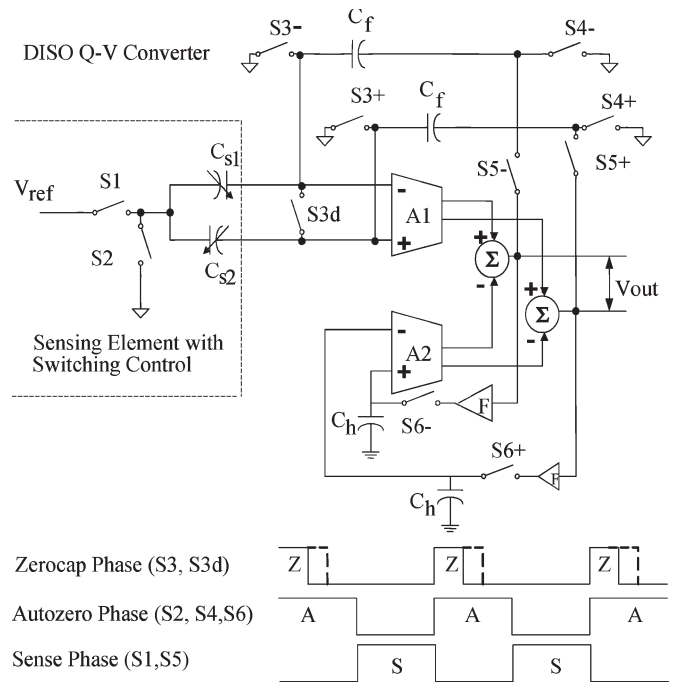


Fig. 2. DISO interface circuit and timing diagram.

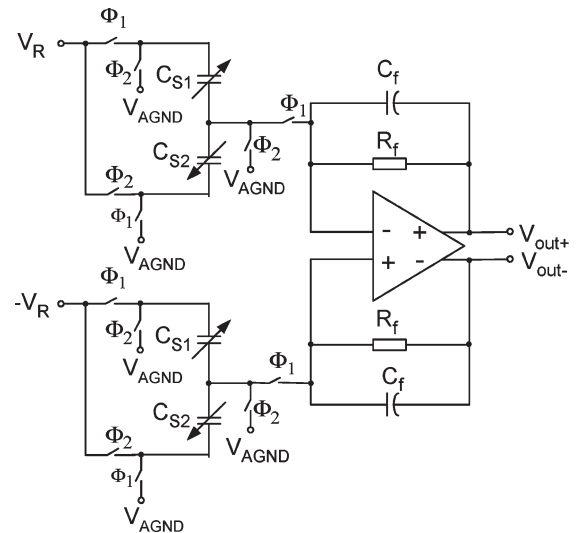


Fig. 3. Differential sensing interface using two pairs of differential capacitive sensors.

tion and low-power consumption through a reduced slew-rate requirement in an op-amp; however, it also suffers the same shortcomings as in the SISO structure because of the single-ended structure. Fig. 3 depicts the fully differential capacitive sensing interface circuit based on the extension of the single-ended output structure [12].

The transducer can effectively reduce the charge injection as well as the common-mode noise or signal due to fully differential operation. Of particular interest is the fact that the circuit needs two pairs of differential capacitive sensors, which is also common in other similar topologies [13]. The use of two pairs of differential capacitive sensors may not be

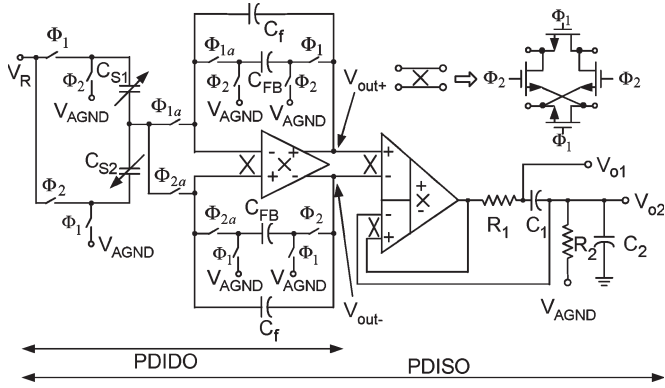


Fig. 4. Proposed SC capacitive transducer.

a cost-effective solution since high-dynamic-based differential capacitive sensing elements are not area-effective in the microelectromechanical technology. An alternative topology [6] needs one pair of differential capacitive sensors plus two critical reference capacitors, but this comes at the expense of increased sensitivity to mismatches in the capacitors. In addition, these circuits demand the op-amp with low-offset as well as low-noise specifications.

III. PROPOSED CAPACITIVE TRANSDUCER

A. Circuit Topology

The proposed PDISO structure, which consists of a chopper-stabilized PDIDO interface stage [8] and a CHSDDA stage, is shown in Fig. 4. Not only does the PDIDO structure act as an SC lossy integrator with an economical filtering function, but it also simplifies the sensor network and reduces the mismatching sensitivity in two capacitors when compared with typically four capacitors in most conventional schemes. This is based on the differential SC input resistors, which are formed by the capacitors C_{s1} and C_{s2} , together with an associated switching arrangement. For integration purposes, the passive feedback resistors are replaced by SC equivalents. Furthermore, the op-amp is replaced by a chopper-stabilized fully differential op-amp, which eliminates the $1/f$ noise and the offset. For a low-power objective, the lossy-integrator-based structure combined with an SC common-mode feedback (CMFB) circuit [8] for dc stabilization is preferred. The lossy integrator is designed as a natural filter to reject noise and is used to eliminate the use of a high slew-rate op-amp. This greatly limits the broadband thermal noise in the front-end stage before being amplified by subsequent stages. For back-end signal processing, a CHSDDA with BPF configuration is added to perform the accurate differential-to-single-ended conversion. The use of the differential difference amplifier (DDA) topology, as a replacement for the traditional differencing amplifier, relaxes the matching in resistive components. With reduced component sensitivity and the employment of an offset cancellation scheme among the signal-processing blocks, this allows a small trimming span if trimming procedures have been applied.

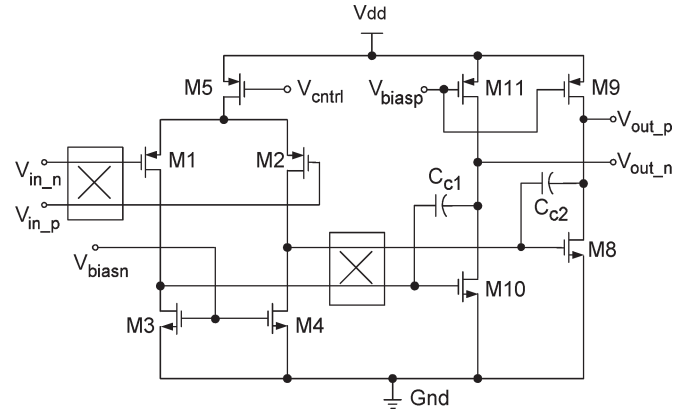


Fig. 5. Fully differential chopper-stabilized two-stage op-amp.

B. Analysis of the Proposed Capacitive Transducer

Referring to Fig. 4, the charge transfer in the PDIDO integrator can be established by the z -domain equations as follows:

$$(V_R - V_{AGND})(C_{S1} - C_{S2}) + C_{FB} [V_{out+}(z) - V_{AGND}] + C_f [V_{out+}(z) - z^{-1}V_{out+}(z)] = 0 \quad (1)$$

$$-(V_R - V_{AGND})(C_{S1} - C_{S2}) + C_{FB} [V_{out-}(z) - V_{AGND}] + C_f [V_{out-}(z) - z^{-1}V_{out-}(z)] = 0. \quad (2)$$

When the differential outputs are applied to the differential input of the DDA, as indicated in Fig. 4, the exact transfer function of the output voltage V_{o1} of the transducer is

$$V_{o1}(s) = V_{diff}(s) = V_{out+}(s) - V_{out-}(s) = \frac{-2(V_R - V_{AGND})(C_{S1} - C_{S2})}{C_{FB}} \times \frac{1}{1 + (1 - z^{-1})\frac{C_f}{C_{FB}}}. \quad (3)$$

If the sampling frequency is much larger than the signal frequency, using the approximation that $z^{-1} \approx 1 - sT$, the output voltages of the PDIDO front-end circuit in (1) and (2) are approximated as

$$V_{out+}(s) \approx \frac{C_{FB}}{C_{FB} + sTC_f} V_{AGND} - (V_R - V_{AGND}) \frac{C_{S1} - C_{S2}}{C_{FB} + sTC_f} \quad (4)$$

$$V_{out-}(s) \approx \frac{C_{FB}}{C_{FB} + sTC_f} V_{AGND} + (V_R - V_{AGND}) \frac{C_{S1} - C_{S2}}{C_{FB} + sTC_f}. \quad (5)$$

When the differential outputs are applied to the differential input of the DDA, as indicated in Fig. 4, the approximated

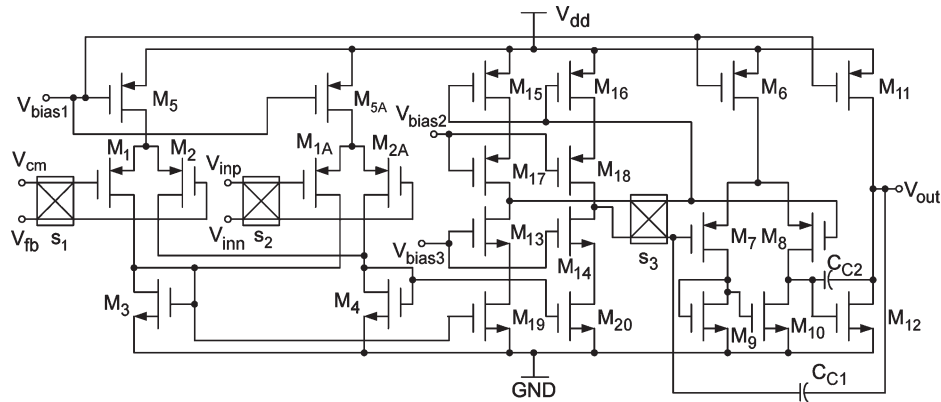


Fig. 6. Simplified schematic of the chopper-stabilized DDA.

transfer function of the output voltage V_{o1} of the transducer is obtained as follows:

$$V_{o1}(s) = V_{\text{diff}}(s) = V_{\text{out}+}(s) - V_{\text{out}-}(s) \\ \approx -2(V_R - V_{\text{AGND}}) \frac{C_{S1} - C_{S2}}{C_{\text{FB}}} \frac{1}{1 + sT \frac{C_f}{C_{\text{FB}}}}. \quad (6)$$

Since the maximum signal frequency of the transducer is 1 kHz, it is much smaller than the sampling frequency of 64 kHz. Therefore, (6) can be further approximated as

$$V_{o1}(s) \approx -(V_R - V_{\text{AGND}}) \frac{4\Delta C}{C_{\text{FB}}} \quad (7)$$

with $C_{S1} = C_{S0} + \Delta C$ and $C_{S2} = C_{S0} - \Delta C$, where C_{S0} is the nominal capacitive value of the sensor capacitance, and the other symbols have their usual meanings. It is noted that with $f = 1$ kHz, $f_s = 64$ kHz, $C_f = 1$ pF, and $C_{\text{FB}} = 1$ pF, the error that is contributed by first approximation $z^{-1} \approx 1 - sT$ in (6) was only 0.475% with respect to (3), whereas the error that is contributed by second approximation $sT \approx 0$ in (7) was only 0.958% with respect to (3). As can be observed in (7), the sensitivity of the SC transducer can be controlled by means of the difference of the reference voltages ($V_R - V_{\text{AGND}}$) and the value of C_{FB} . Of particular note is the fact that the output voltage V_{o1} represents the translated voltage from the capacitive sensing signal, with the signal frequency range down to dc.

In addition, the special op-amp that is used in the second stage is a CHSDDA being configured with a BPF. The transfer function is derived as follows:

$$H(s) = \frac{V_o}{V_{id}} = \frac{\frac{1}{R_1 C_2} s}{s^2 + s \left(\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1} \right) + \frac{1}{R_1 C_1 R_2 C_2}} \quad (8)$$

where $V_{id} = V_{in_p} - V_{in_n}$ is the differential input voltage of the DDA. Similarly, due to the BPF function, the output voltage V_{o2} is obtained as follows:

$$V_{o2}(s) = V_{\text{AGND}} + V_{\text{diff}}(s) \cdot H(s) \\ \approx V_{\text{AGND}} - (V_R - V_{\text{AGND}}) \frac{4\Delta C}{C_{\text{FB}}} \cdot H(s) \quad (9)$$

where $V_{\text{diff}}(s)$ is defined in (6). Note that the output V_{o2} is quiescently biased at V_{AGND} through the integrated resistor R_2 .

The ac sensitivity is identical to that of (7), and, at the same time, the output voltage is frequency-shaped by the transfer function $H(s)$. The transfer function can be programmed by the external capacitors C_1 and C_2 . Hence, this ac output is most suitable for ac-based applications.

C. Low-Power High Dynamic Range Amplifiers

The simplified schematic of the fully differential two-stage core op-amp is shown in Fig. 5. One chopper is placed at the input of the op-amp, whereas another chopper is placed between the first and second stages of the op-amp. However, the transistors M1–M5 form the input stage, whereas the transistors M8–M11 form the respective output stage. To achieve low-power consumption, the SC CMFB circuit [8] is used since it avoids the resistive output loading effect and is a linear discrete-time balanced circuit. The CMFB circuit is configured in a negative feedback loop with the core amplifier to regulate the common-mode output voltage against the variations via the gate of transistor M5.

For the chopper-stabilized DDA design, Fig. 6 depicts the simplified schematic, which comprises two stages. The first stage is the current-mirror op-amp incorporating the CHS technique, whereas the second stage is a simple two-stage op-amp. Both stages are biased through a common biasing voltage v_{bias1} , which is generated from the master current reference circuit (not shown for simplicity). The CHSDDA input positive port consists of n-type metal–oxide–semiconductor (NMOS) chopping switch network S1 and the transconductance stage (M1, M2, and M5). The CHSDDA negative input port consists of an NMOS chopping switch network S2 and the transconductance stage (M1A, M2A, and M5A). The chopper switch networks S1 and S2 modulate the respective input differential signal to the chopping frequency. The differential currents that are flowing through transistors M3 and M4 are converted back to differential voltages via the active load (M15–M18). On the other hand, transistors M15–M18, in conjunction with switch network S3, constitute the demodulator. The common gate connection of the active load is commutatively connected to the drains of M17 and M18 via the periodic chopping action of S3. The output voltages at the drains of M17 and M18 are, thus, demodulated. Last, the differential output of the first stage is coupled to the

TABLE I
SIMULATION RESULTS OF THE AMPLIFIERS THAT ARE USED
IN THE CAPACITIVE TRANSDUCER

Parameter	Fully Differential CHS Op-Amp	CHSDDA
DC Gain	101.7dB	139dB
UGBW	830 kHz	2.73MHz
Phase Margin	73° @ 30 pF	68° @ 15 k// 20 pF
Supply Current	150μA	250μA

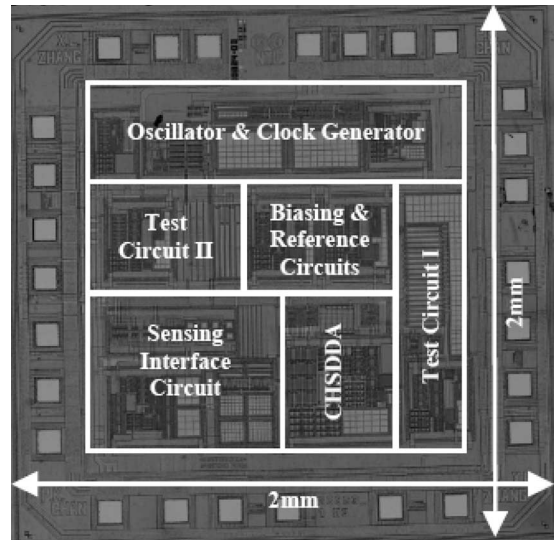


Fig. 8. Microphotograph of the SC capacitive transducer.

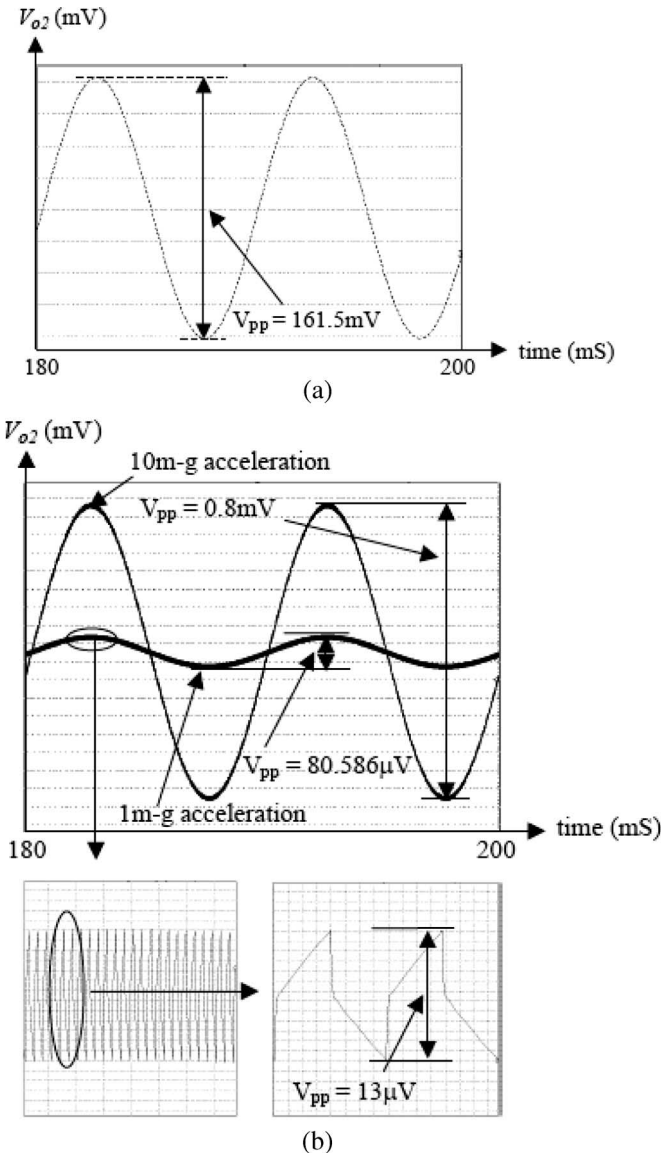


Fig. 7. Simulated output voltage waveform of the transducer. (a) At 2-g sinusoidal accelerations. (b) At 1- and 10-mg sinusoidal accelerations with zoom-in view.

inputs of the two-stage amplifier (M7–M12), serving multiple functions as a differential-to-single-ended converter, the final gain stage, and a buffer. Nested Miller frequency compensation is implemented from the topological placement of C_{C1} and C_{C2} .

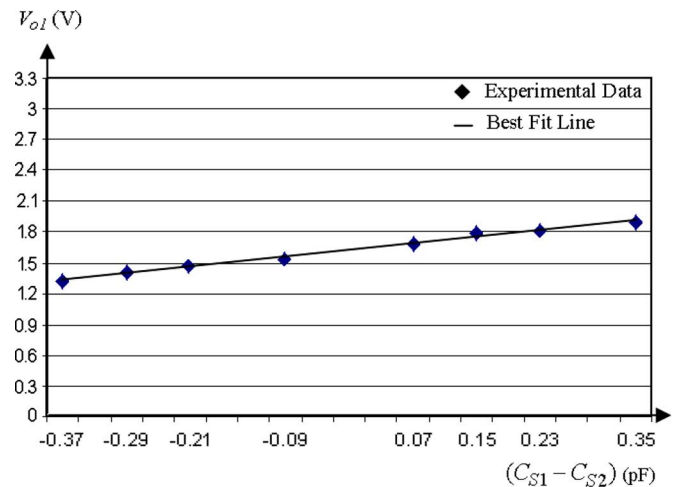


Fig. 9. Measured dc transfer function of the capacitive transducer at V_{o1} .

IV. RESULTS AND DISCUSSIONS

A. Simulation Results

The respective building block of the SC capacitive transducer was verified using HSPICE simulations with Level 49 models for the Austria Mikro Systeme International AG (AMS) 0.6-μm, N-well CMOS technology. The simulated results of the fully differential op-amp and the CHSDDA are summarized in Table I. A programmable oscillator [14] having an external resistor to set the oscillation frequency of 64 kHz was designed and simulated, with the nonoverlapping period of 2.3 nS at the typical condition (25°, 3.3 V).

For the ac response evaluation of the interface circuit, a realistic 2-g electrical sensor model [15] that takes into account nonideal effects was used, and the sensitivity of the sensor was 10 fF/g. It was given that $V_R = 0.65$ V, $V_{AGND} = 1.65$ V, and $C_{FB} = 1$ pF. When the sensor was excited with sinusoidal acceleration, the SC transducer exhibited a sinusoidal output response at V_{o2} . The circuit was simulated with a frequency of 100 Hz for 1-mg, 10-mg, and 2-g sinusoidal accelerations in

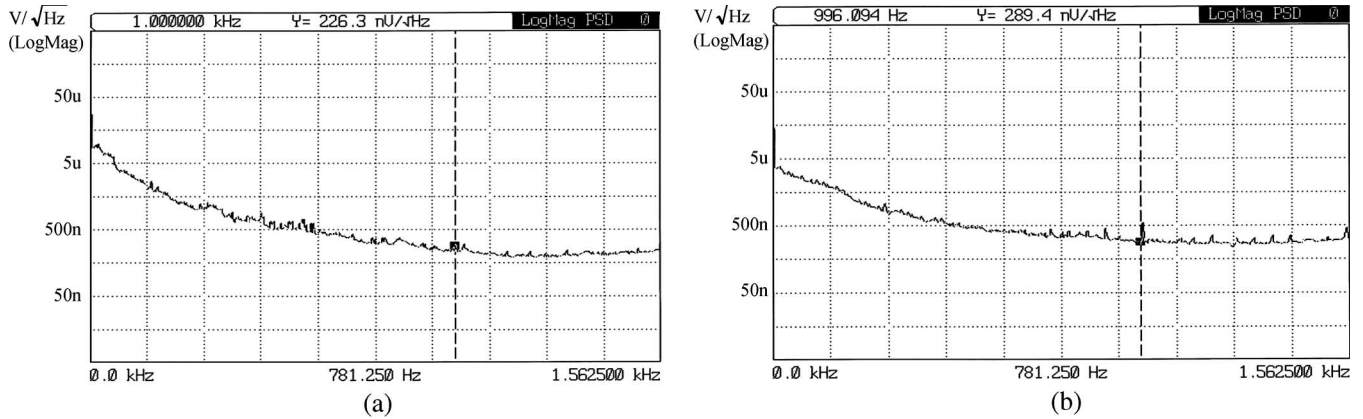


Fig. 10. Measured noise outputs of the capacitive transducer at 1 kHz. (a) At output V_{o1} . (b) At output V_{o2} .

Fig. 7. There is a slight difference between the simulated value and the ideal value of 160 mV for the full range of the 2-g sinusoidal acceleration shown in Fig. 7(a). The difference of 1.5 mV comes from the dominant nonlinearity of the capacitive sensing elements [15]. A portion of simulated output voltage waveforms of the interface circuit at 1- and 10-mg sinusoidal accelerations is shown in Fig. 7(b), with the zoom-in view to observe the magnitude of an ac ripple of $13 \mu\text{V}_{\text{pp}}$ at the 1-mg acceleration. The minute output signals have demonstrated that the proposed sensor interface circuit would exhibit high sensitivity.

B. Measured Results

The SC capacitive transducer was fabricated using the AMS 0.6- μm , N-well CMOS process. A microphotograph of the SC capacitive transducer is shown in Fig. 8. A series of measurements for the fabricated SC capacitive transducer were taken. The spectral plots were taken from a network analyzer (Stanford Research Systems Model SR770 network analyzer).

Different small values of discrete capacitors were used to model the variation of the capacitive sensing element in Fig. 4. Herewith, ceramic capacitors of 1 pF were adopted, and the effective values arising from various series combinations were measured by an HP 4284A Precision LCR meter. With $V_R = 1.15 \text{ V}$ and $V_{\text{AGND}} = 1.65 \text{ V}$, the measured dc voltage at the output V_{o1} against the capacitor difference ($C_{S1} - C_{S2}$) of total change in 0.7 pF is plotted in Fig. 9. This is quite a reasonable performance in view of the parasitic capacitances (estimated to be about 10 pF) that are associated with the nodes of sensing capacitors and the impact of charge injection on the minute capacitance values. The experimental results have validated that the transducer displays reasonably good linearity and sensitivity of approximately 0.9 V/pF. The measured supply current for the stand-alone transducer is 390 μA at a 3.3-V supply, which is very close to the simulated value of 400 μA . The measured supply current for the whole transducer IC (including the biasing circuit, the reference circuits, and the clock generator [14]) is 820 μA .

To evaluate the achievable resolution of the capacitive transducer, the output noise floor was measured at V_{o1} and V_{o2} , as shown in Fig. 10(a) and (b). The integrated output noise

TABLE II
MEASURED OUTPUT NOISE WITH AND WITHOUT THE BPF OF THE CAPACITIVE TRANSDUCER

Frequency Range	Without BPF		With BPF (0.1 Hz to 1 kHz)	
	Output Noise	Equivalent Resolution	Output Noise	Equivalent Resolution
30mHz to 1kHz	60.07 μV	66.74aF	46.13 μV	51.26aF
30mHz to 500Hz	59.83 μV	66.48aF	42.57 μV	47.3aF
30mHz to 100Hz	51.52 μV	57.24aF	30.44 μV	33.82aF

voltages for a different bandwidth are summarized in Table II. The measured noise voltage at output V_{o1} is larger than that at output V_{o2} because the BPF function of the CHSDDA improves the noise performance. Nevertheless, the values of the output noise are low in the proposed capacitive transducer (as shown in Table II). To quantify the performance metric of the capacitive transducer for accelerometer applications, a figure of merit (FOM) [20] that takes into account power and noise parameters is used. It is defined as follows:

$$\text{FOM} = (\text{rms output noise root spectral density}) \times (\text{power dissipation}). \quad (10)$$

Table III gives the comparison of the proposed work with the reported works [16]–[20]. It is noted that the measured output root spectral density of the proposed transducer is 6.6 μV_p at 3.91 Hz, which translates to 4.7 μV_{rms} by dividing the noise peak value by a scaling factor of $\sqrt{2}$ [22]. Taking the total power consumption of 2.71 mW to calculate the FOM, the result suggests that the proposed work gives the best FOM value. This is mainly due to the use of the CHS lossy-integrator interface architecture to effectively reduce noise at the fundamental front-end stage, which is in contrast to the conventional capacitive transducer structures that make use of the SC gain stage without a filtering function. Last, the simplicity of the filter-based CHSDDA circuit

TABLE III
COMPARISON OF THE REPORTED WORKS WITH THE PROPOSED WORK

References and Techniques	RMS Output Noise Root Spectral Density	Power Dissipation	FOM	Area and Technology
[Baschiroto 2003] [16] Two-chip approach, Open-loop, CDS using fully differential amplifier	26.1 $\mu\text{V}/\sqrt{\text{Hz}}$	22.5 mW (4.5mA at 5V)	0.587 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2.60 x 2.84 mm ² (0.5 μm CMOS process)
[Wu 2004] [17] Sensor-integrated, Open-loop, CHS using high BW amplifier	6.5 $\mu\text{V}/\sqrt{\text{Hz}}$	30 mW (6mA at 5V)	0.195 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	3.50 x 2.5 mm ² (0.5 μm CMOS MEMS process)
[Amini 2004] [18] Two-Chip approach, Open-loop, 1 st -order $\Sigma\Delta$ modulator	55 $\mu\text{V}/\sqrt{\text{Hz}}$	6 mW (2.4mA at 2.5V)	0.33 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2 x 2 mm ² (0.25 μm CMOS process)
[Petkov 2005] [19] Two-Chip approach, Open-loop, 4 th -order $\Sigma\Delta$ modulator	13.5 $\mu\text{V}/\sqrt{\text{Hz}}$	18 mW (3.6mA at 5V)	0.243 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2.3 x 2.3 mm ² (0.5 μm CMOS process)
[Lee 2008] [20] Two-Chip approach, Open-loop, Single-ended CDS SC amplifier with Injection-Nulling Switch Technique [21]	8.4 $\mu\text{V}/\sqrt{\text{Hz}}$	10 mW (2mA at 5V)	0.084 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2.8 x 2.3 mm ² (0.6 μm CMOS process)
[This work] Two-Chip approach, Open-loop, Pseudo differential CHS lossy integrator with filter-based CHSDDA	4.7 $\mu\text{V}/\sqrt{\text{Hz}}$	2.71 mW (820 μA at 3.3V)	0.013 $\mu\text{W}\cdot\text{V}/\sqrt{\text{Hz}}$	2 x 2 mm ² (0.6 μm CMOS process)

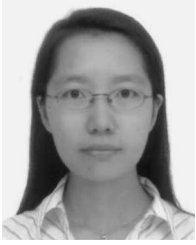
significantly further improves power and noise. As a result, the technical merits that are gained from the proposed circuit architecture lead to a low-power, high-resolution capacitive transducer.

V. CONCLUSION

A new SC capacitive transducer is presented. The proposed SC PDISO structure is simple, which reduces the circuit sensitivity arising from the reduction of matched component pairs, when compared with that of conventional fully differential topologies. The low-power design strategy combined with the chopper-stabilized fully differential op-amp and the CHSDDA has achieved low-power consumption, high resolution, and low noise. The experimental evidence confirms the stated objectives. The new SC capacitive interface IC will be useful for low-cost, high-performance accelerometers, ac-based motion sensors, and, more importantly, low-power portable capacitive transducer-based applications.

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