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Lee, W. F.; Chan, Pak Kwong

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A Capacitive-Based Accelerometer IC Using Injection-Nulling Switch Technique

W. F. Lee and P. K. Chan

Abstract—This paper presents a new fully integrated sensing interface and signal-conditioning application-specific integrated circuit (ASIC) for automotive accelerometers based on an “injection-nulling switch” (INS) technique. The INS technique simplifies the design of both the switched-capacitor (SC) sensing amplifier and its supporting building blocks without jeopardizing its performance. This is done by counteracting the impact of charge injection and clock-feedthrough effects on sensitivity, resolution, and offset. It also decreases the number of opamps, capacitors, and switches being used. This results in reduction of power consumption, potential switching noise, and kT/C noise (sampled thermal noise which increases with the number of SC pairs being used) in the ASIC. A two-chip approach has been adopted in the implementation, with ± 50 g sensing element and ASIC. The built-in trimming circuitry and signal-conditioning blocks, which includes a self-test circuit, are implemented internally to eliminate the need for external components. The experimental results have shown that the sensing system IC has achieved a power consumption of 10 mW (2 mA at 5 V), a maximum noise root spectral density of $11.87 \mu\text{V}_{\text{pk}}/\sqrt{\text{Hz}}$ equivalent to rms noise root spectral density of $0.187 \text{ mg}/\sqrt{\text{Hz}}$ at 15.63 Hz, a signal-to-noise dynamic range of 77 dB for 500-Hz bandwidth and 74 dB for 1-kHz bandwidth based on 50 g, and a maximum clock noise of 1.562 mV. The die size of the ASIC is $2.8 \text{ mm} \times 2.3 \text{ mm}$ using a standard $0.6\text{-}\mu\text{m}$ CMOS technology.

Index Terms—Accelerometer, sensor, signal conditioning, switched-capacitor (SC) circuits.

I. INTRODUCTION

ACCELEROMETERS have been popular ever since the safety requirement for automobiles has tightened, especially for seat belts and air-bag systems. This leads to a high demand for low-cost and small-size accelerometers capable of sensing up to 50 g (where 1 g is the acceleration due to earth gravitational force). Thus, integrated capacitive-based accelerometers that meet the requirements are well received [1]. Commercial products such as those in [2]–[4] are successful examples. The major challenge of designing accelerometers is in the front-end sensing interface. Sensing interfaces [5], [6] that make use of chopper stabilization technique are popular.

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W. F. Lee was with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798. He is now with the School of Electronic Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan Province 610054, China.

P. K. Chan is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: epkchan@ntu.edu.sg).

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Alternatively, other well-known front-end capacitive interfaces [7]–[11] using a switched-capacitor (SC) approach have been reported. Depending on the applications, power consumption is often one of the crucial factors to be considered in the design of sensing interfaces, especially in air-bag applications where there is a potentially low supply of power during a crash situation. Although a simple interface is able to minimize the power consumption, it often suffers from the switched charge injection problem [12], which greatly limits the resolution and affects the stability due to the offset drifting with temperature and time. Thus, an intricate front-end amplifier has been designed in order to compensate for the switch errors [13]. Fully differential operational amplifiers (opamps) with complex switch arrangements and capacitor pairs are commonly used, but they have the possibility of increasing power dissipation and introducing extra switching noise.

The safety requirement demanded by automotive regulations is another important issue in accelerometer design. Integrated accelerometer should provide a self-testing function [4], and this has imposed another design challenge on the sense amplifier. The open-loop structure is preferred because the closed-loop structure uses a force-balanced technique and, depending on the technologies, it may create difficulties in implementing the self-test feature.

In this paper, a design technique pertaining to low-power fully integrated signal-conditioning application-specific integrated circuits (ASICs) in a two-chip approach (i.e., the acceleration sensing element and the ASIC are bonded together on the same package) for automotive accelerometer applications is proposed. The ASIC employs an injection-nulling switch (INS) [14], [15] in the design of low-power front-end sense amplifiers so as to alleviate the switch charge injection problem. Not only does it simplify the front-end sense amplifier by using comparatively fewer switches, it is also able to achieve precision operation just by using a single-ended opamp without resorting to fully differential techniques. As a result, it improves the resolution and reduces the potential noise in the readout circuit. Furthermore, in the context of the switch error compensation, the INS allows a large time-constant single-ended SC filter to be implemented economically, which reduces the design complexity and power consumption significantly without sacrificing the performance. Moreover, it eases the design of the self-testing circuit in the open-loop sensing interface structure.

Section II describes the new front-end sensing interfaces. Section III shows how INS can be incorporated into a two-stage low-pass filter. Section IV depicts the implementation of the overall accelerometer system. The results of the measurement

Fig. 1. Proposed front-end sensing amplifier with employment of INS and self-test switch network.

are discussed in Section V, and the conclusions are drawn in Section VI.

II. FRONT-END SENSING INTERFACE

Fig. 1 shows the proposed front-end sensing interface (or sensing amplifier) using a capacitance-to-voltage converter [12], which incorporates a correlated double-sampling (CDS) technique to reduce both the offset and the low-frequency noise of the amplifier [16]. The differences between the new topology and the conventional topologies [17]–[19] are: 1) the employment of an INS [14], [15] (dotted box in Fig. 1) as a replacement of conventional analog switch and 2) the additional control switches S_3 and S_6 that permit the potential difference of V_{dd} and analog ground to be applied for the capacitive sensor in self-test mode. The INS is effective in compensating for the switch errors arising from switch charge injection and clock feedthrough in single-ended applications. More importantly, it is also insensitive to process variations in comparison with other conventional analog switch types. The added self-test network has the advantages of simplicity and ease of realization.

The front-end circuit is essentially a capacitance-to-voltage converter converting the change of the capacitance value of the capacitive sensing element into voltage. In response to the change of capacitance in the differential capacitive sensor (Fig. 1), the extra feedback loop realized by using a holding capacitor C_h and its associated switches is to ensure that the output voltage V_{sense_out} changes as little as possible between clock phases T_1 and T_2 in each switching period. This structure also reduces the dc error of the realized gain by a factor of $1/A_0^2$ [12], where A_0 is the finite open-loop gain of the opamp. As a result, the circuit relaxes the opamp performance parameters in the context of settling time, open-loop gain, and slew-rate issue. These are the favorable characteristics for implementing a low-power opamp as far as the worst-case slew-rate specification has been met. The output voltage V_{sense_out} at the steady state is given as

$$V_{sense_out} = \frac{(C_{S1} - C_{S2})}{C_f} (V_{REF} - V_{AG}) + V_{AG} \quad (1)$$

where C_{S1} is the capacitance between the top and middle plates of the sensing element defined by $C_{S1} = C_o + \Delta C_S$, and C_{S2} is

Fig. 2. Clocking sequence of INS operation to explain the cancellation of charge injection and clock-feedthrough errors.

the capacitance between the bottom and middle plates defined by $C_{S2} = C_o - \Delta C_S$. Note that C_o is the nominal capacitance under zero acceleration when the middle sensing plate is midway between the two fixed (top and bottom) plates whilst ΔC_S is the change of capacitance when the middle plate is displaced by an external acceleration. The two sensing capacitors are switching between the reference voltages V_{REF} and the analog ground voltage V_{AG} . The change of output voltage V_{out} with reference to nominal analog ground potential (V_{AG}) can be expressed as

$$V_{out} = V_{sense_out} - V_{AG} = \frac{2(V_{REF} - V_{AG})}{C_f} \Delta C_S. \quad (2)$$

The INS connected to the input of the opamp is realized by a switch S_{INSi} , a switch S_{INSn} , and a capacitor C_{INSn} , as illustrated in Fig. 1. With the employment of INS, the circuit is able to resolve a much more precise output value, resulting in an increase of the capacitance sensing resolution. The switch S_{INSi} and the switch S_{INSn} are implemented using a single MOS transistor of identical size. The operation of the INS can be explained using the clocking sequence shown in Fig. 2. It is noted that T_1 and T_2 are biphasic clock signals.

During the time period of τ_1 , both switches ($S_{\text{INS}i}$ and $S_{\text{INS}n}$) are turned on (clocks T_2 and T_{db} are high) and the output signal $V_{\text{sense_out}}$ is then sampled into $C_{\text{INS}n}$ and node Y (Fig. 1) through C_h . At the start of τ_2 , $S_{\text{INS}i}$ remains on, but $S_{\text{INS}n}$ is turned off. When the clock transits from a high supply voltage V_{DD} (ON) to a low supply voltage V_{SS} (OFF), the error charges caused by the channel charge injection and the clock-feedthrough error of $S_{\text{INS}n}$ will be stored in $C_{\text{INS}n}$ and node Y. Unlike the error charges stored in $C_{\text{INS}n}$, the error charges that are injected into node Y will be absorbed by the output signal as $S_{\text{INS}i}$ is still in the ON state. At the beginning of τ_3 (also called the injection phase), $S_{\text{INS}n}$ remains off while $S_{\text{INS}i}$ is switched off. The switching off of $S_{\text{INS}i}$ will create the main source of switch error voltage to the output because the transistor $S_{\text{INS}i}$ will inject its switch error charges into the input (node Y) of the opamp. It is also noted that there is no change in the charges stored in $C_{\text{INS}n}$ because transistor $S_{\text{INS}n}$ is still in the OFF state. The operation of the circuit during time interval τ_4 (nulling phase) is the most crucial phase of the operation because a precise replica of the sampled signal has to be passed to the output. Hence, the error charges at node Y that were injected during τ_3 must be eliminated. At the start of the nulling phase τ_4 , while $S_{\text{INS}i}$ remains off and $S_{\text{INS}n}$ is switched on again, electrons from $C_{\text{INS}n}$ and node Y are drawn into $S_{\text{INS}n}$ to form the inverted channel, whilst clock-feedthrough error charges are generated in reverse polarity due to positive transition of the clock signal from V_{SS} (OFF) to V_{DD} (ON) on both sides of $S_{\text{INS}n}$. The flow of these two error-compensating charges is in complete reverse direction to the flow of error charges created by the switching-off action of $S_{\text{INS}n}$ in τ_2 and switching-off action of $S_{\text{INS}i}$ in τ_3 previously. As the switches are identical to each other, the output error voltage will be reduced significantly by this reverse directional canceling action.

Regarding the self-test case, two switches S_3 and S_6 are controlled by a digital control bit B_{st} as shown in Fig. 1. It is noted that B_{st} is low (digital “0”) during normal sensing operation. To activate the self-test operation, B_{st} is set to high (digital “1”), which connects the sensor bottom plate to V_{AG} (Fig. 1) and enables the sensor top plate to be switched between V_{DD} (5 V) and V_{AG} (2.5 V). With the bottom plate held at V_{AG} , the switching of the top plate establishes an electric field between the top and middle plates. The electric field will produce a net electrostatic force to displace the movable middle plate a distance from its equilibrium position. As a result, a difference in the sensing capacitance is created and, hence, produces a self-test voltage being displayed at the output $V_{\text{sense_out}}$. On the other hand, if the sensor is faulty, the middle plate would fail to move under the influence of the electrostatic force. Then, the self-test voltage will not be sensed at $V_{\text{sense_out}}$.

It is well known that cascode opamps with a slew-rate enhancement circuit have the advantages of high power supply rejection ratio (PSRR), fast settling time, and low power consumption. Fig. 3 shows the slew-rate-enhanced [12] folded-cascode opamp used in the sensing amplifier. The input transistors M_{p1} and M_{p2} are pMOS transistors because they have lower flicker noise than that of the nMOS transistors. In addition, they are biased by the cascode current source transistors M_{p3} and M_{p4}

Fig. 3. Simplified folded-cascode opamp circuit with improved slew rate.

Fig. 4. Programmable SC gain stage with gain and offset calibration.

to achieve high common-mode rejection ratio (CMRR). Transistors M_{p5} , M_{p6} , M_{p7} , and M_{p8} realize a high-swing cascode current mirror to obtain a high open-loop gain. Transistors M_{p9} and M_{p10} are added to improve the slew-rate parameter of the opamp. The current sources (M_{n3} and M_{n4}) in conjunction with the active loads (M_{p5} and M_{p6}) are optimized in dimensions to achieve minimum noise according to [20]. The current consumption of the opamp is $180 \mu\text{A}$ at 5-V supply.

Fig. 4 shows the SC gain stage with programmable capacitors for gain and offset adjustment to the sensing amplifier. This calibration is essential because it compensates the parameter variations arising from the fabrication of the acceleration capacitive sensor and limits the output amplitude within 0.4 V before entering the filter stage. Similar to the sensing amplifier, the gain stage utilizes the capacitive-reset topology together with the employment of INS (dotted box) to minimize the switch injection errors.

III. LOW-PASS FILTER

A low-pass filter (LPF) is necessary to remove the out-of-band noise. Area efficiency and low power dissipation are the major considerations in designing LPFs for the signal-conditioning circuit. As the cutoff frequency for the type of filter tends to be low (1 kHz and below), there exists an implementation problem in the continuous-time filter (CTF) since large resistors and capacitors are needed. Conversely, a switched-capacitor filter (SCF) is able to realize a very low

Fig. 5. Programmable SC Sallen-Key LPF stage.

cutoff frequency using small capacitors. Hence, a cascade of the SCF and CTF gives an optimal solution for area efficiency. On the other hand, the Bessel filter response is usually preferred over its counterparts such as Butterworth and Chebyshev because of its linear phase and zero overshoot properties [21], which are required by automotive air-bag applications [4]. Nevertheless, the roll-off rate in the stop band is lower, leading to a high-order filter that has to be implemented, which will result in the increase of power consumption. Hence, to solve this problem, a Sallen-Key structure realizing a Bessel filter response is employed as the number of opamps can be reduced. The downside of this approach is that the Sallen-Key structure has a limited common-mode voltage range due to noninverting configuration [22]. Therefore, the input signal is kept low (below 0.4 V by the preceding gain stage), and the filter system is designed to have a unity gain.

As shown in Fig. 5, the filter stage is a second-order SCF using Sallen-Key topology [22]. The objectives of including this filter stage are, first, to employ the INS for ensuring that the signal quality does not suffer from potential switch error and that the filter can operate at large capacitor ratios for a minimum 500-Hz system bandwidth; second, to provide economical implementation without resorting to fully differential structure. Third, as long as kT/C is within the acceptable noise level, SCF has the advantage of realizing a very large resistance value with a small value of capacitor because the equivalent resistance value is inversely proportional to the clocking frequency and the capacitance. The equivalent resistor connected to the input V_{tc_out} is realized by switches S_{11} , S_{12} , S_{13} , and S_{14} , and capacitor C_{r1} while the resistor that is connected to the noninverting input of the opamp is realized by switches S_{21} , S_{22} , S_{23} , and S_{INSi} and capacitor C_{r2} . The INS (dotted box) consists of a switch S_{INSi} , a switch S_{INSn} , and a capacitor C_{INS} . The cutoff frequency can be selected as either 1 kHz or 500 Hz via programming a digital bit B_{capsel} . The component values are calculated according to the Bessel transfer function given in [21]. The capacitances C_{r1} and C_{r2} are equal and are calculated from the equivalent resistance as

$$C_{r1} = C_{r2} = \frac{1}{f_{clk} R_{eq}}. \quad (3)$$

Fig. 6 shows the second filter stage, which is a third-order CTF. It is realized using a passive first-order LPF cascaded to a second-order low-pass Sallen-Key filter. Based on the clock frequency of 125 kHz and the practical values of integrated resistors and capacitors, a specification of 5-kHz cutoff frequency

Fig. 6. Continuous-time Sallen-Key LPF stage.

Fig. 7. Architecture of the accelerometer system IC.

is chosen. This structure requires only one opamp to implement a third-order LPF. For matching consideration and ease of design, the resistors R_1 , R_2 , and R_3 are designed to have the same resistance. The values of the other components are selected according to a third-order Bessel filter response [21].

IV. SYSTEM IMPLEMENTATION

The accelerometer system architecture with respective building blocks is illustrated in Fig. 7. The ASIC comprises a sense amplifier, a gain stage, a filter stage, an output stage, an oscillator [23], a clock generator [23], a trimming and control logic circuit [23], and a serial-to-parallel register [23]. The self-test and the filter bandwidth are controlled by respective external inputs. The programming data are serially shifted into the serial-to-parallel register to provide the calibration data for the trimming and control logic circuit. With these calibration data, the circuit will then calibrate the gain stage, the output stage, as well as the oscillator. After the required output has been calibrated, the finalized settings will be programmed through the program on/off pin that enables the programming of polysilicon fuses in the trimming circuits.

The implementations of the sensing amplifier, the gain stage, and the filter stage have been described in the preceding sections, and note that the oscillator, the clock generator, the trimming and control logic circuit, and the serial-to-parallel register were explained in [23]. The output stage, comprising a scaling amplifier (using low-power class-AB opamp topology [24]) and trimming resistor topology [22], calibrates the output signal based on a full-scale of 4.5 V (0.25 to 4.75 V), equivalent to 100 g peak-to-peak value, with a 5-V supply. The current consumption for the entire ASIC is designed to be 2 mA in typical conditions. Fig. 8 shows the microphotograph of the

TABLE I
COMPARISON OF OUTPUT SIMULATION RESULTS OF THE SENSING AMPLIFIER USING DIFFERENT SWITCH TOPOLOGIES
UNDER THREE DIFFERENT OPERATING CONDITIONS

Case	Typical Condition (Typical transistor model, V_{dd} @ 5V, V_{REF} @ 3.5V, temp @ 25°C)		Worst-Power Condition (Worst-power transistor model, V_{dd} @ 5.5V, V_{REF} @ 3.5V, temp @ -40°C)		Worst-Speed Condition (Worst-speed transistor model, V_{dd} @ 4.5V, V_{REF} @ 3.5V, temp @ 90°C)	
	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)
1. Ideal Switch	2.599984	-----	2.599994	-----	2.599946	-----
2. Single MOS Switch	2.606437	6.453	2.606564	6.57	2.607523	7.577
3. Dummy Switch	2.600152	0.168	2.596963	3.031	2.603509	3.563
4. INS	2.599984	0.0001	2.599998	0.004	2.599951	0.005

Fig. 8. Microphotograph of the accelerometer ASIC.

Fig. 9. Microphotograph of the proposed accelerometer system IC in a 16-pin DIL package.

ASIC, which illustrates the various building blocks that have been discussed.

The ASIC is fabricated using AMS (Austria Mikro Systeme International AG) 0.6- μm , n-well, double-poly and triple-metal CMOS process. The die size of the ASIC is 2.8 mm $\times$ 2.3 mm. The ASIC is bonded to ± 50 g sensing element (a commercial type from Temic) in a 16-pin DIL package. The microphotograph of the entire accelerometer system IC is shown in Fig. 9.

V. RESULTS AND DISCUSSIONS

To verify the INS effectiveness on minimizing the switch errors, four different cases of switch topologies were implemented

on S_i in the sensing amplifier of Fig. 1 (normal sensing operation) and the results were compared using Hspice simulations. Case 1 is an ideal switch, which will not exhibit any switch error. Case 2 is a single MOS switch topology (a single nMOS transistor acting as a switch). Case 3 is a dummy switch (DS) topology [12] formed by a main nMOS transistor connected to a half-size dummy switch (NMOS transistor with half size of that of the main nMOS transistor), with its drain and source being tied together. While the main nMOS transistor is connected to C_h , the drain and source of the half-size dummy switch (which is switched by a clock signal complementary to that of the main transistor) is connected to the inverting input of the opamp. Case 4 is the INS topology. Each of the switches S_{INSi} and S_{INSn} was implemented using a single nMOS transistor, and the connection of the INS can be referred to the dotted box in Fig. 1. Note that, other than S_i , all of the switches in Fig. 1 were implemented using CMOS switches and each of the sensing capacitors C_{S1} and C_{S2} was also been replaced with a fixed capacitor. To have a fair comparison, the nMOS transistor in case 2, the main nMOS transistor in case 3 and the two nMOS switches in case 4 were designed to be identical to each other, whereas the dummy transistor switch in case 3 is half the size of the main nMOS transistor. Fixing $V_{REF} = 3.5$ V, $V_{AG} = 2.5$ V, and $(C_{S1} - C_{S2})/C_f = 0.1$, the output voltage V_{sense_out} of the sense amplifier was designed to have an ideal voltage of 2.6 V according to (1). These circuits were simulated under typical, worst power, and worst speed conditions using Hspice level-49 transistor models of AMS 0.6- μm CMOS technology.

Fig. 10 depicts the simulation results of the four types of switch topology under typical condition. The INS operation on nulling the switch error is also highlighted. Fig. 11 gives the expanded view of the dotted box in Fig. 10, indicating the actual value of the output voltage V_{sense_out} . Table I summarizes the simulation results without switch mismatch under the three conditions. The absolute errors in Table I are calculated using ideal switch topology results as reference. The simulation results have shown that the switch errors in INS are smaller than that of the other two topologies and the output voltage at the end of nulling phase is equivalent to that of the ideal switch topology.

Figs. 12–14 illustrate the simulation results of the circuits with intentional mismatches (3%, 5%, and 8%) in the DS topology and the INS topology. It can be observed that the respective output voltage has deviated from that in Fig. 11 in

Fig. 10. Simulation results of the sensing amplifier with four types of switch topologies under typical conditions.

Fig. 11. Expanded view of the simulation results in Fig. 10.

view of mismatch effects and process parameters variations. These results are summarized in Table II, and the comparison of the absolute error voltage under different mismatch conditions are plotted in Fig. 15. Considering a mismatched factor of typically 5% (that is, a lumped mismatch factor contributed by mismatches on gate oxide thickness, charges mobility, threshold voltage, and dimension), the error voltage using DS is 1.1 mV under typical condition, 2.231 mV under worst power condition, and 4.754 mV under worst speed condition, while using INS it is 0.469, 0.204, and 0.602 mV, respectively. Comparing the maximum error voltages at 8% mismatch under worst case condition, the error for DS is 5.35 mV while for INS it is 0.9 mV. Note that, under worse power conditions, the output voltage of the DS topology is less than that of the ideal switch because the dummy switch has overcompensated for the main switch errors. It can also be observed that the

Fig. 12. Simulation results of DS and INS topology with intentional mismatches under typical condition.

Fig. 13. Simulation results of DS and INS topology with intentional mismatches under the worst power conditions.

increase in error voltages for each step of percentage mismatch in INS topology is less and the deviation of the output voltage from the ideal value is lower than that of the DS topology. Thus, these results have revealed that not only does INS have a better precision performance in minimizing the switch error but it is also insensitive to variation in process parameters. In comparison, the DS topology is less effective than INS owing to the fact that the main nMOS transistor is difficult to match to the half-sized nMOS transistor. Hence, the compensation of the switch error becomes more sensitive to variation of process and environmental parameters.

A series of measurements for the ± 50 -g accelerometer IC was taken. The time-domain measurement results were obtained using an oscilloscope (HP 54645D MegaZoom Mixed-Signal oscilloscope) whereas the spectral plots were taken from a network analyzer (Stanford Research Systems Model SR770 FFT Network Analyzer). The acceleration excitation to the

TABLE II
COMPARISON OF OUTPUT SIMULATION RESULTS OF THE SENSING AMPLIFIER USING DS AND INS TOPOLOGIES
WITH INTENTIONAL MISMATCHES UNDER THREE DIFFERENT OPERATING CONDITIONS

Case	Typical Condition (Typical transistor model, V_{dd} @ 5V, V_{REF} @ 3.5V, temp @ 25°C)		Worst-Power Condition (Worst-power transistor model, V_{dd} @ 5.5V, V_{REF} @ 3.5V, temp @ -40°C)		Worst-Speed Condition (Worst-speed transistor model, V_{dd} @ 4.5V, V_{REF} @ 3.5V, temp @ 90°C)	
	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)	V_{sense_out} (V)	Absolute Error Voltage (mV)
Ideal Switch	2.599984	-----	2.599994	-----	2.599946	-----
DS (0% mismatch)	2.600152	0.168	2.596963	3.031	2.603509	3.563
(3% mismatch)	2.600618	0.634	2.597363	2.631	2.604105	4.159
(5% mismatch)	2.601084	1.1	2.597763	2.231	2.60470	4.754
(8% mismatch)	2.60155	1.566	2.598163	1.831	2.605296	5.35
INS (0% mismatch)	2.599984	0.0001	2.599998	0.004	2.599951	0.005
(3% mismatch)	2.600219	0.235	2.600198	0.204	2.60025	0.304
(5% mismatch)	2.600453	0.469	2.600396	0.402	2.600548	0.602
(8% mismatch)	2.600687	0.703	2.600595	0.601	2.600846	0.9

Fig. 14. Simulation results of DS and INS topology with intentional mismatches under the worst speed conditions.

Fig. 15. Comparison of the absolute error voltage of DS and INS under different mismatch conditions.

accelerometer IC was performed using a vibration shaker (Ling Dynamic Systems LDS V406).

Fig. 16. Measured output spectrum of the ASIC for full-scale ± 50 -g excitation at 500 Hz.

The measured power consumption of the proposed accelerometer IC is 10 mW, consuming 2 mA at a 5-V power supply, without an external active circuit. The measured output spectrum in Fig. 16 shows the fundamental and its harmonic contents together with the noise floor of the output voltage for ± 50 -g excitation at 500 Hz. The odd harmonics are due to the nonlinearity of the differential capacitive sensor [25] while the even harmonics are caused by the mismatch between the two sensing capacitors C_{S1} and C_{S2} .

The output noise power spectral density plot is shown in Fig. 17. A maximum output noise root spectral density of $11.87 \mu V_{pk}/\sqrt{Hz}$, which is equivalent to an rms noise root spectral density of $0.187 mg/\sqrt{Hz}$, at frequency of 15.63 Hz is obtained. This corresponds to a dynamic range of 77 dB for a 500-Hz bandwidth and 74 dB for a 1-kHz bandwidth based on a two-pole filter bandwidth using a bandwidth scaling factor of 1.4 [26] for a 50-g input with a sensitivity of 45 mV/g. For applications with 100-Hz bandwidth, the accelerometer IC can attain a dynamic range of 84 dB. The time-domain clock noise

Fig. 17. Measured noise root spectral density.

Fig. 18. Measured time-domain clock noise.

Fig. 19. Measured time-domain output voltage of the ASIC for full-scale ± 50 -g excitation at 500 Hz.

at the ASIC output is shown in Fig. 18. It has demonstrated that the filtering stage is effective in reducing the clock noise to 1.562 mV_{pp}. These results confirm that the application of the INS into the accelerometer design has improved the resolution and noise performance of the readout circuit on the basis of simplicity. Furthermore, Fig. 19 shows the measured time domain response of ± 50 -g excitation at 500 Hz. The excitation

Fig. 20. Measured peak-to-peak ac output voltage against acceleration excitation at 500 Hz.

Fig. 21. Measured percentage linearity error against acceleration excitation at 500 Hz.

TABLE III
SUMMARY OF THE PERFORMANCE OF THE PROPOSED ACCELEROMETER
USING THE INS TECHNIQUE

Performance Index	Proposed Work
Supply Current	2mA
Operating Power at 5V	10mW
Output Noise Root Spectral Density (in V/√Hz)	11.87μVpk/√Hz at 15.63Hz
RMS Noise Level (in Vrms)	0.314mVrms (1kHz BW)
Output RMS Noise Root Spectral Density (in g/√Hz)	0.187mg/√Hz at 15.63Hz
RMS Noise Level (in g rms)	7mg (1kHz BW) 5mg (500Hz BW) 2.2mg (100Hz BW)
Clock Noise	1.562mVpp (0.781mVpk)
Self Test Output Change	1.547V (equivalent to 34.4g)
-3dB Bandwidth	dc to 1kHz
Sensitivity	45mV/g
Acceleration Range	±50g
Full-scale Output Voltage Range for ±50g	0.25V to 4.75V
Power Supply	5V
Non-Linearity Error	1%
Integration Approach	Two-Chip

of ± 50 g caused the output voltage to swing with a full-scale magnitude of 4.5 V_{pp}. Fig. 20 shows the peak-to-peak output voltage plot for the range of acceleration excitation from 0 to ± 50 g. The measured data points are plotted together with the best-fit line. It can be observed that the transfer function is quite

TABLE IV
COMPARISON OF REPORTED WORKS WITH THIS WORK

Reference and Techniques	RMS Output Noise Root Spectral Density	Power Dissipation	FOM	Area and Technology	Self-test Function
[Kuehnel 1994] [5] Fully-integrated, Closed-loop, CHS using high BW FD amplifier	98 $\mu\text{V}/\sqrt{\text{Hz}}$	50 mW (10 mA at 5 V)	4.9 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process)	Yes
[Chau 1996] [27] Fully-integrated, Closed-loop, CHS using high BW FD amplifier	120 $\mu\text{V}/\sqrt{\text{Hz}}$	40 mW (8 mA at 5 V)	4.8 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3 x 3 mm ² (3 μm BiCMOS process)	Yes
[Lemkin 1999] [28] Fully-integrated, Closed-loop, 1-bit 2 nd -order $\Sigma\Delta$ modulator, charge integrator using FD amplifier	4.4 $\mu\text{V}/\sqrt{\text{Hz}}$ (x-axis)	45mW (9 mA at 5 V) (x-axis)	0.198 $\mu\text{W-V}/\sqrt{\text{Hz}}$ (x-axis)	4 x 4 mm ² (2 μm CMOS MEMS process)	No
[Kulah 2000] [29] Two-chip approach, Closed-loop, 1-bit 1 st -order $\Sigma\Delta$ modulator, CDS front-end charge integrator	110 $\mu\text{V}/\sqrt{\text{Hz}}$	7.2 mW (1.44 mA at 5 V)	0.792 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3.4 x 3.6 mm ² (3 μm CMOS process)	No
[Baschiroto 2003] [30] Two-Chip approach, Open-loop, CDS using FD amplifier	26.1 $\mu\text{V}/\sqrt{\text{Hz}}$	22.5 mW (4.5 mA at 5 V)	0.58725 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2.60 x 2.84 mm ² (0.5 μm CMOS process)	Yes
[Wu 2004] [31] Sensor-integrated, Open-loop, CHS using high BW amplifier	6.5 $\mu\text{V}/\sqrt{\text{Hz}}$	30 mW (6 mA at 5 V)	0.195 $\mu\text{W-V}/\sqrt{\text{Hz}}$	3.5 x 2.5 mm ² (0.5 μm CMOS MEMS process)	No
[Amini 2004] [32] Two-Chip approach, Open-loop, 1 st -order $\Sigma\Delta$ modulator	55 $\mu\text{V}/\sqrt{\text{Hz}}$	6 mW (2.4 mA at 2.5V)	0.33 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2 x 2 mm ² (0.25 μm CMOS process)	No
[Petkov 2005] [33] Two-Chip approach, Open-loop, 4 th -order $\Sigma\Delta$ modulator	13.5 $\mu\text{V}/\sqrt{\text{Hz}}$	18 mW (3.6 mA at 5V)	0.243 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2.3 x 2.3 mm ² (0.5 μm CMOS process)	No
[This work] Two-chip approach, Open-loop, CDS using single-ended amplifier with INS	8.4 $\mu\text{V}/\sqrt{\text{Hz}}$	10 mW (2 mA at 5 V)	0.084 $\mu\text{W-V}/\sqrt{\text{Hz}}$	2.8 x 2.3 mm ² (0.6 μm CMOS process)	Yes

Fig. 22. Measured output response under self-test mode.

linear. Fig. 21 shows that the measured percentage linearity error is within 1%. The linearity error of 1% obtained is still acceptable for automobile air-bag applications. Finally, Fig. 22 shows the measured self-test response. An output voltage of 1.547 V, equivalent to 34.4 g, under the self-test mode was obtained. This voltage is large enough for easy detection, which will relax the resolution of the comparator designed for indicating fault in the sensing element.

Table III summarizes all of the results mentioned. Table IV gives the comparison of the reported works with the proposed work. In order to evaluate the performance of different sensing

interface circuits, a figure of merit (FOM) is introduced. It is defined as the product of spectral noise and power, i.e.,

$$\text{FOM} = (\text{rms output noise root spectral density}) \times (\text{power dissipation}). \quad (4)$$

The lower the FOM is, the better the tradeoff is in terms of power and noise. Note that the unit for FOM is $\mu\text{W-V}/\sqrt{\text{Hz}}$.

It can be seen from Table IV that the result of this study has exhibited the best FOM value among the reported works. In summary, it has verified that the proposed accelerometer IC in conjunction with its design methodologies is promising for obtaining the optimum tradeoff in the realization of low-power low-noise accelerometer systems.

VI. CONCLUSION

A low-power low-noise ASIC for automotive accelerometers in standard CMOS technology has been presented. The experimental evidence has confirmed that the proposed INS-based accelerometer ASIC design has led to a high-dynamic-range system while maintaining design simplicity. The system performance has improved significantly in terms of power consumption, noise, accuracy, resolution, and integration capability. Through the use of the INS technique to dedicated SC circuit topologies, the apparent advantage is the significant reduction of switch injection errors in the front-end sensing amplifier, the amplifier stage, and the filter stage while without increasing circuit complexity. Apart from economic means, the INS offers good immunity to process and temperature

variations. This demonstrates its technical merit among the conventional analog switch topologies. Finally, not only does it give an attractive low-cost fully integrated solution for automotive accelerometers, it is very useful for other types of INS-based SC circuits in analog signal processing.

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W. F. Lee was born in Singapore. He received the B.Eng. (Hons), M.Eng., and Ph.D. degrees in electrical and electronic engineering from Nanyang Technological University (NTU), Singapore, in 1996, 1999, and 2006, respectively.

He was an Application Engineer for more than two years in the field of instrumentation and measurement for electronic circuits from 1991 to 1993. He was previously with NTU, but joined the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2006, where he is currently an

Associate Professor with the School of Electronic Engineering. He holds one patent. His research interests include low-power mixed-signal circuit design, high-precision readout circuits and signal conditioning circuits for sensor applications (e.g., MEMS accelerometers and gyroscopes), integrated filters, reference circuits, and data converters.

P. K. Chan was born in Hong Kong. He received the B.Sc. (Hons) degree from the University of Essex, Colchester, U.K., in 1987, the M.Sc. degree from the University of Manchester, Institute of Science and Technology (UMIST), Manchester, U.K., in 1988, and the Ph.D. degree from the University of Plymouth, Plymouth, U.K., in 1992.

From 1989 to 1992, he was a Research Assistant with the University of Plymouth, working in the area of MOS continuous-time filters. In 1993, he joined the Institute of Microelectronics (IME), Singapore,

as a Member of Technical Staff, where he designed CMOS sensor interfaces for industrial applications. In 1996, he was a Staff Engineer with Motorola, Singapore, where he developed the magnetic write channel for Motorola first-generation hard-disk preamplifiers. He joined Nanyang Technological University (NTU), Singapore, in 1997, where he is an Associate Professor with the School of Electrical and Electronic Engineering and Program Director (analog/mixed-signal IC and applications) for the Center for Integrated Circuits and Systems (CICS). He holds five patents and is an IC Design Consultant to local and multinational companies in Singapore. He has also conducted numerous IC design short courses to industrial companies and design centers. His research interests include circuit theory, amplifier frequency-compensation techniques, sensing interfaces for integrated sensors, biomedical circuits and systems, integrated filters, and data converters.