Fully Symmetrical Monolithic Transformer (True 1 : 1) for Silicon RFIC

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Abstract—A novel on-chip transformer configuration that gives an identical inductor pair, a higher individual coil self-resonant frequency (SRF), and excellent area efficiency are presented. This technique involves the unique way of inter-crossing the transformer's primary and secondary coils using multiple metallization layers. Truly symmetrical transformer configuration (100%) is demonstrated using minimum die size. Thus, a true 1 : 1 transformer has been realized on silicon. The effects of the parasitic within the transformer are represented by an equivalent-circuit model. Accurate semiempirical expressions describing the circuit components are provided based on the various layout parameters. Of all the transformer structures presented, the two designs occupying the minimum silicon area by a factor of $> 2\times$ have been selected for performance evaluation of the SRF, coupling coefficient, input impedance, quality factor, and inductance. The transmission line transformer mode has also been studied to examine the designs' performance in the differential mode. The second proposed design reported in this paper, with enhancements in $S21$ and k performance, is created by adding a unique routing technique onto the first proposed structure. The method presented is fully compatible with the standard foundry CMOS processes. The silicon data reported in this study are based on Chartered Semiconductor Manufacturing's 0.13-μm RF CMOS technology node.

Index Terms—Area efficiency, coupling coefficient, differential inductor, fully symmetrical transformer, identical inductor pair, inter-coil crossing, interleaved transformer, multidirectional coupling, RF CMOS, self-resonant frequency (SRF), stacked transformer, system-on-chip (SoC), transmission line transformer (TLT).

I. INTRODUCTION

THE HIGH demand for system-on-chip promotes the interest of integrating on-chip transformers for RF CMOS applications. Due to the physical isolation property of the transformer, it can be easily exploited to implement several functional blocks such as impedance matching, low-noise feedback, differential-to-single-ended conversion, and input differential-mode inductor pair [1]–[4].

In recent years, on-chip transformers have become more profound in high-frequency applications. This is mainly because many RF integrated circuit (RFIC) designers started to integrate transformer blocks with voltage-controlled oscillators (VCOs), power amplifiers (PAs), etc. [5]–[8]. The majority of the research done has shown enhancement in circuit performance
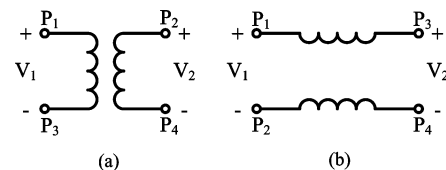
Fig. 1. (a) FL transformer mode. (b) TLT mode.

compared to that of a nontransformer integrated design. In general, the key advantage of using a transformer is the ability to reduce the large silicon area consumption by as high as 50%. This reduction has become a figure-of-merit, as the silicon area is a limiting factor in current and future RFIC designs.

A transformer is primarily designed to couple alternating current from one winding to the other without significant loss of power. Impedance levels between the windings are transformed in the process as the ratio of the terminal voltage to current flow changes across windings. In addition, direct current flow is isolated by the transformer, allowing the windings to be biased at different potentials. A microstrip line is the simplest on-chip element for monolithic implementation of an inductor. Interwinding or overlapping of the microstrip inductors to magnetically coupled independent conductors results in a simple monolithic transformer [3].

Commonly, there are two main types of transformer structure, i.e., the interleaved and stacked transformer, which are widely used in two different transformer modes (i.e., flux-linkage (FL) and transmission line transformer (TLT) mode [9] [refer to Fig. 1(a) and (b)]). Many RFIC designs such as VCOs, low-noise amplifiers (LNAs), and mixers prefer a fully differential architecture in order to suppress common-mode noise. In these circuits, one fully symmetrical passive component can be adopted to replace two asymmetric ones in the differential paths so as to save chip area and cost. Most importantly, by means of the miniaturized symmetric architecture, the effective inductance can be increased by inherent mutual coupling. Usually, the FL transformer is limited to lower frequency applications by its inherent distributed winding capacitance. Thus, the TLT mode is introduced for higher frequency applications. In fact, the TLT mode design requires a pair of fully symmetrical coils. The ideal way of constructing the TLT, using transmission lines, is often too bulky for high inductance applications. The area needed to build a pair of high inductance transmission lines is too large. Therefore, an alternative solution comprised of monolithic transformers has been introduced to realize an on-chip TLT by trading off the bandwidth as compared to the conventional transmission line design.
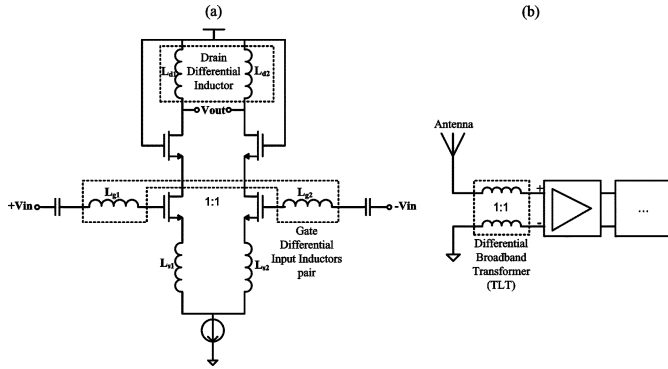
Fig. 2. Fully symmetrical (1 : 1) transformer used as: (a) drain and input differential inductor pairs in simple differential LNA design [15] and (b) input stage of the system as differential broadband transformer in TLT configuration.

Fig. 3. 3-D view of the FST1 and 0.13-μm silicon die photograph.

Fig. 4. (a) Virtual separation of the primary and secondary coil that depicts the fully symmetrical property of the FST1. (b) Layers description of the FST1 based on one of the coils.

Significant efforts have already been reported in the literature that aim at characterizing the existing transformer design [3], [10], [11]. In general, achieving a turn ratio of 1 : n is proven to be relatively simpler than realizing an ideal 1 : 1 fully symmetrical transformer in the monolithic implementation [3]. It is well known that the real world monolithic transformers, be it interwinding or overlapping of the coils, have problems such as the different finite metal line resistances on various backend layers, unmatched finite inductances between the primary and secondary coils, and imperfect power losses, especially with a lossy silicon substrate. With the challenge identified, [12] and [13] have proposed a new type of transformer structure that demonstrates a nearly 1 : 1 ratio design. However, a *True 1 : 1* transformer on-chip has yet to be developed. Some general circuit applications for a fully symmetrical device are shown in Fig. 2. In [14], Kluge *et al.* has highlighted that a symmetric differential inductor is proven to be better in suppressing common-mode signals instead of two single-ended inductors. However, using conventional differential inductor, it does not have true symmetricity property. The coupling coefficient is low and the area consumption is usually very high for large inductance applications. Thus, a fully symmetrical transformer connected as a differential inductor is one of the solutions to this limitation.

The need for a fully symmetrical transformer extends to unconventional circuits as well such as an *LC*-VCO [16]. In [16], it requires an electrically symmetrical structure to form the parallel *LC*-tank that yields identical inductance and resistance values.

In this study, two novel monolithic fully symmetrical transformer designs are proposed and compared with the existing transformer structures. The first proposed design demonstrates better performance in terms of area efficiency, self-resonant frequency (SRF), and symmetry. An equivalent-circuit model that shows good agreement to the measured novel transformer is also reported in this study using accurate geometry-based equations. The tradeoff option between the SRF and $S21$ and k are introduced in the second proposed design, offering more flexibility to RFIC designers.

This paper is organized as follows. In Section II, the detailed introduction for the first proposed fully symmetrical transformer (FST1) is discussed together with its proposed equivalent lumped-circuit model. In Section III, having the
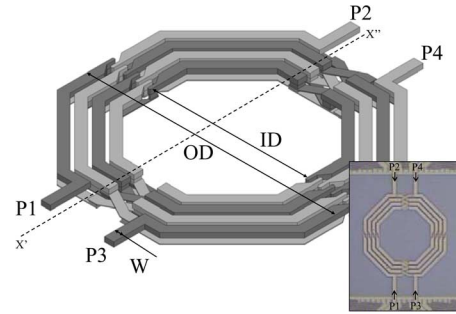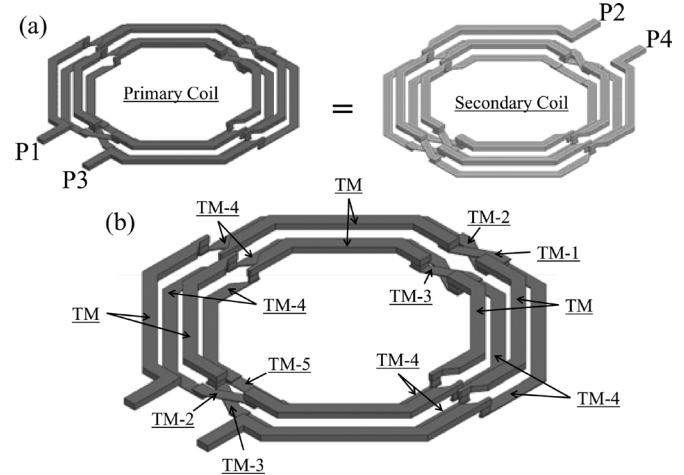
inductance as a benchmark, a silicon area comparison is carried out for all different types of configurations. Subsequently, the transformers are normalized to the smallest device size for performance evaluation based on same on-chip area. In the latter part of Section III, the second proposed fully symmetrical transformer (FST2) is introduced, demonstrating enhancements to the transformer's $S21$ and k performance. Finally, a conclusion is drawn in Section IV.

II. NOVEL FULLY SYMMETRICAL TRANSFORMER

A. Description

The FST1 has its primary and secondary coils inter-crossed, equalizing the physical aspect of the two windings [17]. The concept of the design is based on using several metallization layers as interconnects to achieve inter-coil crossing. Thus, the impedance looking into the two windings are expected to be identical. The 3-D view of the FST1 is depicted in Fig. 3 together with its silicon die photograph.

The structure consists of four segments. Each quadrant will experience a switching from the top layer to the corresponding bottom layer. The fully symmetrical property of the design can be illustrated by virtually separating the two coils from their inter-crossing, as shown in Fig. 4(a). Each coil will be experiencing an equal amount of various metallization layers, while maintaining the same physical length (number of turns, irrespective of the layers). For example, Fig. 4 demonstrates a four-turn
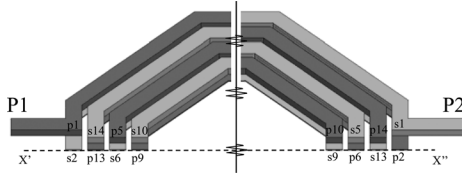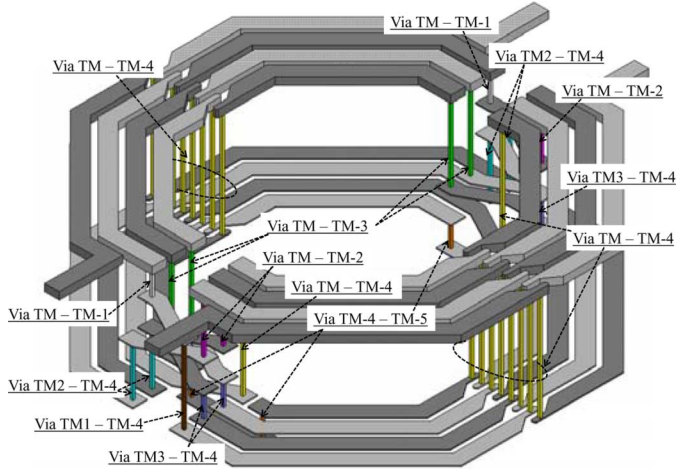
Fig. 5. Cross-sectional view of the FST1 along $X'–X''$, as shown in Fig. 3.

Fig. 6. 3-D exploration view of the FST1 with detail vias mapping.

transformer design with each coil having eight quadrants of both the top and bottom layers. It is clearly visible that the two coils are, in fact, identical. They are integrated with 180° difference in the port orientation.

In the conventional transformer design, the mutual coupling is *unidirectional*, either laterally or vertically. However, in the FST1, a *multidirectional* mutual coupling can be achieved. Fig. 5 illustrates this process using the cross-sectional view of the proposed design along the $X'–X''$ axis. Quadrant s6 is not limited to vertical coupling provided by quadrant p5, it has quadrant p9 and p13 contributing to the lateral coupling. Thus, the mutual coupling of the FST1 is expected to improve. The routing of the design must also ensure the current travels only in one direction within the same coil. This is crucial, as the reverse current will result in a negative self-inductance effect that substantially reduces the overall coil inductance.

The proposed transformer's novel way of inter-coil crossing method, requires six metallization layers as shown in Fig. 4(b). By expanding the 3-D view of the design shown in Fig. 6, it reveals the detailed via mapping of the FST1. The vertical deck of the metal layers is illustrated in Fig. 7. TM and TM-4 are the layers forming the turns quadrant, whereby TM-1, TM-2, TM-3, and TM-5 are used to form underpasses and overpasses for this design. TM being the topmost metal layer and TM-5 being the bottommost layer.

B. Equivalent Lumped-Circuit Model

Generally, a simple two-port lumped-circuit element is sufficient to model all multiport devices, as one or more ports will be grounded in most practical circuit applications. However, for this fully symmetrical device, the model with independently driven terminals is much more appropriate in showing the cred-
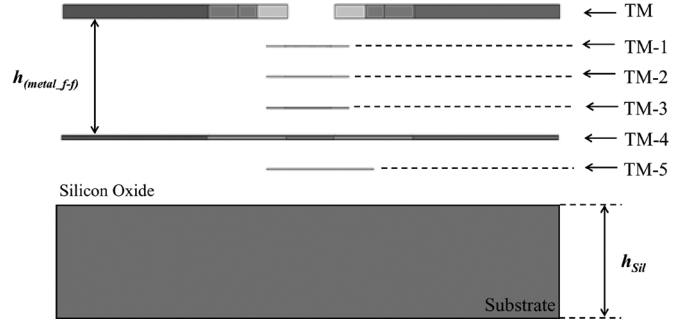

Fig. 7. Vertical metallization profile of the FST1 design.

ibility of the differential mode applications. Fig. 8 illustrates the proposed equivalent lumped-circuit model for the novel design. The electrical model of this design is relatively simpler as compared to the conventional transformer. This is because both winding are identical, requiring only single branch solutions. The proposed design's turns are described by ideal inductors together with resistors in a ladder network, as suggested in [18] and [19]. The magnetic coupling coefficient are modeled in terms of k. The port-to-port capacitive effects from various nodes are captured with $C_{pp,P2-3}$, $C_{pp,P1-4}$, $C_{pp,P1-\mathrm{sec\_ctr}}$, $C_{pp,P2-\mathrm{pri\_ctr}}$, $C_{pp,P3-\mathrm{sec\_ctr}}$, and $C_{pp,P4-\mathrm{pri\_ctr}}$, whereas $C_{\mathrm{ox},P1}–C_{\mathrm{ox},P4}$ models the parasitic capacitance of the device to the silicon substrate. The entire substrate network (silicon area beneath the device) is separated into six blocks of C_{sub} and R_{sub} to better model the distribution effect of the lossy substrate.

1) Series Inductance and Resistance: Extensive effort has been reported in finding an accurate analytical expression for the self-inductance. In this study, a well-known formula suggested by Mohan *et al.* [20] is used as follows in (1):

$$
\begin{aligned}
L_{\mathrm{DC}} &= \frac{\mu \times n^2 \times d_{\mathrm{avg}} \times c_1}{2} \left(\ln\left(\frac{c_2}{\delta}\right) + c_3 \times \delta + c_4 \times \delta^2 \right) \\
d_{\mathrm{avg}} &= \frac{\mathrm{OD} + \mathrm{ID}}{2} \\
\delta &= \frac{\mathrm{OD} - \mathrm{ID}}{\mathrm{OD} + \mathrm{ID}}
\end{aligned}
\tag{1}
$$

where coefficients $c_1–c_4$ has the value of 1, 2.29, 0, and 0.19, respectively. The OD and ID correspond to the outer and inner diameters of the structure.

The series resistance computation is expressed in (2). This formula consists of two main parts: the resistance contributed by the metallization layers and the vias. The huge amount of vias utilization in this design demands a necessity to include via resistance in the ohmic calculation. The technology parameters of the Chartered Semiconductor Manufacturing's 0.13-μm process are summarized in Table I

$$
\begin{aligned}
R_{\mathrm{DC}} &= \rho_{\mathrm{metal}} \times \frac{l_{\mathrm{length}}}{2\left(w_{\mathrm{width}} \times t_{\mathrm{TM\_thickness}}\right)} \\
&+ \rho_{\mathrm{metal}} \times \frac{l_{\mathrm{length}}}{2\left(w_{\mathrm{width}} \times t_{\mathrm{TM-4\_thickness}}\right)} \\
&+ \rho_{\mathrm{via}} \times t_{\mathrm{via\_height}}.
\end{aligned}
\tag{2}
$$

Fig. 8 shows two series $L–R$ branches to model the skin and proximity effects. An analytical equation is suggested in [18].
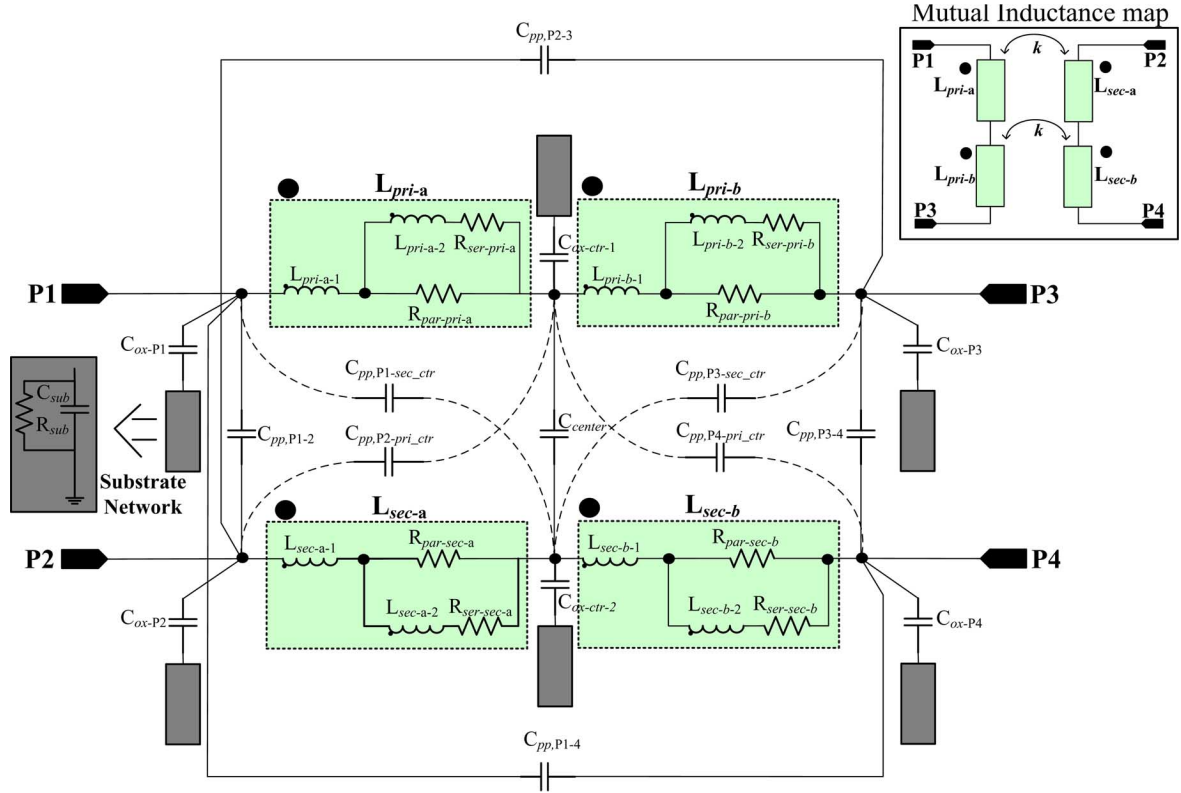
Fig. 8. Equivalent lumped-circuit model for the proposed design.

TABLE I
TECHNOLOGY PARAMETERS FOR 0.13-μm PROCESS

Parameter	Value
Silicon resistivity	10 Ω-cm
Silicon thickness (h_{sil})	150 μm
Silicon dielectric constant	11.9
Top Metal thickness (T_{TM})	3.03 μm
Metal 1-5 thickness (T_M)	0.465 μm
Metal sheet resistivity (ρ_{metal})	26.55 mΩ-μm
Inter-metal oxide thickness	0.42 μm
Eff. Inter-metal dielectric constant	4.2
Eff. Via sheet resistance (ρ_{via})	90 mΩ/μm
Metal Vert. plate-plate separation ($h_{(metal\_f-f)}$)	3.038 μm
Top Metal - Silicon distance ($h_{(TM-Sil)}$)	6.595 μm
Metal 2 - Silicon distance ($h_{(TM-4-Sil)}$)	1.593 μm

However, for SPICE simplicity, Gao and Yu have reported using a semiempirical equation to compute the ladder elements shown as follows in (3) [19]:

$$R_{\text{ser}-\text{pri}-a,b} = K_{Rp} \times R_{\text{par}-\text{pri}-a,b}$$
$$L_{\text{pri}-a-2,\text{pri}-b-2} = K_{Lp} \times L_{\text{pri}-a-1,\text{pri}-b-1}$$
$$R_{\text{par}-\text{pri}-a} = R_{\text{par}-\text{pri}-b} = \left(\frac{1+1}{K_{Rp}}\right) \times \frac{R_{\text{DC}}}{2}$$
$$L_{\text{pri}-a-1} = L_{\text{pri}-b-1} = \frac{L_{\text{DC}}}{[2 + 2K_{Lp} \times (1 + K_{Rp})^{-2}]}. \tag{3}$$

The semiempirical coefficients K_{Rp} and K_{Lp} are held constant for this work, e.g., $K_{Rp} = 1.1$ and $K_{Lp} = 0.3$. The k term indicates the strength of the magnetic coupling between the primary and secondary coils. The use of SiO_x as the isolation median instead of ferromagnetic material results in finite

magnetic losses. The relationship between the k factor and the fabrication parameters can be rather complicated. Alternatively, [10] and [21] proposed a closed-form k expression based on the layout parameters. However, those suggested equations are based on unilateral coupling that underestimate the capability of this novel design. Therefore, a semiempirical geometries-based equation proposed by Mohan *et al.*, expressing the k term as a function of the layout offset, is applied in this study [22]. The d_s suggested are modified to take into account the vertical separation between the primary and secondary coils, as shown in (9)

$$k = 0.9 - \left(\frac{d_s}{d_{\text{avg}}}\right) \tag{4}$$

where $d_s = \sqrt{(\Delta x)^2 + (\Delta y)^2 + (\Delta h)^2}$. In this proposed design, Δx and Δy are zero, as the two windings do not offset in the x- and y-axis. Thus, it can be simplified as $d_s = \Delta h$.

2) Parasitic Capacitances: Beneath the device's lowest metal, there is a series of oxide layers before the silicon–oxide interface. This is described as a parasitic capacitance in the lumped-circuit model. For a passive device, the coplanar dimensions are much larger than the oxide thickness. Hence, the oxide capacitance is proportional to the total area occupied by the device (10)

$$\text{Area} = 8 \times \tan 22.5° \left(\left(\frac{\text{OD}}{2}\right)^2 - \left(\frac{\text{ID}}{2}\right)^2\right) \tag{5}$$

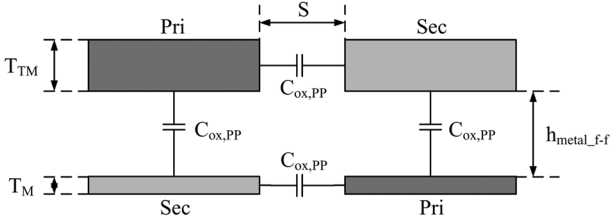$$C_{\text{ox}-\text{pri,ox}-\text{sec}} = \frac{\varepsilon_0 \times \varepsilon_r \times \text{Area}}{2 \times t_{\text{TM}-4-\text{Sil}}}. \tag{6}$$

Fig. 9. Cross-sectional view of the fully symmetrical transformer showing multidirectional electrical coupling.

TABLE II
COMPONENTS VALUE FOR THE PROPOSED DESIGN

Component	Measured value	Computed value	Optimized value
L_{DC-pri}	2.933 nH	2.999 nH	2.999 nH
L_{DC-sec}	2.933 nH	2.999 nH	2.999 nH
R_{DC-pri}	10.074 Ω	9.907 Ω	9.907 Ω
R_{DC-sec}	10.074 Ω	9.907 Ω	9.907 Ω
$C_{pp-overall}$	-	349.23 fF	350 fF
C_{ox-pri}	-	176.69 fF	176.69 fF
C_{sub}	-	18.156 fF	18 fF
R_{sub}	-	522.78 Ω	530 Ω
$C_{pp,P1-sec_ctr}$	-	-	3 fF
k	0.86	0.86	0.86

Fig. 3 shows that $\sim$80% of the trace is part of the main octagonal block. Therefore, the distribution of the oxide capacitance can be expressed as $C_{ox,P1} = C_{ox,P3} = C_{ox,P2} = C_{ox,P3} = 0.1 \times C_{ox-pri}$, whereas $C_{ox-ctr-1} = C_{ox-ctr-2} = 0.8 \times C_{ox-pri}$.

The C_{PP} and C_{center} modeling in this design is slightly different from the conventional transformer. The proposed design's electrical capacitive coupling from one winding to another involves both the vertical and lateral axes, as shown in Fig. 9.

The total vertical overlapping and horizontal length is geometrically computed by

$$l_{vertical} = 8 \times \tan(22.5°)$$
$$\times \left(\sum_{i=1}^{i=N} ID + (2 \times i - 1) \times W + 2 \times (i-1) \times S \right)$$
$$l_{horizontal} = 8 \times \tan(22.5°)$$
$$\times \left(\sum_{i=1}^{i=N} ID + 2 \times i \times W + \frac{(2 \times i - 1) \times S}{2} \right). \quad (7)$$

Subsequently, the overall port–oxide–port capacitance can be derived by substituting the length into the general capacitance (13). The overall port–oxide–port capacitance is distributed across the lumped-circuit model with minimum fitting coefficient, i.e., $C_{pp,P1-2} = C_{pp,P3-4} = 0.1 \times C_{pp-overall}$, $C_{center} = 0.2 \times C_{pp-overall}$, and $C_{pp,P2-3} = C_{pp,P1-4} = 0.3 \times C_{pp-overall}$.

The components $C_{pp,P1-sec\_ctr}$, $C_{pp,P2-pri\_ctr}$, $C_{pp,P3-sec\_ctr}$, and $C_{pp,P4-pri\_ctr}$ are introduced to model the inter-quadrants electrical coupling. However, the derivation is rather complicated. Therefore, an optimization process has been performed on these components using Agilent Technologies' Advanced Design System (ADS) to identify its value. In order to lower the dynamic range for optimization, all these capacitance are set to be equal since this is a fully symmetrical design.

3) Substrate Network: The capacitance C_{sub} models the parasitic capacitive effect between the device and substrate. The area equation based on device's layout parameters (10) is calculated using (13)

$$C_{sub} = \frac{2 \times \varepsilon_0 \times \varepsilon_r \times Area}{h_{sil}}. \quad (8)$$

For the ohmic losses in the substrate, [23] suggested an analytical layout parameter-based equation

$$R_{sub} = \frac{1}{\pi \times \sigma_{sub} \times l_{mean}}$$
$$\times \ln \left[2 \times \coth \left(\frac{\pi \times (W_{dev} + 6 \times h_{TM-4-Sil} + T_M)}{8 \times h_{sil}} \right) \right] \quad (9)$$

where $W_{dev} = (OD - ID)/2$ is the complete width of the coil, and $l_{mean} = 8 \times \tan(22.5°) \times d_{avg}$ denotes the mean perimeter of the device. All the component values are optimized using ADS optimization tools, as shown in Table II. The variation of the optimization is kept to be <1% so as to maintain the credibility of all the proposed semiempirical equations. The model is verified with the measurement data obtained using Agilent Technologies' E8364B PNA network analyzer and physical layer test system (PLTS) on a Cascade S300 probe station. Ground–signal–ground–signal–ground (G–S–G–S–G) type of Infinity probes (pitch: 100 μm) are carefully calibrated using a short, open, load, reciprocal thru (SOLR) on an impedance standard substrate (ISS : 129-239) so as to ensure no measurement errors are brought over to the device data. Figs. 10 and 11 show the transmission and reflection power of the *through* structure with 2-ps delay found in the ISS. The results has demonstrated that the calibration is well performed with minimum transmission loss ($\approx$ 0 dB, refer to Fig. 10) and excellent noise floor (<−60 dB, refer to Fig. 11).

Good agreement between the modeled and measured parameters (*S*-parameters and figure-of-merits) of the device has been achieved. Details measurement techniques and extraction procedure are depicted in Fig. 12.

III. EXPERIMENTAL EVALUATION

A. Existing Transformer Design

The existing transformer designs are studied in this section prior to their performance evaluation. Fig. 13(a)–(c) illustrates the interleaved, stacked, and differential inductor configurations, respectively. Each figure comes with the silicon die photograph based on Chartered Semiconductor Manufacturing's 0.13-μm process. In this study, all the configurations will be standardized to octagonal shape. The closest approximation to a circle is an octagon, which does not violate any design rule.
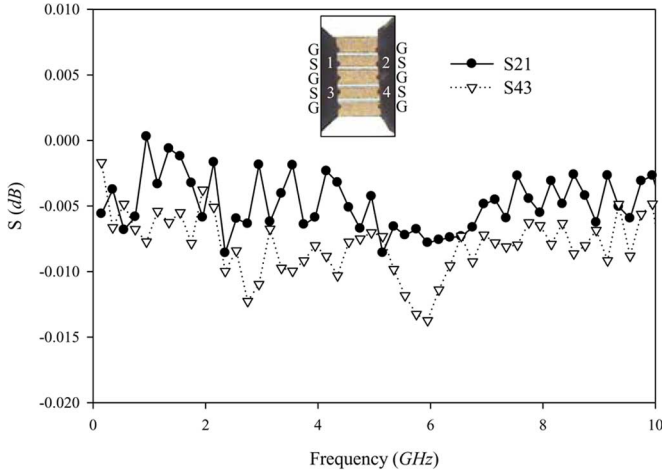
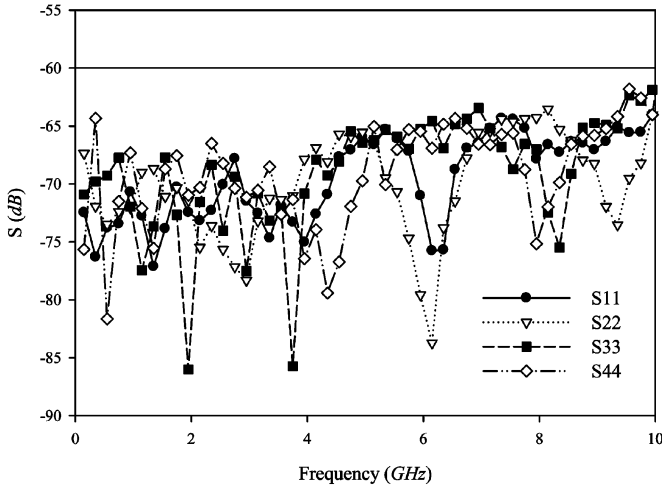Fig. 10.　Transmission power of the 2-ps delay through line.

Fig. 11.　Reflection power of the 2-ps delay through line.

B. Silicon Area Efficiency

To conduct a study on the area efficiency of various configurations, the inductance has been identified as a reference figure-of-merit (15). All the designs are drawn to achieve individual coil inductance of ∼3–3.5 nH, as displayed in Fig. 14. The geometry parameters are tabulated in Table III with the silicon area normalized to the smallest device size (stacked and fully symmetrical design)

$$L_p = \frac{\mathrm{imag}\left(\dfrac{1}{Y_{11}}\right)}{2 \times \pi \times f}. \tag{10}$$

Table III demonstrates that the interleaved and differential inductor occupied more than twice the silicon area as compared to the stacked or the fully symmetrical transformer. Therefore, in order to perform a fair evaluation, these transformers with the smallest silicon area are chosen to be the suitable candidates.

C. Stacked Versus Fully Symmetrical

Stacked and fully symmetrical transformer with the same silicon area of 228.28 μm^2 have been tested. The quality (Q) factor, inductance, coupling coefficient, and $S21$ between the two transformers are compared and discussed in Section III-C.1. The proposed equivalent lumped-circuit model is also tested
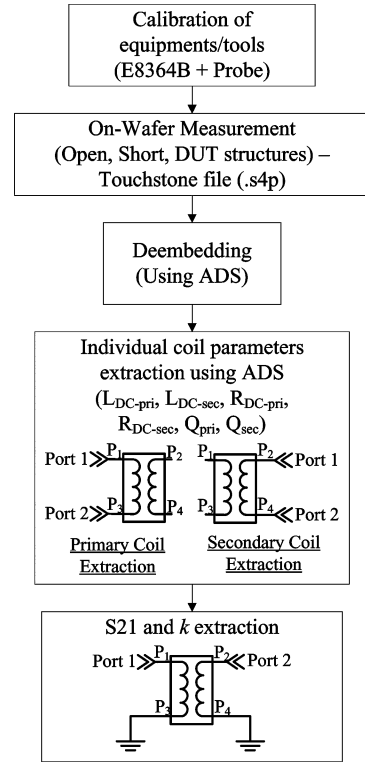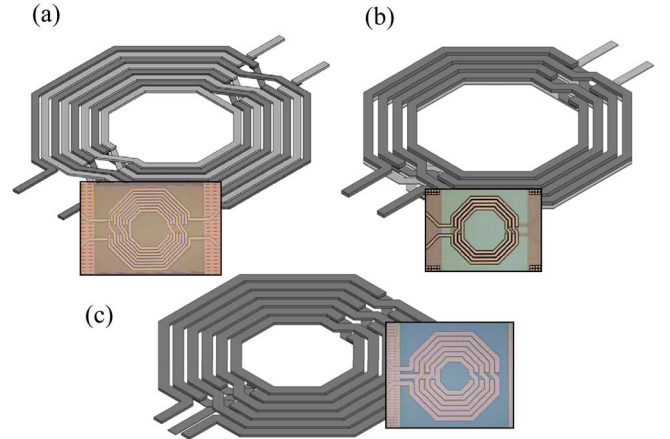

Fig. 12.　Flowchart of the measurement and extraction process.

Fig. 13.　3-D view of the: (a) interleave transformer, (b) stacked transformer, and (c) differential inductor configuration with their respective 0.13-μm silicon die photograph.

against the measured silicon data to demonstrate the ability to achieve good agreement.

1) Q Factor and SRF: The individual Q factors illustrated in Fig. 15 is extracted from (16). During this extraction, the coil of no interest will be isolated (unconnected) so as not to affect the extracted data, i.e., while extracting for Q_{pri}, terminal P1 and P3 will be connected to Port 1 and Port 2 leaving terminal P2 and P4 unconnected; the same method applies for Q_{sec} extraction (refer to Fig. 12)

$$Q_{\mathrm{pri,sec}} = \frac{\mathrm{imag}\left(\dfrac{1}{Y_{11}}\right)}{\mathrm{real}\left(\dfrac{1}{Y_{11}}\right)}. \tag{11}$$
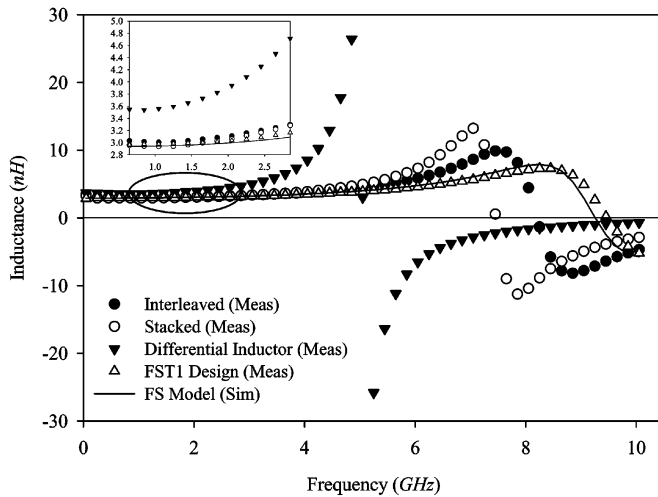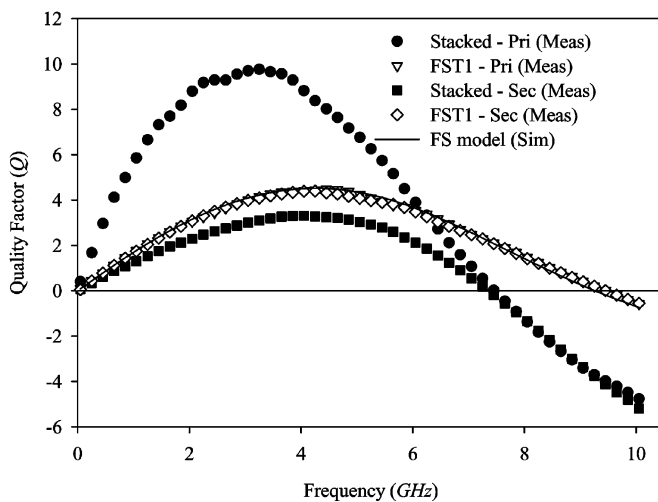
Fig. 14. Inductance plot of the various transformer configurations.

TABLE III
LAYOUT PARAMETERS OF THE VARIOUS TRANSFORMERS

Design	ID (μm)	W (μm)	N	OD (μm)	Area (μm^2)	Norm Area
Interleaved	100	6	4	238	469.25	2.06
Stacked	100	6	4	160	228.28	1
Differential	100	15	6	310	796.12	3.49
Fully symmetrical	100	6	4	160	228.28	1

Fig. 15. Q factor plot of the stacked and FST1 design.

The outcome for the FST1, in term of the Q factor, does not show any advantage as compared to the primary (topmost) coil of the stacked transformer, and it does exhibit excellent symmetry between the two windings. In fact, the resulting lower individual Q factor for the proposed transformer is due to the mixture of multiple thick and thin metal quadrants. Thinner metal layers (t) has higher ohmic losses, shown as follows in (12):

$$R = \rho \times \frac{length}{width \times thickness}. \tag{12}$$

For the same reason, the stacked transformer's secondary winding demonstrates a much lower Q factor of < 4. The data has clearly shown that the stacked's primary winding is able
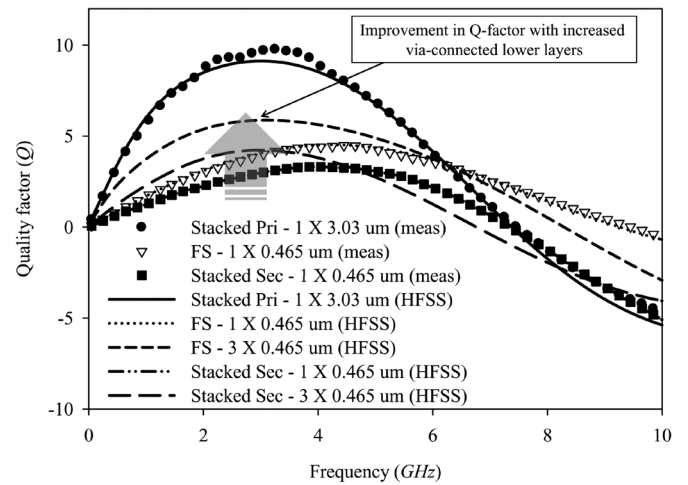
Fig. 16. Q factor plot of the ordinary FST1 design, stacked design, and the FST1 design with via-connected three lower metal layer, together with the respective HFSS simulation result.

to achieve a high Q factor, its secondary winding exhibits a much poorer asymmetrical performance. This asymmetricity will cause degradation in the circuit performance, especially for a differentially driven design. Majority of the practical RF circuits require inductors/transformers to have a higher Q factor, but there are certain parts of the circuit that do not really require a high-Q factor, i.e., see Fig. 2(a) [15]—the drain inductors and source inductors can be replaced by a fully symmetrical transformer configured as differential inductors as this portion of the design demands the device to be fully symmetrical instead of having a higher Q factor.

Nonetheless, it is still plausible to mitigate the low-Q factor drawback faced by the proposed design using physical layout optimization. The top metal has a thickness of 3.03 μm, which is more than six times thicker than the lower layers (0.465 μm). By increasing the thickness of the bottom layer that is formed by via-connected multiple layers of lower metal, the effective real term of the coil's impedance $\mathrm{real}(1/Y_{11})$ will decrease. To justify this argument, simulation has been performed using Ansoft's High Frequency Structure Simulator (HFSS). The HFSS simulation profile is calibrated to the Chartered's 0.13-μm technology so as to ensure that the results obtained are credible. The calibrated HFSS has demonstrated an excellent matching on the comparison of the simulated ordinary FST1 design (FS $- 1X0.465\,\mu$m metal layer thickness) and the stacked design with its measured silicon data, as shown in Fig. 16. The 3-D view of the FST1 design with a via-connected three lower metal layer is illustrated in Fig. 17. In Fig. 16, the HFSS simulation demonstrates that with the increase of the effective thickness of the lower metal layers, a higher Q factor can be achieved. The inductance plot shown in Fig. 18 illustrates that the Q improvement technique does not affect the dc inductance value of the device. In contrast, the SRF of the individual coil has dropped. This reduction is attributed to the shortening of the distance between the two coils, which increases the distributed winding capacitance. (i.e., $h_{\mathrm{before}} > h_{\mathrm{after}}$, as displayed in Fig. 17). On top of that, Danesh et al. has also suggested that a microstrip winding driven differentially gives a higher Q factor and broader bandwidth than a single-ended terminal [24].
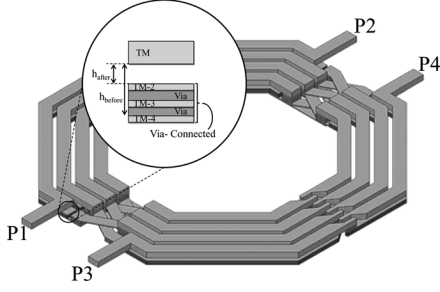
Fig. 17. 3-D view of the FST1 design with via-connected three lower metal layer.
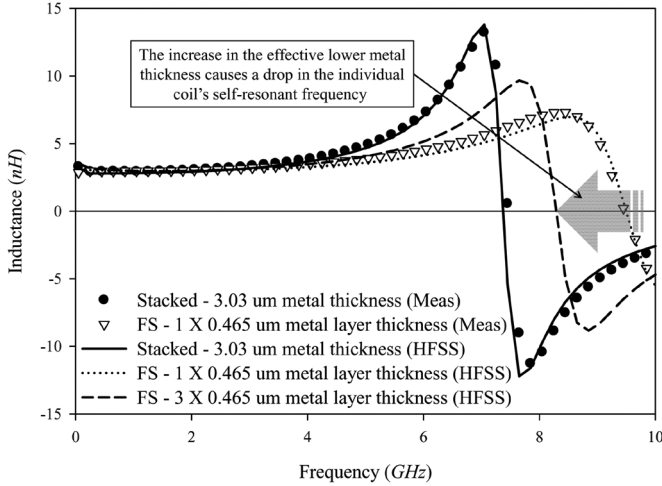

Fig. 18. Inductance plot of the ordinary FST1 design, stacked design, and the FST1 design with via-connected three lower metal layer, together with their respective HFSS simulation result.

The individual SRF (f_{SRF}) demonstrated by the FST1 design shows a significant improvement as compared to the stacked transformer depicted in Figs. 14 and 15, i.e., the stacked transformer's $f_{\mathrm{SRF}} = 7.5$ GHz and the FST1 design's $f_{\mathrm{SRF}} = 9.5$ GHz. This increment in f_{SRF} can be attributed to the larger separation of the winding's vertical plate-to-plate distance ($h_{(\mathrm{metal\_f-f})}$). The stacked transformer is formed using TM and TM-2, whereas the new design uses TM and TM-4 layers. The increment in the separation causes an decrease in capacitance, which translates to higher f_{SRF}. In order to model the individual SRF (f_{SRF}) of the proposed design, a modification to Zhou and Allstot's differential SRF equation in [2] is used, as shown in (13). The individual SRF is extracted with the coil of no interest unconnected. This is to isolate the mutual coupling effect that causes the individual coil inductance to change (e.g., while extracting primary coil, the secondary coil is unconnected). Based on the novel inter-coil crossing method, the oxide height of each proposed winding is not constant throughout. Thus, an average oxide height [refer to (14)] is needed to determine the effective oxide capacitance ($C_{\mathrm{ox-avg}}$) using (13) as follows:

$$f_{\mathrm{SRF}} = \frac{1}{2 \times \pi \sqrt{L \times C_{\mathrm{ox-avg}}}} \left(1 - \frac{R_{\mathrm{DC}}^2 \times C_{\mathrm{ox-avg}}}{L} \right)^{0.5} \quad (13)$$

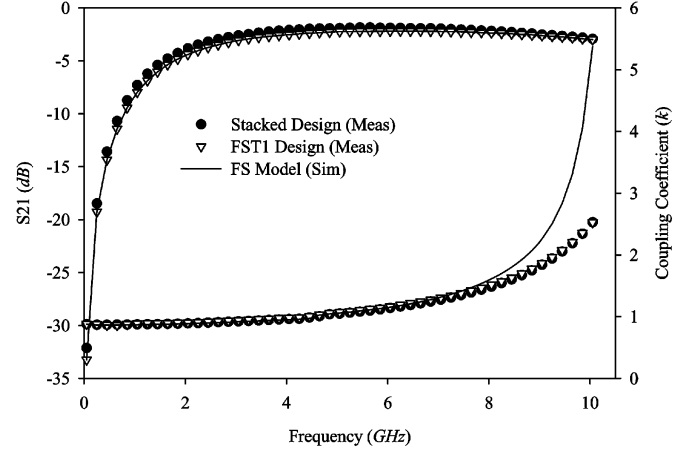$$h_{\mathrm{ox-avg}} = \frac{h_{\mathrm{TM-Sil}} + h_{\mathrm{TM-4-Sil}}}{2}. \quad (14)$$

Fig. 19. $S21$ and coupling coefficient (k) plot of the stacked and FST1 designs.

Based on (13), the computed $f_{\mathrm{SRF-model}}$ is 9.483 GHz and the extracted $f_{\mathrm{SRF-meas}}$ is 9.5 GHz (see Fig. 15). It can be concluded that the equation is able to predict the SRF of the proposed design with less than 0.2% error.
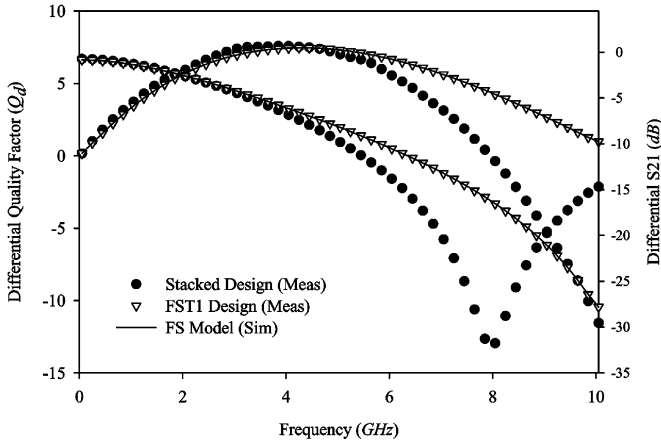
2) $S21$ and Coupling Coefficient (k): Lastly, the most critical figure-of-merits, $S21$—transmission gain and k—are addressed. Both transformers are connected in a two-port configuration to evaluate the ability to transfer power ($S21$) and its magnetic strength (k) from one winding to another. The schematic connection of the transformers is shown in the $S21$ and k extraction block of Fig. 12. The magnetic coupling coefficient is extracted using (9). Both $S21$ (in decibels) and k are plotted in Fig. 19

$$k = \sqrt{\frac{\mathrm{imag}(Z_{12}) \times \mathrm{imag}(Z_{21})}{\mathrm{imag}(Z_{11}) \times \mathrm{imag}(Z_{22})}}. \quad (15)$$

These two parameters are considered the most fundamental requirements in transformer design. In Fig. 19, the FST1 is able to attain the same comparable transmission power as the stacked transformer, having $S21 < 5$ dB. However, the FST1 shows a slight improvement in the k value as compared to the stacked transformer, i.e., the stacked transformer has $k = 0.82$ and the FST1 has $k = 0.86$. The enhancement demonstrated by the novel inter-coil crossing method is not drastic, as it does not allow the coils to have maximum overlapping surface area (which is needed to facilitate the quadrants crossing shown in Fig. 4). Nevertheless, the comparison with the stacked transformer that has the highest k value (having the largest coil overlapping surface area) ever reported demonstrates that although the proposed design does not geometrically favor its k value, it is still able to attain a comparable value with slight improvement. The above finding has proven that this unique way of connecting the coils is both electrically and magnetically effective.

3) Differentially Driven TLT Mode: In this section, the proposed and stacked designs are tested in the differentially driven TLT mode shown in Fig. 1(b). The differential data can be extracted using PLTS (as touchstone (.s2p) file) or standard

Fig. 20. Differential Q and $S21$ of the stacked and FST1 design in TLT mode.
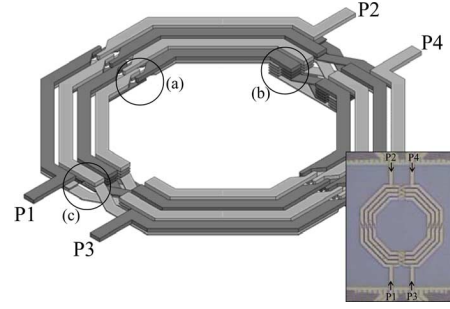

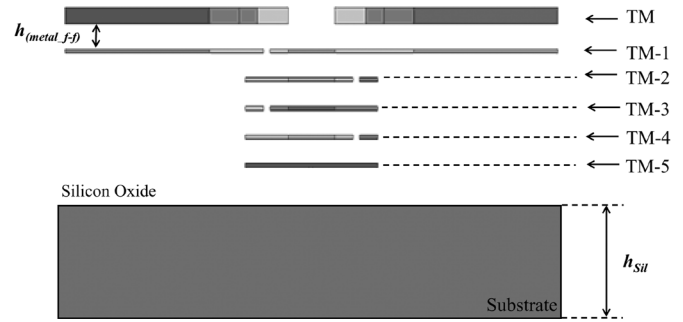Fig. 21. 3-D view of the FST2 design using the top two metal layers to enhance the transmission power.

Fig. 22. Cross-sectional view of the second proposed transformer design using the top two metal layers to enhance the transmission power.

single-ended to differential mode conversion method (16) as follows:

$$S_{D11} = 0.5 \times (S11 - S21 + S12 - S22)$$
$$S_{D12} = 0.5 \times (S13 - S23 + S14 - S24)$$
$$S_{D21} = 0.5 \times (S31 - S41 + S32 - S42)$$
$$S_{D22} = 0.5 \times (S33 - S43 + S34 - S44). \qquad (16)$$

The differential performance (Q_d and S_d21) are taken using (16) and plotted in Fig. 20. The result has shown that the proposed design is suitable for higher frequency band applications as compared to the stacked design. Based on Fig. 20, it shows that the stacked design's differential $S21$ rolls off rapidly after 5 GHz and reaches its self-resonant point at ≈ 8 GHz. On the other hand, the proposed design is able to attain a more gradual rolloff in its transmission loss (S_d21) with its SRF at 10 GHz. This is to say that the proposed design is able to achieve 2 GHz more operating frequency than the stacked design at no additional cost. Looking into the differential Q performance plot (see Fig. 20), it has proven that the symmetricity is an important aspect in differential application. The single-ended Q factor of the stacked's primary coil (refer to Fig. 15) has been reduced by its asymmetric secondary coil. Thus, the stacked design has experienced a lower differential Q value shown in Fig. 20. On the other hand, the proposed design (with a fully symmetrical structure) has further boosted the differential Q value comparable to that of the stacked design. In general, the proposed design is expected to perform even better with a higher individual coil's Q value. This can be achieved based on the discussion in Section III (Q factor and SRF).

4) Enhancement to the Proposed Design: The FST1 shows improvement in the k value, f_{SRF}, and better area efficiency. However, the transmission power ($S21$) illustrated in Fig. 19 is only able to achieve a similar value to that of the stacked transformer. It is because the proposed design's primary and secondary coil vertical plate-to-plate distance has become further apart. This physical implementation reduces the electrical coupling capability. To demonstrate the ability to achieve higher transmission gain, the FST1 design has been enhanced by shifting the lower metal quadrants from TM-4 to TM-1, as
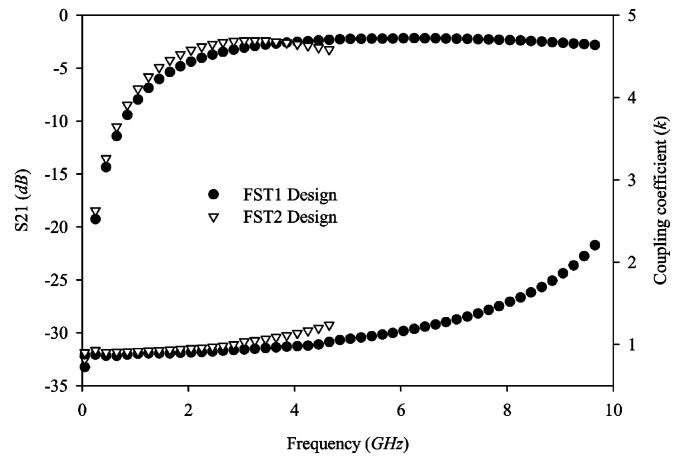
Fig. 23. Measured $S21$ and coupling coefficient (k) plot of the FST1 and FST2 designs.

shown in Fig. 21, the 3-D view of the second proposed design (FST2). The vertical profile of the second proposed design is depicted in Fig. 22.

Fig. 21(a) and (c) presents the narrowing of the inter-coil plate-to-plate distance. Fig. 21(b) shows the rerouted traces from the lower metal layer (TM-4) to the higher one (TM-1).

The performance parameters of the FST2 design are plotted in Fig. 23. It has demonstrated improvement in terms of the transmission gain, up to a frequency band of 4 GHz. In Fig. 23, at 2 GHz, the $S21$ value of the first design is -4.4 dB and the second design has a $S21$ of -3.29 dB. The high frequency response of the $S21$ starts to roll off rapidly after 4 GHz. This phenomenon is caused by the intensive electrical coupling within
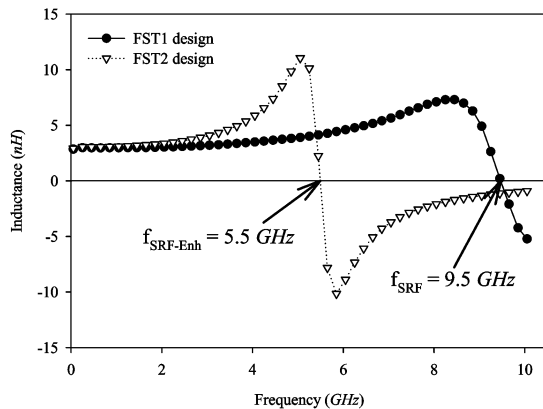
Fig. 24. Measured inductance of the FST1 and FST2 designs reflecting the drop in the f_{SRF}.

the coils that induced high leakage in high-frequency applications. Concurrently, the plot also displays an increase in the k value. It has risen from $k_{1st} = 0.86$ to $k_{2nd} = 0.9$.

There is a tradeoff point for this enhancement technique. The increase in the electrical capacitive effect results in a reduction of the individual coil SRF (f_{SRF}), as revealed in Fig. 24. The FST2 design's f_{SRF} drops from 9.5 GHz, for the FST1 design, to 5.5 GHz. This is caused by the large distributed shunt capacitance that dominates the oxide–substrate capacitance. Although fabricating an ideal $1:1$ fully symmetrical design is now feasible, the realization of a $1:n$ (where $n \gg 1$) transformer design that uses the minimum silicon area is still a challenge. In [25] and [26], the authors have reported that an extremely high turn ratio monolithic transformer design is also plausible.

IV. CONCLUSION

An area efficient fully symmetrical transformer has been developed. Compared to the existing transformers, the new design is able to achieve higher SRF without much degradation in the other device performance at no additional cost. The full symmetry feature of the design has been investigated and confirmed with measured silicon data. The proposed design has also proven that a fully symmetrical design is able to produce a better Q factor in differential applications. In addition, the novel transformer configuration has opened another means of creating an identical inductor pair without expending on the expensive silicon area. The second proposed design has offered RFIC designers a choice between higher f_{SRF} and better $S21$. The credibility of the semiempirical equations introduced in this study have been verified with measurement data based on Chartered Semiconductor Manufacturing's 0.13-μm process.

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