Complex shaped on-wafer interconnects modeling for CMOS RFICs

Shi, Xiaomeng; Yeo, Kiat Seng; Ma, Jianguo; Do, Manh Anh; Li, Erping

2008

Shi, X., Yeo, K. S., Ma, J. G., Do, M. A., & Li, E. (2008). Complex Shaped On-Wafer Interconnects Modeling for CMOS RFICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 16(7), 922-926.

<https://hdl.handle.net/10356/93083>

<https://doi.org/10.1109/TVLSI.2008.2000445>

© 2008 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder. <http://www.ieee.org/portal/site> This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

Transactions Briefs

Complex Shaped On-Wafer Interconnects Modeling for CMOS RFICs

Xiaomeng Shi, Kiat Seng Yeo, Jian-Guo Ma, Manh Anh Do, and Erping Li

Abstract—A model development methodology for complex shaped on-wafer interconnects is presented. The equivalent circuit of the entire interconnect is obtained by cascading basic subsegment models. The extracted parameters are formulated into empirical expressions. Thus, the proposed model can be easily incorporated with commercial electronic design automation (EDA) tools. The accuracy of the model is validated by the on-wafer measurements up to 20 GHz.

Index Terms—CMOS radio frequency integrated circuits (RFICs), equivalent circuit model, interconnects, on-wafer measurements.

I. INTRODUCTION

The recent decade has witnessed the growing interests in radio frequency integrated circuits (RFICs). As the operating frequency reaches RF spectrum, the interconnect has become one of the most crucial factors affecting the performance of the RFICs [1]. Thereafter, incorporating the interconnect into the RFIC design flow becomes increasingly essential. Thus, there is an urgent demand for precise and simple interconnect models which can be implemented into conventional electronic design automation (EDA) tools.

In order to develop desired interconnect models, there are mainly three stages to follow. First, the model structure has to be established. The main challenge in this stage is that the interconnect becomes frequency-variant at high frequencies [2]. Furthermore, most of the models reported in the literature are for straight-line interconnects [2], [3]. However, the interconnect shapes on a real chip are much more complicated. Interconnect models which handle straight lines only are far from sufficient. In this work, a lumped equivalent circuit model for complex shaped interconnect is proposed. It is capable of characterizing frequency-variant behaviors with frequency-independent components, hence can easily be implemented in any standard simulators such as SPICE. Second, after model construction, it comes to the stage of parameter extraction. Finally, the proposed model should be verified with on-wafer measurements to ensure accuracy.

In this work, interconnect test structures with various physical shapes are designed and fabricated employing a Chartered Semiconductor Manufacture Ltd. (CHRT) 0.18- μm RF CMOS technology. On-wafer measurements of S -parameters up to 20 GHz are used to verify the proposed interconnect model.

Manuscript received November 27, 2006; revised June 22, 2007 and August 10, 2007.

X. Shi, K. S. Yeo, and M.A. Do are with the Center for Integrated Circuits and Systems, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: xmshi@ntu.edu.sg).

J.-G. Ma is with the School of Electronic Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu 610054, China (e-mail: jgma@uestc.edu.cn).

E. Li is with the Institute of High Performance Computing (IHPC), Singapore 117528 (e-mail: eplee@ihpc.a-star.edu.sg).

Digital Object Identifier 10.1109/TVLSI.2008.2000445

Fig. 1. Fabricated interconnect test structures: interconnects with bends. (a) Interconnects with 45° bends. (b) Interconnects with 90° bends.

This paper is organized as follows. Section II interprets the proposed approach for the interconnect model development in detail. Section III presents the model parameter extraction. Section IV lists the extracted parameters and the formulated empirical expressions. Verifications are also given in this section. Finally, this paper is summarized and concluded in Section V.

II. MODEL DEVELOPMENT SCHEME

A. Test Structure Design and Measurement

In order to develop interconnect models with silicon verified accuracy, this work is based on on-wafer measurements of test structures. Since the top metal layer is commonly allocated for routing critical high frequency paths [2], the test structures are designed and fabricated on the top metal layer.

The top view of the fabricated test structures is illustrated in Fig. 1. Since 45° bends and 90° bends are most commonly used in RFICs, these two angles are selected for the test structures. The total length of the test structures is fixed as $300\ \mu\text{m}$, while the widths vary from 3, 5, 10, and $20\ \mu\text{m}$. Open structures [2] are employed for de-embedding purpose.

After fabrication, a Cascade Microtech Probe Station and a HP 8510C Vector Network Analyzer are employed for on-wafer S -parameter measurements from 50 MHz to 20 GHz. Then, the Y -parameter-based de-embedding [2] is carried out to exclude the parallel parasitics, while with the aid of an electromagnetic (EM) simulator (HFSS), series parasitics of the pads are extracted and de-embedded from the measurements.

B. Proposed Development Methodology of the Interconnect Model

According to the physical configuration of the test structures in Fig. 1, the whole trace of the interconnect can be divided into different sub-segments, i.e., straight-line segments and corner segments. The structure analysis and nomenclatures are given in Fig. 2. Herein, the model development methodology can be proposed. First, a complex shaped interconnect is decomposed into sub-segments, as shown in Fig. 3. Second, equivalent circuit models are developed for these

Fig. 2. Structure analysis of interconnect with bends.

Fig. 3. Schematic block model of interconnect with bends.

Fig. 4. Proposed equivalent circuit model of straight line segment.

sub-segments. Last, the sub-segments are cascaded forming the model of the entire interconnection.

C. Straight-Line Segment

The proposed equivalent circuit model for the straight-line segment is shown in Fig. 4. This lumped model is capable of characterizing frequency-variant high frequency effects with frequency independent components. Details of the straight-line interconnect model can be found in our previous work [2]. In [2], model parameters of straight-line interconnects are extracted directly from on-wafer measurements of the test structures. The extracted parameters are summarized as empirical functions of the length and width. Therefore, with every set of the length and the width, S -parameters of that straight-line interconnect are computable.

D. Corner Segment

The lumped equivalent circuit model for microstrip bends has been introduced in [4]. However, that model cannot sufficiently characterize the lossy substrate of the CMOS process, which is currently widely used for RFIC designs.

Based on the understanding of the physical structure, a T-network as shown in Fig. 5 is proposed for the interconnect bends of CMOS processes by adding the substrate effects.

At the corner, the current's flow in the conductor is distributed unevenly such that most of the flows crowd at the inner edge [4]. Hence, the resistance reduces. Given the sheet resistance of straight lines to be R_{square} , the sheet resistance of the corner is approximately $0.6 \times R_{\text{square}}$ [5]. Additionally, considering the relative smaller physical size compared with the straight line, R_b in the series branch can be removed. Thus, the model can be further simplified as shown in Fig. 6.

Fig. 5. Modified equivalent circuit model of corner segment.

Fig. 6. Simplified equivalent circuit model of corner segment.

E. Cascading of Sub-Segments

Herein, the construction for the model of the complex-shaped interconnects seems quite straightforward. However, simply connecting the sub-segments together will not lead to a precise model. The reason is that the inductance of a curved interconnect does not equal the sum of the inductance of each straight-line sub-segment. Due to the mutual inductance constellation of different sub-segments, the general trend is that the larger curvature an interconnect has the smaller is the inductance [6]. Consequently, in order to characterize this effect, the series inductance in the Π -network of the straight-line segments which is connected to the corner segment should be modified. Hence, an additional parameter α ($0 < \alpha < 1$), which is multiplication factor, is introduced to represent this variation of the inductance. In Fig. 3, the segments to be modified are highlighted as shaded boxes, i.e., inductance L_s in the second Π -network of *Straight-line Segment 1*, L_s in both of two Π -networks of *Straight-line Segment 2* and L_s in the first Π -network of *Straight-line Segment 3* are multiplied with the multiplication factor α . As for the shunt blocks of the straight-line segments, the influences of the corner can be omitted, so the parameters are kept unchanged.

III. MODEL PARAMETER EXTRACTION

The problem of the parameter extraction of this work can be formulated as an objective function.

As shown in Fig. 2, three straight-line segments and two corner segments are cascaded in a sequence. In order to get the ABCD matrix of the whole trace, five corresponding ABCD matrixes of each segment should be multiplied accordingly, as presented in the following:

$$T_{\text{wire}} = T_{\Pi} \cdot T_{\Pi\text{corner}} \cdot T_{\text{corner}} \cdot T_{\Pi\text{corner}} \cdot T_{\Pi\text{corner}} \cdot T_{\text{corner}} \cdot T_{\Pi\text{corner}} \cdot T_{\Pi} \quad (1)$$

where T_{Π} denotes the ABCD matrix of each Π -network of the equivalent circuit model in Fig. 4, $T_{\Pi\text{corner}}$ denotes the ABCD matrix the corner influenced Π -network and T_{corner} denotes the ABCD matrix of the corner segment.

T_{corner} can be derived as functions of the circuit components L_b , R_b , and C_b , as presented in the following:

$$T_{\text{corner}} = \begin{bmatrix} 1 + \frac{j\omega L_b}{j\omega C_b + R_b} & 2j\omega L_b - \frac{\omega^2 L_b^2}{j\omega C_b + R_b} \\ \frac{1}{j\omega C_b + R_b} & 1 + \frac{j\omega L_b}{j\omega C_b + R_b} \end{bmatrix} \quad (2)$$

T_{II} can be described in (3)–(7)

$$T_{II} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (3)$$

where

$$A = 1 + \frac{j\omega C_{ox} \left(j\omega C_{sub} + \frac{1}{R_{sub}} \right) \left(j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (4)$$

$$B = j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \quad (5)$$

$$C = \frac{2j\omega C_{ox} \left(j\omega C_{sub} + \frac{1}{R_{sub}} \right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} + \left(j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \right) \left[\frac{j\omega C_{ox} \left(j\omega C_{sub} + \frac{1}{R_{sub}} \right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \right]^2 \quad (6)$$

$$D = 1 + \frac{j\omega C_{ox} \left(j\omega C_{sub} + \frac{1}{R_{sub}} \right) \left(j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \right)}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (7)$$

The previous matrix elements presented in (3)–(7) are for a Π -network without the corner influence. The corner-influenced Π -network $T_{IIcorner}$ is similar to T_{II} , just replacing the item L_s with $\alpha \cdot L_s$ to account for the corner effect.

By using the obtained formulas mentioned in Section II-C, values of all components in the straight-line segment can be calculated. Thereafter, the ABCD matrix of the entire complex shaped interconnect can be interpreted as functions of L_b , C_b , R_b , and α . Consequently, corresponding S -parameters can be expressed in functions of these variables with the aid of the ABCD to S -parameter transform formulas.

The proposed objective function $F_0(X)$ can then be obtained as

$$F_0(X)|_{X=(\alpha, L_b, C_b, R_b)} = \sum_{i=1}^m (f_{1i}^2(X) + [f_{1i}(X) - F_{1mean}]^2 + f_{2i}^2(X) + [f_{2i}(X) - F_{2mean}]^2) \quad (8)$$

where m is the total number of the frequency points under consideration. f_{1i} is the error between the simulated S_{11} and those corresponding ones acquired from measurement results at each frequency point i . It is stated in (9). f_{2i} is the error between the simulated S_{21} and the measurement results at each frequency point i , which is stated in (10). F_{1mean} and F_{2mean} are the mean errors of S_{11} and S_{21} at each frequency point i , respectively, as illustrated in (11) and (12). Given the symmetry of the interconnect test structure, it is known that $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$ [7]. Therefore, we use the average value of measured S_{11} and S_{22} , S_{12} and S_{21} in the following steps, denoted as S'_{11} and S'_{21} , respectively

$$f_{1i}(X) = \frac{S_{11-i-simulated} - S'_{11-i-measured}}{S'_{11-i-measured}} \quad (9)$$

$$f_{2i}(X) = \frac{S_{21-i-simulated} - S'_{21-i-measured}}{S'_{21-i-measured}} \quad (10)$$

$$F_{1mean} = \frac{\sum_{i=1}^m f_{1i}(X)}{m} \quad (11)$$

$$F_{2mean} = \frac{\sum_{i=1}^m f_{2i}(X)}{m} \quad (12)$$

The optimization algorithm used in [2] is applied to search for the optimal model parameters, i.e., L_b , C_b , R_b , and α , which can minimize

TABLE I
EXTRACTED PARAMETERS OF THE CORNER SEGMENT

Parameter	W=3(μ m)	W=5(μ m)	W=10(μ m)	W=20(μ m)
45°	L_b (pH)	18.7	19.4	22.1
	C_b (fF)	12.3	18.6	27.9
	R_b (k Ω)	99.5	82.3	61.2
	α	0.86	0.86	0.86
90°	L_b (pH)	17.8	18.1	21.1
	C_b (fF)	15.8	20.1	29.4
	R_b (k Ω)	92.1	78.3	50.0
	α	0.80	0.80	0.80

TABLE II
COEFFICIENTS OF EXPRESSIONS FOR 45° BENDS

Coefficient	L_b	C_b	R_b
a	1.828E1	-1.055E1	7.710E1
b	5.087e-2	-1.144E-2	-2.502
c	-1.266E-3	1.331E1	8.949E1

TABLE III
COEFFICIENTS OF EXPRESSIONS FOR 90° BENDS

Coefficient	L_b	C_b	R_b
a	3.647	1.092E1	1.152E2
b	4.994	1.379	-7.894
c	1.650E1	2.512E-1	4.365E-2

the objective function $F_0(X)$. The returned component values are the optimized set that makes the simulation results fit the measurement data best.

IV. EXTRACTION RESULTS AND MODEL VERIFICATIONS

A. Extraction

The extracted model parameters are summarized in Table I. It is observed that α is always smaller than 1. The value of α of 90° corner segment is smaller than that of 45° corner segment. This can be explained as stated in Section II-E that the multiplication parameter applied to L_s is introduced to characterize the inductance reduction which is a result of the mutual inductance cancellation of different sub-segments. The general trend is that the larger curvature an interconnect has, the smaller the inductance is. Hence, α should be always smaller than 1 and reversely proportional to the curvature of the interconnect.

B. Formulation

Empirical formulas of the model parameters are summarized as functions of design parameters. Thus, provided with the geometrical information, characteristics of the complex shaped interconnect can be obtained by following the algorithm presented in Section II. The empirical formulas of the straight-line segment can be found in our previous work [2]. Formulas of the corner segment are listed in the following. The formulated expressions for the 45° bends are defined in (13)–(15). The corresponding coefficients are shown in Table II. Equations (16)–(18) are expressions for the 90° bends. The coefficients are presented in Table III

$$L_b = a + bW^2 + cW^3 \quad (13)$$

$$C_b = a + bW^{2.5} + cW^{0.5} \quad (14)$$

$$R_b = a + bW + cW^{-1} \quad (15)$$

$$L_b = a + bW^{0.5} + cW^{-1} \quad (16)$$

Fig. 7. Comparisons of interconnects with 45° bends. (a) Comparisons between simulated and measured magnitude. (b) Comparisons between simulated and measured phase.

$$C_b = a + bW^{1.5} + cW^2 \quad (17)$$

$$R_b = a + bW + cW^{2.5}. \quad (18)$$

C. Verification

Simulations of the proposed model are performed using MATLAB. Since $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$ [7], only S_{11} and S_{21} are compared here. The simulated S -parameters are compared with the corresponding measured ones. Four different dimensions of the test structures are examined in the simulation as described in Section III-A. The lengths are fixed at 300 μm. The widths range from 20, 10, 5, and 3 μm.

Fig. 8. Comparisons of interconnects with 90° bends. (a) Comparisons between simulated and measured magnitude. (b) Comparisons between simulated and measured phase.

From Figs. 7 and 8, satisfactory agreements between the simulated S -parameters and the measurement results over the whole frequency range have been achieved. The error is less than 9%. It demonstrates that the proposed model and the extracted parameters are capable of accurately characterizing the on-wafer interconnect with bends over a large range of frequencies up to 20 GHz. In Figs. 7 and 8, simulation results by using straight-line interconnect model in Fig. 4 are also plotted. Values of model parameters are obtained from empirical formulas [2] with the total length (l) and width (W) of the interconnects with bends ($l = 300 \mu\text{m}$, $W = 3 \mu\text{m}$, $10 \mu\text{m}$, and $20 \mu\text{m}$). From Figs. 7 and 8, it is clear that the straight-line interconnect model is not adequate to

model interconnect with bends. Hence, the proposed cascading method is more appropriate.

It is important to note that the given formulas of the model parameters are fit to our specific test chip and process. Moreover, these formulas are only valid within a geometrical range, which is within the coverage of our test structures. For the corner segments, the valid range for the width is from 3 to 20 μm and the angles are 45° and 90° . However, as stated in Section II-A and [2], most of the on-wafer interconnects used in RFICs are within this range.

V. CONCLUSION

An equivalent circuit model is proposed for real case on-wafer CMOS RFIC interconnects. The equivalent circuit of the entire complex shaped interconnect is obtained by cascading basic sub-segment models according to the physical structure. The model parameters are extracted from the on-wafer S -parameter measurements and formulated into empirical expressions. The validity of the proposed model is proved by the measurements of the test structures within a tolerance of 9%. It is highlighted that with the geometrical information, i.e., the length, width and angle of the bend, most of the commonly used on-wafer RF CMOS interconnect can be characterized by using this proposed model. Moreover, given the compact nature of the model, it can be easily implemented into commercial EDA tools.

REFERENCES

- [1] X. Shi, J. Ma, B. H. Ong, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer interconnects for CMOS RFICs," in *Proc. IEEE RAWCON*, Atlanta, GA, Sep. 2004, pp. 95–98.
- [2] X. Shi, J. Ma, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer CMOS interconnects for RFICs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 9, pp. 1060–1071, Sep. 2005.
- [3] R. H. Havemann and J. A. Hutchby, "High-performance interconnects: An integration overview," *Proc. IEEE*, vol. 89, no. 5, pp. 586–601, May 2001.
- [4] T. C. Edwards and M. B. Steer, *Foundations of Interconnect and Microstrip Design*, 3rd ed. New York: Wiley, 2000.
- [5] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Design, Layout and Simulation*. Piscataway, NJ: The Institute of Electrical and Electronics Engineers, Inc., 1997.
- [6] X. Qi, "High frequency characterization and modeling of on-chip interconnects and RFIC wire bonds," Ph.D. dissertation, Dept. Elect. Eng., Stanford University, Stanford, CA, 2001.
- [7] W. R. Eisenstadt and Y. Eo, " S -parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 15, no. 4, pp. 483–490, Aug. 1992.

Multilevel-Huffman Test-Data Compression for IP Cores With Multiple Scan Chains

Xrysovalantis Kavousianos, Emmanouil Kalligeros, and
Dimitris Nikolos

Abstract—Various compression methods have been proposed for tackling the problem of increasing test-data volume of contemporary, core-based systems. Despite their effectiveness, most of the approaches that are based on classical codes (e.g., run-lengths, Huffman) cannot exploit the test-application-time advantage of multiple-scan-chain cores, since they are not able to perform parallel decompression of the encoded data. In this paper, we take advantage of the inherent parallelism of Huffman decoding and we present a generalized multilevel Huffman-based compression approach that is suitable for cores with multiple scan chains. The size of the encoded data blocks is independent of the slice size (i.e., the number of scan chains), and thus it can be adjusted so as to maximize the compression ratio. At the same time, the parallel data-block decoding ensures the exploitation of most of the scan chains' parallelism. The proposed decompression architecture can be easily modified to suit any Huffman-based compression scheme.

Index Terms—Huffman encoding, test data compression.

I. INTRODUCTION

In order to meet the tight time-to-market constraints, contemporary digital systems embed predesigned and preverified Intellectual Property (IP) cores. The structure of IP cores is often hidden from the system integrator and as a result, neither fault simulation, nor test pattern generation can be performed for them; only a precomputed test set is delivered along with such a core. Various methods have been proposed for reducing both the test-data volume and test-application time of unknown-structure IP cores [1]–[7], [9], [10], [12]–[18], [20]–[25]. Many of them encode directly the statically or dynamically compacted test sets using various (usually classical) compression codes like Golomb [2], [3], [21], alternating run-length [4], frequency-directed run-length (FDR) [5], [18], statistical codes [7], [10], [12], nine-coded-based [23], and combinations of codes [22]. Unfortunately, these code-based methods cannot exploit the existence of multiple scan chains in a core. This shortcoming stems from the fact that parallel decompression is not possible due to either the nature of the code or the way it is used in the specific method. For example, the decoding of the various run-length codes is performed in a strictly serial manner. On the other hand, the straightforward approach for parallelizing selective Huffman decoding (i.e., by encoding slice-sized data blocks and then by loading the scan chains in parallel with a whole slice after the decoding of every codeword) leads to both large decompressors and very low compression ratios. Since the vast majority of the cores have multiple scan chains, a serial-in, parallel-out register must be used for spreading the decoded data in them and thus, no test-time savings, despite the existence of multiple scan chains, are possible. The solution of using multiple decoders in parallel is too

Manuscript received May 6, 2007; revised August 8, 2007. This work was supported in part by the European Social Fund (ESF), Operational Program for Educational and Vocational Training II (EPEAEK II) and by the program PYTHAGORAS.

X. Kavousianos is with the Computer Science Department, University of Ioannina, 45110 Ioannina, Greece (e-mail: kabousia@cs.uoi.gr).

E. Kalligeros is with the Information and Communication Systems Engineering Department, University of the Aegean, 83200 Karlovassi, Samos, Greece (e-mail: kalliger@aegean.gr).

D. Nikolos is with the Computer Engineering and Informatics Department, University of Patras, 26500 Patras, Greece (e-mail: nikolosd@cti.gr).

Digital Object Identifier 10.1109/TVLSI.2008.2000448