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Lu₂O₃/Al₂O₃ gate dielectrics for germanium metal-oxide-semiconductor devices

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Effect of Ge out diffusion into Lu₂O₃/Al₂O₃ high-*k* dielectric stack was investigated. Increasing Ge signal intensity with increasing annealing temperature was observed, which suggests that there may be excessive Ge incorporation into the high-*k* film. The electrical measurement shows an improvement of the *k* value with annealing temperature, as well as an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and result in degradation of the electrical performance of the device due to the increased leakage current. © 2008 American Institute of Physics. [DOI: 10.1063/1.2970036]

The future of semiconductor industries would depend on the continuous development of integrated circuit performance in order to meet the ever increasing demand for higher performance devices. The gate oxide thickness downscaling with conventional silicon dioxide will soon reach its limit for electron tunneling (~2 nm). With the decreased thickness, silicon dioxide is not a suitable material to be used due to the high leakage current, in which the gate current density will exceed the limit set by power dissipation considerations. It has therefore become necessary to replace the conventional SiO₂ with a high-*k* material for the continual improvement of next generation devices. Nevertheless, downscaling is not the only mean to achieve further improvement in device performances. High mobility semiconductors other than Si have been considered as an alternative channel material. Ge has attracted much interests as a possible replacement for Si due to the fact that both electron and hole mobilities in Ge are higher compared to that of Si.¹ However, Ge has been known to have poor quality of its thermal oxide, which is unstable, water hydrolysable, and has poor electrical properties.² It has been reported that Ge oxides thermally decompose and desorb from the surface at relatively low temperatures and induce point defects on the surface.^{3–5} These defects can easily act as recombination and generation centers because of the small bandgap of Ge.⁶ It has been shown that by depositing high-*k* material on Ge to replace the thermally oxidized layer of Ge, it is possible to obtain a thin equivalent oxide thickness (EOT) and high mobility.⁷ This has fueled the research into alternative channel material and dielectric materials. Rare earth oxides, such as La₂O₃, Yb₂O₃, and Lu₂O₃,^{8–11} are promising candidates for the next generation of high-*k* gate insulators, which are expected to be thermally stable in contact with Si even at high temperatures. Previously, Lu₂O₃ was reported to have a *k* value of 11–12 (Refs. 9 and 11) with a reported leakage current of 1.2 × 10^{−3} A/cm² (at +1 V) for a 4.5 nm thick

film.⁹ Lu₂O₃ is expected to have a good conduction band offset with Si and is a suitable high-*k* dielectric candidate because of the large band gap that is expected from Lu₂O₃ due to the completely filled 4*f* shell of Lu and its unique oxidation number (equal to 3), which avoids mixed Lu oxide stoichiometries with different electronic structures.¹¹ In addition, the 2:3 metal:oxygen stoichiometry ratio promotes a low charge neutrality level and hence a high conduction band offset at the oxide/silicon interface.^{11,12} In order to achieve a stable high-*k*/Ge interface, it is very crucial to tailor the interfacial or passivation layer. One of the most common methods of Ge passivation is through the surface nitridation of the Ge substrate¹³ and through intentionally grown GeON interfacial layer.¹⁴ Work on Al₂O₃ as a passivation layer on Ge is still limited although it has been widely used on Si substrate. In this work, we report the Lu₂O₃/Al₂O₃ gate dielectrics for germanium metal-oxide semiconductor devices.

The Ge substrate used was *n*-type wafers (111). Before film deposition on the Ge substrates, it is necessary to remove the native oxide present. We have used a conventional wet cleaning of cyclic HF (1:100 diluted HF solution) dip with rinsing in de-ionized water. The substrate was then treated with NH₃ plasma for the oxynitride passivation layer. Atomic layer deposition (ALD) was used to deposit a thin Al₂O₃ passivation layer using trimethylaluminum and O₂ plasma precursors. The ALD equipment used is Oxford FlexAL™ system. The Lu₂O₃ ultrathin films were deposited *ex situ* using the pulse laser deposition technique at a base pressure of 1.0 × 10^{−7} Torr. A KrF excimer laser with a wavelength of 248 nm and an energy density of ~1.5 J/cm² was used. The frequency of the laser was set to 5 Hz. Rapid thermal annealing (RTA) was done on the samples in N₂ temperature for temperatures ranging from 300 to 600 °C. Top electrodes of Au with a diameter of 0.3 mm were sputtered using a physical mask. The bottom of the Si substrates was first cleaned using 1% HF to remove the native oxide before sputtering of gold to make the back contact. The film thickness and interfacial property were examined using high-

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FIG. 1. (a) Cross-sectional HRTEM image of $\text{Lu}_2\text{O}_3/\text{Al}_2\text{O}_3$ thin film after RTA at 600 °C in N_2 ambient. (b) Illustration on the effect of annealing on the $\text{Lu}_2\text{O}_3/\text{Al}_2\text{O}_3$ gate stack before and after annealing at 600 °C in N_2 ambient. Model is first proposed by Kamata.

resolution transmission electron microscopy (HRTEM) with JEOL 2010 microscope. The electrical characteristics of the fabricated metal-insulator-semiconductor devices were measured using a precision LCR meter (HP4284A) at a high frequency of 100 kHz for capacitance-voltage measurements (C - V) and semiconductor parameter analyzer (Keithley 4200) for the current density-voltage (J - V) measurements. For the high-resolution Rutherford backscattering spectroscopy (HRBS), a beam of 500 keV He^+ is used. The beam was incident on the sample which was mounted on a high-precision five-axis goniometer installed in a UHV chamber. The incident angle of the beam is 59.5°. The HRBS spectrum is observed at a scattering angle of 65°. The secondary ion mass spectroscopy (SIMS) measurements were obtained using a TOFSIMS IV instrument, with 1 keV Cs^+ as sputtering beam and 25 keV $^{69}\text{Ga}^+$ as analysis beam and detection of negative secondary ions.

Figure 1(a) shows a cross-sectional HRTEM image of $\text{Lu}_2\text{O}_3/\text{Al}_2\text{O}_3$ on the Ge substrate after RTA at 600 °C. As observed from the HRTEM micrograph, the thickness of the deposited films was approximately 7–8 nm. The film appeared to be amorphous throughout and there was no distinctive layer to indicate the deposited Al_2O_3 . There was a clear abrupt edge between the substrate and the thin film, suggesting an absence of unstable interfacial layer. Comparing as-deposited and 600 °C Ge spectra from the SIMS analysis shown in the inset of Fig. 2, Ge updiffusion is evident. The above observation may be explained using the intermixing model proposed by Kamata,¹⁵ as illustrated in Fig. 1(b), whereby it is possible that both Al_2O_3 and Lu_2O_3 was able to mix with residual GeO_x or out diffused elemental Ge as the case of ZrO_2 or Y_2O_3 ,^{16,17} such that the $\text{Lu}_2\text{O}_3/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ stack was converted to Lu/Al-based germanate without an interfacial layer after annealing. It was shown in the HRBS spectrum in Fig. 2 that the Ge content in the high- k film increases with increasing annealing temperature. HRBS spectra fitting revealed that the introduction of annealing promoted the growth of the Lu-based germanate, partial conversion for the 300 °C sample and full conversion for the 400 and 600 °C sample;

FIG. 2. (Color online) HRBS spectrum for the samples: as-deposited to 600 °C annealed sample in N_2 ambient. The red arrow indicates the increasing intensity of Ge in the high- k stack. The inset shows SIMS data illustrating the outdiffusion of Ge throughout the Lu_2O_3 film. The dashed spectrum represent the as-deposited condition.

suggesting intermixing in the film stack. In addition, the HRBS spectra fitting suggest that more Ge was found nearer to the film surface with higher annealing temperature. It was calculated from the HRBS spectra that the presence of Ge content increases for approximately 4% with 600 °C annealing as compared to the as-deposited sample. This result suggests a better intermixing with possible residual GeO_x film or outdiffused Ge with increasing temperature.

The typical C - V measurement at 100 kHz is shown in Fig. 3(a). The curves obtained were relatively well-shaped albeit some humps are present, which normally attributed to the presence of slow traps and relatively large interface trap density as indicated by the relatively stretched out curve.

FIG. 3. (Color online) (a) High frequency (100 kHz) C - V curve of Au/(Lu/Al) germanate/Ge capacitors. (b) J - V curve of Au/(Lu/Al) germanate/Ge capacitors of samples annealed between 300 and 600 °C in N_2 ambient.

Observed from the C - V curves, the accumulation capacitance increased with the increasing annealing temperature. A k value of 11.7 was obtained for the sample annealed at 600 °C in N_2 ambient, without taking into account the quantum mechanical tunneling effect. This translates to a capacitance equivalent thickness (CET) of 2.42 nm for the stack. This is close to the reported value for Lu_2O_3 of about 11–12.^{9,11} The electrical data seems to support earlier postulation that the higher annealing temperature allows better intermixing, thereby improving the electrical performance of the MOS stack. Increasing the annealing temperature from 300, 400, and 600 °C has improved the k value from 9.9, 10.8 to 11.7, respectively. In this case, the Al_2O_3 layer seems to suggest that it is an effective passivation layer. We believed that the Al_2O_3 may have had acted as an effective oxygen reaction barrier in preventing the formation of low quality interfacial GeO_2 .^{18,19} This is plausible since GeO_2 and Al_2O_3 has a heat of formation of 43.9 and 1675 kJ/mol, respectively. Nevertheless, further effort in reducing the CET is required as the International Technology Roadmap for Semiconductors (ITRS) (Ref. 20) outlines that for a sub-22-nm technology, an EOT of <0.5 nm is required by 2016 to sustain gate terminal control of the charge carrier in the semiconductor channel.

The general trend of the J - V characteristic measured from the rapid thermal annealed samples is shown in Fig. 3(b). The leakage current at +1 V bias for the 300, 400, and 600 °C annealed samples was 2.19×10^{-2} , 1.87×10^{-4} , and 1.37×10^{-2} A/cm², respectively. The reduction of leakage current is likely to have been caused through better intermixing at elevated temperature along with densification and defect alleviation in the film. In addition, it is observed that the leakage current was higher at 600 °C annealed sample as compared to the 400 °C annealed sample. One possible explanation is that although intermixing is a necessary condition to stabilize the interface and the leakage current, it is not entirely governed by the amount of Ge updiffusion. An excess Ge in the high- k layer is likely to quickly result in a poor electrical performance.¹⁵ Subsequently, the excessive Ge updiffusion may have caused defects in the film itself, which may contribute to leakage path and thus lead to the observed increase in the leakage current for the 600 °C annealed sample. HRBS spectra revealed an increasing trend of Ge content in the film with increasing annealing temperature. For the 300, 400, and 600 °C annealed sample, the Ge content is approximated to be about 5.0, 6.8, and 8.8 at. %, respectively. In the 600 °C annealed sample, the excess out-diffused Ge content in the film may have led to the creation of more defects in the film, which provide for leakage path resulting in higher leakage current density. Although the amount of Ge content in the film that will cause the degradation in the leakage current density is not precisely determined, our result offers a reference in which at 8.8 at. % degradation in the leakage current density is likely to be observed. A more detailed experimental work is needed to determine the exact excess Ge at. % that will degrade the

electrical performance. Our work suggests that 400 °C is an optimum annealing temperature in which an acceptable k value of 10.8 and low leakage current density of 1.87×10^{-4} A/cm² was obtained.

In summary, the effect of annealing on the $Lu_2O_3/Al_2O_3/Ge$ stack was studied. In the study, it was found that with annealing, there was intermixing of the high- k film with possible residual GeO_x that was present due to incomplete removal of the native oxide due to wet cleaning and/or outdiffused elemental Ge due to annealing, resulting in a Lu/Al based germanate. No interfacial layer was observed using HRTEM suggesting absence of GeO_x based interfacial layer after annealing. HRBS spectrum revealed an increasing Ge signal intensity with increasing annealing temperature which suggests that there may be excessive Ge incorporation into the high- k film, which may degrade the electrical performance. This is reflected in the electrical measurement, although the k value is improved with annealing temperature, there is an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and result in degradation of the electrical performance of the device due to the increased leakage current.

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