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Charging phenomena in pentacene-gold nanoparticle memory device

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The authors demonstrate a new organic memory system, using pentacene as the active semiconductor layer and citrate-stabilized gold (Au) nanoparticles as charge storage elements. A pronounced clockwise capacitance-voltage (C - V) hysteresis is observed with a memory window of 1.25–2.05 V achievable under 5–10 V programing range. Similar clockwise C - V hysteresis window and an almost constant full width at half maximum of the conductance peaks in conductance-voltage (G - V) characteristics, obtained in the frequency range of 50 kHz–1 MHz, indicated that positive charge trapping/detrapping originated mainly from the Au nanoparticles.

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Nonvolatile memory devices based on conventional silicon electronics have experienced explosive growth over the past decade in applications ranging from high end computing to low-cost mobile pen-sized flash drives. Applications such as large area electronics, low-cost dispensable sensor arrays, and memory tags on the other hand necessitate the design and development of alternate cost-effective memory solutions. Only recently organic electronics have been considered as candidates for such nonvolatile memory applications due to their simple structure, lower cost, and the prospect of stacking them for packing bits at high densities. In recent years, development of an electronic bistable device with a triple-layer structure consisting of two semiconducting or insulating organic layers and a middle discontinuous metal layer,^{1,2} or polymeric blend of metal nanoparticles,^{3–5} sandwiched between two metal electrodes, exhibits promising performance and was proposed for nonvolatile memory application.

The chemical self-assembly of Au nanoparticles has been reported to show great potential in silicon memory applications.^{6,7} We took the next step forward, and introduce a new organic memory system by using pentacene as the active organic semiconductor layer and citrate-stabilized gold (Au) nanoparticles as the charge storage elements. The deposition of the Au nanoparticles was carried out through the immobilization of citrate-stabilized Au nanoparticles^{8,9} onto amine-terminated modified silicon substrate surfaces.^{10–12} The charge storage properties of the Au nanoparticles are studied using capacitance-voltage (C - V) and conductance-voltage (G - V) measurements. Frequency dependent measurements were done to ascertain that most of the charging effect originated mainly from the Au nanoparticles, and minimal influence from interface traps which typically led to frequency dependent C - V and G - V characteris-

tics. All electrical measurements were carried out at room temperature and in vacuum environment ($\sim 10^{-4}$ torr). C - V and (G - V) measurements were done with an HP 4284A Precision LCR analyzer at the frequency of 100 kHz and amplitude of 15 mV was superimposed on the dc bias.

Figure 1(a) provides the schematic illustration of the organic memory device, which comprises a metal-pentacene-insulator-silicon (MPIS) structure. The MPIS devices were fabricated on degenerately doped n -type silicon wafer, used

FIG. 1. (Color online) (a) Schematic illustration of organic memory device with citrate-stabilized Au nanoparticles. The silicon substrate is used as the bottom gate electrode. (b) TEM images of citrate-stabilized Au nanoparticles of size of 3–7 nm.

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as the bottom gate electrode, with 4.5 nm thermally grown silicon dioxide (SiO_2) on top. The substrate surface was first functionalized with a self-assembled monolayer of 3-aminopropyl-triethoxysilane (APTES) by immersing the silicon substrate in 5% volume of APTES in absolute ethanol for 1 h. The self-assembled monolayer of APTES was used due to its well known ability to produce uniform and stable adsorption of Au nanoparticles on SiO_2/Si substrates through electrostatic attraction between negatively charged citrate Au nanoparticles and positively charged amino-terminating group ($-\text{NH}_2$). The APTES thickness was measured to be 0.9 nm using an ellipsometer. The Au nanoparticles were assembled on the amino-terminated silicon substrate surface by immersing the substrates into the Au colloids for 12 h and the Au colloids solution was maintained at pH 6. After the deposition of the Au nanoparticles, a 45 nm thick active layer of pentacene and top gold electrode (0.3 mm diameter size) are then deposited via sequential thermal evaporation. Control samples without the Au nanoparticles (metal/pentacene/APTES-modified substrate) were also prepared for comparison. Figure 1(b) shows the transmission electron microscope (TEM) image of the citrate-stabilized Au nanoparticles. The Au nanoparticles are of 5 ± 2 nm in size; the agglomeration of Au nanoparticles is minimized due to the citrate induced surface energy stabilization.¹³

The memory effect of the MPIS device is observed using the double sweep C - V and G - V measurements. For the control sample without Au nanoparticles, (metal/pentacene/APTES-modified substrate), there is negligible hysteresis being observed regardless of the sweeping direction, indicating the absence of trapped charges in the fabricated structure [Fig. 2(a)]. The hysteresis is defined to be the flatband voltage shift. A clockwise hysteresis window of 1.25 V is observed for the sample with Au nanoparticles upon double sweeping within the range of ± 5 V [Fig. 2(b)], thus indicating a net hole trapping effect.¹⁴ Under the influence of a negative bottom gate voltage, holes are injected into the pentacene layer from the top Au electrode [due to the highest occupied molecular orbital level of pentacene which is close to the work-function of Au (Ref. 15)], creating an abundance of holes in the pentacene layer. This promotes the injection of holes from the pentacene layer to the citrated Au nanoparticles and leads to a net hole trapping effect. Upon applying a positive gate voltage, the stored charges in the Au nanoparticles are flushed out, resulting in a flatband voltage shift. It should be noted that the hysteresis or conductance peak shift is independent of the scan direction and speed (10–100 mV/s). The single conductance peak is observed in two directions, indicating trapping and detrapping events of the charge carriers.¹⁶ Both the magnitude of hysteresis in C - V and the shift in the peak positions in G - V are the same. The absence of hysteresis or conductance peaks for the control sample is an indication that the observed phenomena may be attributed to holes being trapped inside the Au nanoparticles or at its interface with pentacene. Charge injection from the substrate has been excluded as we have the same charging response with devices of thickness of 45 nm thermal oxide layer (not shown).

As shown in Fig. 2(c), the hysteresis window of the C - V curve increases from 1.25 to 2.05 V with the increment of maximum operation bias from 5 to 10 V. This indicates that more and more holes are being trapped in the Au nano-

FIG. 2. (Color online) Double sweeping C - V and G - V characteristics at 100 kHz obtained by biasing the bottom gate electrode between +5 and -5 V on (a) control sample (pentacene on APTES-modified substrates without Au nanoparticles) and (b) with Au nanoparticles, respectively. (c) C - V curves with Au nanoparticles at 100 kHz for different gate bias sweeps.

particles and/or at the interface of the Au nanoparticles upon increasing the gate voltage. There is little or negligible shift in the initial flatband voltage upon increasing the operation bias, indicating minimal influence of interface traps.

In order to relate the origin of the conductance peaks and hysteresis with the Au nanoparticles, as opposed to the interface traps, frequency dependent measurements were performed. As is evident in Fig. 3, we found similar clockwise C - V hysteresis and an almost constant (standard deviation of 0.04) full width at half maximum (FWHM) of the conductance peaks in G - V characteristics in the frequency range of 50 kHz–1 MHz at room temperature. This indicates that the hysteresis and conductance peak are of the same origin,^{17,18} and since interface traps are minimal in the high frequency ranges, we can conclude that the charge trapping effect originates from the Au nanoparticles.

In summary, the fabrication of organic memory device using functionalized Au nanoparticles has been demonstrated. The double sweeping C - V and G - V characteristics of the device were shown to exhibit a clockwise hysteresis, in-

FIG. 3. (Color online) Frequency dependent (a) C - V and (b) G - V characteristics of the organic memory device. The inset shows the FWHM as a function of frequency.

dicating a net hole trapping effect. The charge trapping effect is attributed to the Au nanoparticles in the frequency range of 50 kHz–1 MHz. This approach of using functionalized Au nanoparticles as nanotraps, by virtue of its simplicity in design and processing, can realize integrated memory devices and circuits in low-cost plastic electronics applications. Further work on cycling stability and data retention times are currently in progress.

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¹L. Ma, J. Liu, and Y. Yang, Appl. Phys. Lett. **80**, 2997 (2002).

²L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott, Appl. Phys. Lett. **84**, 607 (2004).

³J. Ouyang, C. W. Chu, C. R. Szmanda, L. Ma, and Y. Yang, Nat. Mater. **3**, 918 (2004).

⁴R. J. Tseng, J. Huang, J. Ouyang, R. B. Kaner, and Y. Yang, Nano Lett. **5**, 1077 (2005).

⁵L. D. Bozano, B. W. Kean, M. Beinhoff, K. R. Carter, P. M. Rice, and J. C. Scott, Adv. Funct. Mater. **15**, 1933 (2005).

⁶S. Kolliopoulou, P. Dimitrakis, P. Normand, H. L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas, J. Appl. Phys. **94**, 5234 (2003).

⁷S. Paul, C. Pearson, A. Molloy, M. A. Cousins, M. Green, S. Kolliopoulou, P. Dimitrakis, P. Normand, D. Tsoukalas, and M. C. Petty, Nano Lett. **3**, 533 (2003).

⁸J. Turkevitch, P. C. Stevenson, and J. Hillier, Discuss. Faraday Soc. **11**, 55 (1951).

⁹J. Zhang, M. Kambayashi, and M. Oyama, Electrochem. Commun. **6**, 683 (2004).

¹⁰S. Flink, F. C. J. M. van Veggel, and D. N. Reinhoudt, J. Phys. Org. Chem. **14**, 407 (2001).

¹¹T. Sato, D. G. Hasko, and H. Ahmed, J. Vac. Sci. Technol. B **15**, 45 (1997).

¹²S. Liu, T. Zhu, R. Hu, and Z. Liu, Phys. Chem. Chem. Phys. **4**, 6059 (2002).

¹³M. C. Daniel and D. Astruc, Chem. Rev. (Washington, D.C.) **104**, 293 (2004).

¹⁴Dieter K. Schroder, *Semiconductor Materials and Device Characterization*, 2nd ed. (Wiley, New York, 1998), Chap. 6, p. 360.

¹⁵F. Amy, C. Chan, and A. Kahn, Org. Electron. **6**, 85 (2005).

¹⁶S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York 1981), Chap. 7, p. 362.

¹⁷E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, 1st ed. (Wiley, New York, 1982), Chap. 7, p. 285.

¹⁸C. W. Beenakker, Phys. Rev. B **44**, 1646 (1991).