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Study of charge distribution and charge loss in dual-layer metal-nanocrystal-embedded high- κ /SiO₂ gate stack

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In this work, we present a comprehensive experimental study of charge loss mechanisms in a dual-layer metal nanocrystal (DL-MNC) embedded high- κ /SiO₂ gate stack. Kelvin force microscopy characterization reveals that the internal-electric-field assisted tunneling could be a dominant charge loss mechanism in DL devices that mainly depends on the charge distribution in two MNC-layers and inter-layer dielectric (ILD) thickness between the two layers of nanocrystals. Our findings suggest that an optimized DL-MNCs embedded memory cell could be achieved by defining the ILD thickness larger than the average MNC-spacing for enhancement of retention ability in MNC embedded gate stacks. It implies the possibility of reducing MNC spacing in DL structure of scaled memory devices by controlling the thickness of ILD. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4712565>]

Non-volatile memory with discrete storage nodes such as semiconductor and metal nanocrystals has been introduced to reduce defect related charge loss and to overcome the scaling limitation in conventional floating gate memories.^{1,2} The work function engineering and the high density of states in metal nanocrystals (MNCs) have been found to be efficient in improving the storage capacity and retention time.²⁻⁴ It is reported⁵⁻⁷ that double-layer (DL) MNCs structure provides significant improvement of charge storage capacity and retention over the single layer MNC devices. Since the DL-MNC structure has shown a high potential for memory applications, a full understanding of its retention performance and charge loss mechanisms is crucial. Moreover, in order to design memory cell with specific retention characteristic, understanding the charge distribution and its impact on the charge loss behavior is important for device optimization, reliability predictions, and future scaling.⁸

In this work, a comprehensive experimental study is carried out with microscopic and macroscopic measurements on the DL-Pt-MNCs embedded in Al₂O₃/SiO₂ gate stacks. A comparative study is performed on the DL devices with inter-layer dielectric (ILD) thickness variation. First, the temperature dependence of retention time is studied and their charge loss behaviors are compared. The charge leakage paths in the DL devices are investigated using gate-bias accelerated retention measurements. Since electron detrapping should be dependent on the trapped electron distribution in the devices, the charge distribution in two MNC-layers is investigated using Kelvin force microscopy (KFM) and the physical model of charge loss in DL devices is proposed.

The DL-MNCs devices were fabricated on p-type Si substrate with a doping of $\sim 1 \times 10^{15} \text{ cm}^{-3}$. After the surface cleaning by HF, 50 Å SiO₂ tunnel oxide was thermally grown using a *in-situ* steam generation process. The MNC formation was realized by blanket Pt thin film deposition using physical vapor deposition (PVD) technique and subsequent annealing it in a RTP chamber resulting in a random distribution of NC position and size as a result of dewetting (agglomeration). An optimized PVD deposited Al₂O₃ was used as ILD. A thin layer of Pt was then deposited again and annealed to form another MNC layer. A 120 Å optimized Al₂O₃ was then deposited and annealed to form the control dielectric. Two DL devices were fabricated with a variation in the ILD thickness. More details of the fabrication procedures can be found in Ref. 9. The planar view TEM micrograph in Fig. 1(a) shows well isolated MNCs after Pt thin film deposition and annealing. From the cross-sectional view TEM micrographs shown in Figs. 1(b) and 1(c), the average diameter of the MNCs is around 3 nm and the two MNCs-layers are clearly separated by a 2 nm and 3 nm thick Al₂O₃ ILD in DL2 and DL3, respectively. The area coverage of MNCs was observed to be $\sim 26\%$ with a density of $\sim 3.4 \times 10^{12} \text{ cm}^{-2}$ in each MNC layer.

The macroscopic capacitor structure with Pt electrodes was used to measure charge loss in the DL devices. In Fig. 2, the charge retention behavior of the DL devices at elevated temperatures ranging from 298 to 398 K is presented. The measurements were performed on “fresh” devices (i.e., without endurance cycling) after programming at +18 V for 100 ms. The charge loss was obtained by measuring the flat band voltage shift (ΔV_{FB}) at 100 KHz. Fig. 2(b) shows the box plot of the retention time for a 5% charge loss in the DL2 and DL3 devices at various temperatures, respectively.

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FIG. 1. (a) Planar view TEM micrograph of Pt-MNCs in DL device showing well-isolated MNCs. Cross-sectional TEM micrographs of (b) DL2 and (c) DL3 samples with different ILD thickness.

The results clearly reveal that the charge retention in DL3 is better than DL2 at all temperatures. It is interesting to note that the charge loss in DL2 was independent of temperature below 100 °C.

To separate the contributions of the tunnel oxide and control oxide in the retention deterioration characteristics, gate bias (i.e., top electrode) accelerated charge leakage measurements were carried out by applying a bias to the top electrode during retention. An application of a positive bias (+Vg) accelerates the electron detrapping across the Al₂O₃ control oxide layer, while an application of a negative bias (−Vg) enhances the electron detrapping towards the SiO₂ tunnel oxide. Fig. 3 shows the retention loss from the program state for DL2 and DL3 devices at various gate biases for 15 min. It is found that the charge loss increased with increasing Vg positively. For Vg = −4 to 0 V, insignificant charge loss was observed. For Vg = −8 to −4 V, the slight increase in retention loss was found due to an increased electric field across the tunnel oxide layer. The electron trapping during the negative bias retention was found to be negligible by applying a gate voltage between −2 V and −8 V on the fresh devices. Therefore, the gate bias accelerated charge loss measurements suggest that (1) DL3 devices have better charge retention than DL2 which is consistent with the tem-

FIG. 2. (a) Charge retention in DL2 and DL3 devices at temperature ranging from 298 to 398 K. (b) Box plot of the retention time for a 5% charge loss.

FIG. 3. Retention charge loss from the program state at various gate biases for 15 min in DL2 and DL3 devices.

perature accelerated measurements and (2) the primary charge leakage path in the DL devices is through the Al₂O₃ control oxide. Moreover, a similar trend but different amount of charge loss in DL2 and DL3 was observed under a positive bias during retention, i.e., in order to have the same amount of charge loss as DL2, a larger positive bias is required to be applied to DL3 during retention. Hence, it clearly indicates the internal electric field in DL2 is higher than that in DL3.

Considering that the charge leakage path is through control oxide in the DL devices, the localized electric field F across Al₂O₃ control oxide can be defined as: $F = F_1 + F_2$, where F_1 is the electric field due to localized trapped charge in the top MNC layer and F_2 is the Coulomb-repulsion field due to the neighboring (bottom) MNC layer. Assuming a capacitor formed between each MNC and the control gate with the sandwiched Al₂O₃ control oxide as insulator, F_1 can be expressed as¹⁰

$$F_1 = \frac{Q_{NC}}{C \cdot t_{co}},$$

where Q_{NC} is the amount of charge stored in the top-layer MNC, $C = (\frac{\epsilon_{co}}{t_{co}} \cdot A)$ is the capacitance across the control oxide and A is the plane-collapsed area πR^2 for a MNC with radius R . Similarly, the Coulomb-repulsion field due to the neighboring NC layer, F_2 is given by the Coulomb's Law:

$$F_2 = \frac{Q'_{NC}}{4 \cdot \pi \cdot \epsilon_0 \cdot t_{ILD}^2},$$

where Q'_{NC} is the amount of charged stored in the “neighboring” MNC-layer and t_{ILD} is the ILD thickness. Thus, the internal electric field in DL devices can be defined as

$$F = \frac{Q_{NC}}{C \cdot t_{co}} + \frac{Q'_{NC}}{4 \cdot \pi \cdot \epsilon_0 \cdot t_{ILD}^2},$$

which depends on amount of charge stored in the top-MNC layer Q_{NC} , its neighboring bottom MNC layer Q'_{NC} , and the ILD thickness between two MNC layers t_{ILD} .

To further confirm higher internal electric field observed in DL2 from the gate bias accelerated retention measurement, the charge distribution in two MNC-layers was analyzed by KFM characterization since the distribution of trapped electrons in MNC-layers contributes the internal

electric field across oxide. The charges were injected first over the surface of the dielectric film using a Pt coated conductive tip which was in contact with the surface during the charge injection process. After charging the MNCs, KFM images were acquired in a two-pass procedure.¹¹ From the potential images, we confirmed that the positive (negative) voltage stress applied to the AFM tip always results in a positively (negatively) trapped charge. This indicates that the charge transfer occurs between the tip and the oxide layer rather than from the Si-substrate which is in good agreement with other literature reports.^{12–15} Therefore, the charge injection in the KFM characterization always results in gate (AFM tip) injection, which is opposite from the charge injection to the macroscopic capacitor structure by the gate electrodes, where the charge transfer is shown to be substrate injection.

Fig. 4(a) shows the potential profiles of DL2 and DL3 samples upon negative charge injection. The full-width-at-half maximum (FWHM), (i.e., 50% of the peak) and $1/e^2$ width ($\sim 13.5\%$ of the peak) of DL2 and DL3 samples were extracted from the potential profiles acquired at ~ 60 s right after charge injection. Fig. 4(b) presents the change in FWHM and $1/e^2$ width with various potential peaks (i.e., various injection voltages). As the injection voltage increases, the diameter of charge cloud at FWHM and $1/e^2$ increases in both DL2 and DL3. It is interesting to note that the rate of increase in the $1/e^2$ width with injection voltages in DL3 is much more significant than that in DL2 (see Fig. 4(b)).

As illustrated in Fig. 4(c), we propose the preferential path of charge injection model in dual-layer MNCs to explain the potential profiles observed in DL2 and DL3. Under the AFM tip (gate) injection, most of the carriers were injected into the top MNC-layer since the direct tunnel distance to the lower MNC-layer was larger. However, the

charges injected into the top NC layer can be emitted and re-trapped either in the neighboring MNC (P1) or in the bottom NC layer (P2) due to the presence of enhanced electric field between MNCs during charge injection. Also, it is possible to charge the bottom layer directly from the tip depending upon the position of the bottom layer MNC (P3). In either case, it is reasonable to assume that the top MNC-layer received more charges than the bottom MNC-layer under gate injection. Similarly, it is expected that more charges will be injected into the bottom layer under the substrate injection mode.

The significant increase in the rate of $1/e^2$ width potential profile with tip injection voltages in DL3 suggests that most of the carriers injected to the top MNC-layer were emitted and re-trapped in the adjacent MNCs in the same layer, rather than tunneling to the neighbor MNC-layer (P1 $\gg$ P2) in DL3. It depicts the average MNC spacing is smaller than the ILD thickness of DL3 (< 3 nm) and the difference in charge distribution of two MNC-layers in DL3 is large. On the other hand, the similar trend (slope) of increase in both FWHM and $1/e^2$ width with injection voltages in DL2 (see Fig. 4(b)) suggests the carries were most likely to be injected in both top and bottom MNC layers owing to thinner ILD. In this case, the average MNC spacing would be comparable or larger than the ILD thickness of DL2 (≥ 2 nm) and the difference in the injected charge distribution of two MNC-layers in DL2 is less compared to that in DL3. Assuming the average MNC spacing in the DL2 and DL3 is to be the same because MNCs were deposited using same process parameters, the average MNC spacing in DL devices was estimated to be of between 2 and 3 nm, based on the diameter ~ 500 nm potential profiles observed in KFM characterization. Also, the less difference in charge distribution of two MNC-layers in DL2 implies that there are more injected charges in the neighbor MNC layer compared with DL3, which could result higher internal electric field in DL2 during retention due to a stronger repulsive field F_2 as discussed earlier.

Hence, the difference in the retention behavior of DL2 and DL3 observed under the temperature accelerated retention measurements could be explained by the energy band diagram based on the internal-electric field induced by charge distribution in the two MNC-layers and ILD thickness (see Fig. 5). In this illustration, the charge distribution is considered under the substrate injection in the temperature accelerated retention measurements—where more charges are injected in the bottom MNC-layer and fewer charges are injected in the top MNC-layer especially in the sample with thicker ILD (i.e., DL3). Since the deep-level traps present in the Al_2O_3 ,^{16–18} the capture and emission should be essentially a multiphonon process,^{19–21} i.e., phonon-induced and accompanied by the emission of some phonons.¹⁹ Hence, the multi-phonon-assisted tunneling model²¹ was adopted to explain the charge loss through Al_2O_3 control oxide in DL structures which considers electron-phonon coupling in the oxide. According to this model, the charge loss occurs by electron tunneling to different trapping level presented in the high- κ control oxide and the capture and emission rates of these traps depends on the phonon transition probability.

In DL2, the high internal electric field across oxide and more charges stored in the top MNC layer comparing with

FIG. 4. (a) Potential profile of DL2 and DL3 samples at ~ 60 s after negative charge injection. (b) Evolution of FWHM and $1/e^2$ width with various potential peaks. (c) Illustration of preferred paths of charging in DL-MNCs structure under gate injection.

FIG. 5. The schematic energy band diagrams according to the charge distribution under substrate injection and internal electric field during retention in (a) DL2 and (b) DL3 devices. 1-4 corresponds to the possible charge loss processes through trap-assisted-tunneling, thermally assisted tunneling, thermionic emission, and direct tunneling through rectangular barrier, respectively.

DL3 could provide an alignment of oxide traps and the trap inside the NCs (see Fig. 5(a)). As a result, the discharging might easily occur through a trap-assisted-tunneling. Simultaneously, the thermally detrapped electrons could reach the oxide conduction band through thermally assisted tunneling and/or thermionic emission and are collected by the control gate which becomes dominant at higher temperatures ($T > 100^\circ\text{C}$ in this case).

In DL3, the reduced internal electric field across Al_2O_3 and fewer electrons trapped in the top layer under substrate injection could result in a misalignment between the trapping states in the MNCs and the traps presented in the high- κ . Hence, “only” the thermally excited electrons have a high possibility to tunnel into the traps in the high- κ . As a consequence, the resulting charge loss is reduced and the charge loss rate strongly depends on the temperature. Moreover, the tunneling probability P from one NC layer to another through rectangular barrier is exponentially proportional to the ILD thickness t_{ILD} : $P \propto \exp(-2k_{\text{ox}}t_{\text{ILD}})$, where k_{ox} is the wave vector in the oxide. Hence, the larger ILD thickness in DL3 of 1 nm significantly reduces the electron tunneling probability from the bottom NC layer to the top NC layer minimizing the charge leakage through the control oxide during retention.

In summary, the charge loss and the charge distribution study in DL-MNCs devices suggest that charge loss in DL structures is mainly due to the internal electric field induced by trapped electrons which depends on the ILD thickness and MNC spacing. When the ILD thickness is comparable to MNCs spacing (i.e., DL2), the charge distribution in two-MNC layers is similar and the internal electric field induced by charges stored in the MNCs is higher. It leads to internal-electric-field assisted tunneling dominates at lower temperature (below 100°C). In contrast, when the ILD thickness is

larger than the average MNC spacing (i.e., DL3), less charge injected in the neighboring MNC layer, resulting in a reduction of both internal electric field and possibility of oxide trap alignment with the traps inside the MNCs. Moreover, a thick ILD reduces the electron tunneling probability from one MNC-layer to another during retention. Therefore, the DL-MNC devices with ILD thickness larger than the average MNC spacing are proposed to be an optimum memory cell design with retention reliability perspective.

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