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Role of low temperature rapid thermal annealing in post-laser-annealed *p*-channel metal-oxide-semiconductor field effect transistor

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In this letter, the authors study the importance of a low temperature anneal in the removal of crystalline defects resulting from pulsed laser annealing of preamorphized ultrashallow p^+/n junction. Using an additional low thermal budget rapid thermal annealing at 600 °C for 60 s, suppression of junction leakage current of two orders in a single-pulse laser annealing and one order in a ten-pulse laser annealing is achieved through a reduction of the residual crystalline defects that could not be annihilated by laser annealing. *p*-channel metal-oxide-semiconductor field effect transistors with good electrical characteristics can be obtained using pulsed laser annealing followed by a low thermal budget rapid thermal annealing. © *2006 American Institute of Physics*.
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Highly activated and ultrashallow junction is essential in nanoscale complementary metal-oxide-semiconductor technology for suppression of short channel effects.[1,2] One promising candidate for the postimplantation annealing process is laser annealing (LA).[3–5] LA typically melts the surface region of the implanted substrate and causes the dopant to be distributed uniformly, producing a boxlike profile after regrowth. This is possible due to the fact that the diffusivity of boron in liquid Si is about eight orders higher than that in solid Si.[3,4] The junction depth is normally determined by the melt depth induced by the laser irradiation. LA melting technique typically employs a preamorphization implantation (PAI) of Si^+ or Ge^+ ions creating a continuous amorphous Si (α-Si) layer in which subsequent implantation is performed. Since the melting temperature of α-Si is about 200 °C lower than that of crystalline Si (*c*-Si), LA could melt the α-Si without melting the underlying substrate, resulting in an improved process window.[3,4] The final junction depth is thus defined by the PAI depth. However, residual defects, such as stacking faults, microtwins, dislocation, and end-of-range (EOR) damage, that were not removed by LA can be detrimental and can drastically increase the leakage current when the defects are situated in the depletion region of the junction.[2] Reports have shown improvement in annihilation of residual defects using a rapid thermal annealing (RTA) at a temperature greater than 800 °C.[6–8] However, a high temperature RTA above 800 °C could cause undesirable boron deactivation and enhanced boron diffusion.[9–11] Furthermore, the effects of post-LA RTA are not decoupled from subsequent thermal cycles, such as silicidation, in the reported articles.[6,7] In this letter, we report that a post-LA RTA with an annealing temperature as low as 600 °C can be used in reducing the crystalline defects unannealed out by LA during the formation of laser annealed ultrashallow p^+/n junctions, leading to a good electrical performance of *p*-channel metal-oxide-semiconductor field effect transistor (*p*-MOSFET). In order to isolate the effects of the low temperature RTA, the electrical properties of the fabricated devices were characterized without additional subsequent thermal process upon post-LA RTA.

Ultralow energy B^+ implantation was performed at 0.5 keV with a dose of 1×10^{15} cm^{-2} on *n*-type Si (100) substrate. Prior to B^+ implantation, some of the wafers were preamorphized using Si^+ implantation at 10 keV with a dose of 2×10^{15} cm^{-2}. Cross-sectional transmission electron microscopy (XTEM) shows that a continuous amorphous layer of about 30 nm was created by the Si^+ implantation. *p*-MOSFET with a thermally grown 6.5 nm gate oxide was also fabricated for the electrical study. After gate stack patterning, the source/drain region was preamorphized using a Si^+ implantation at 10 keV with a dose of 3×10^{15} cm^{-2}, creating an amorphous layer of 35 nm. B^+ implantation was then performed at 2.0 keV with a dose of 3×10^{15} cm^{-2}. The 2.0 keV B^+ implantation was used to overcome a surface oxide present during the device integration and to optimize a

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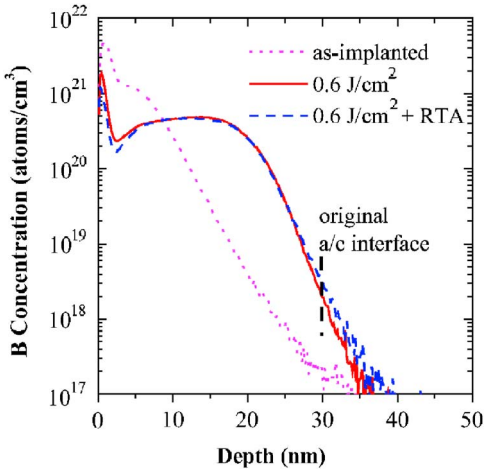

FIG. 1. (Color online) SIMS profiles of boron subjected to LA at 0.6 J/cm^2 with or without a post-LA low temperature RTA at 600 °C for 60 s. Minimum diffusion near the tail region occurred due to the additional RTA cycle. The B^+ implantation was performed at 0.5 keV with a dose of 1×10^{15} cm^{-2}, while the Si^+ amorphization implantation was conducted at 10 keV with a dose of 2×10^{15} cm^{-2}.

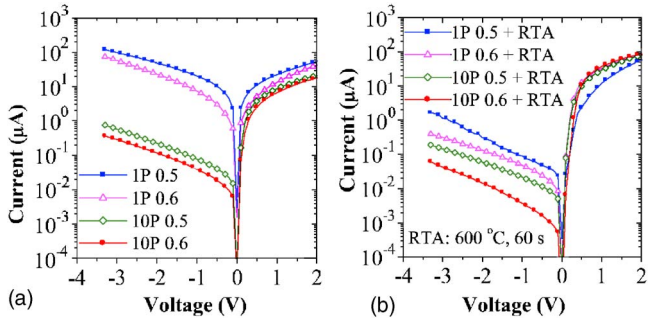

FIG. 2. (Color online) *I-V* characteristics of p^+/n junction subjected to (a) only LA and (b) LA followed by a RTA. Both single-pulse (1P) and ten-pulse (10P) LAs for laser fluences of 0.5 and 0.6 J/cm^2 were used for (a) and (b). The post-LA RTA in (b) was conducted at 600 °C and 60 s. The B^+ implantation was performed at 2.0 keV with a dose of 3×10^{15} cm^{-2}, while the Si^+ preamorphization implantation was conducted at 10 keV with a dose of 3×10^{15} cm^{-2}.

junction overlap region near the gate/spacer edge. p^+/n diodes were also fabricated using the same *p*-MOSFET implantation processes. Based on a TRIM simulation, both boron profiles in the unpatterned and device samples fall within the Si^+ preamorphized layer. LA was carried out in a normal ambient using a 248 nm KrF excimer laser with a pulse duration of 23 ns and a repetition rate of 1 Hz. After LA, some of the devices were then subjected to a RTA at a low temperature of 600 °C for 60 s. The low temperature is chosen to avoid undesirable boron deactivation and enhanced diffusion typically seen in a high temperature range.[9–11] To avoid additional thermal process, no silicidation was performed on the devices. The dopant profiles were analyzed by secondary ion mass spectrometry (SIMS) using a Cameca IMS 6f instrument. A primary beam of O_2^+ ions with a net energy of 1 keV at 56° incidence was scanned over an area of 250×250 μm^2. XTEM samples were prepared by standard mechanical polishing and ion-milling procedures.

Figure 1 shows the SIMS profiles of boron subjected to LA at 0.6 J/cm^2 with or without a post-LA RTA at 600 °C for 60 s. A boxlike boron profile is contained in the original 30 nm PAI region due to the melting of the α-Si layer only during LA. It is observed that the 600 °C low temperature RTA causes minimum diffusion near the tail region of the laser annealed boron profile. The diffusion is attributed to the presence of EOR defects left unannealed upon LA.[9] A Hall measurement reveals a decrease of the corresponding sheet resistance from 286 to 166 Ω/□ when the LA samples were subjected to the post-LA low temperature RTA. This corresponds to an enhanced Hall mobility of about two times to 25 cm^2/V s with negligible dopant deactivation. The enhancement in the mobility is caused by a reduction in the crystalline defects annealed out by the additional low temperature RTA that will be explained in the following discussion.

Figure 2 shows the diode characteristics of the ultrashallow p^+/n junctions formed using similar LA conditions to those shown in Fig. 1, i.e., by LA only or LA followed by the RTA. Laser fluence of 0.5 or 0.6 J/cm^2 was used to completely melt the PAI layer without melting of the underlying substrate. The conditions were established from the XTEM, SIMS analysis, and using a one-dimensional heat flow calculation.[12] In Fig. 2(a), single-pulse LA of fluences of 0.5 and 0.6 J/cm^2 resulted in a high junction leakage current of the same order as the forward current. As depicted in Fig. 3(a), the high leakage current is due to the presence of crystalline defects, such as stacking faults, microtwins, dislocation, and EOR damage, extending throughout the original PAI region that could not be removed by the single-pulse LA.[13–15] Fast recrystallization of the melted PAI region causes the formation of crystalline defects.[13–15] Even the recrystallized PAI layer is epitaxial with the Si (100) substrate, as shown by the diffraction pattern in the inset in Fig. 3(a); the crystalline defects lead to the highly leaky junctions shown in Fig. 2(a). It is also observed that a higher fluence at 0.6 J/cm^2 resulted in a lower leakage current, which confirms a higher defect removal efficiency at high fluence.[9,16] However, high fluence at 0.6 J/cm^2 is sufficient to cause a melting in *c*-Si and leads to undesirable deformation of the polycrystalline Si gate.[17] On the other hand, a ten-pulse LA suppresses the leakage current by two orders of magnitude.[15] The corresponding TEM results indicate that the crystalline defects were effectively eliminated by the subsequent laser pulses. Figure 2(b) indicates an improved diode characteristic in both single- and ten-pulse LAs following a post-LA low temperature RTA at 600 °C for 60 s which alone shows very leaky junction. A suppression of the leakage current of about two orders in the single-pulse LA and one order in the

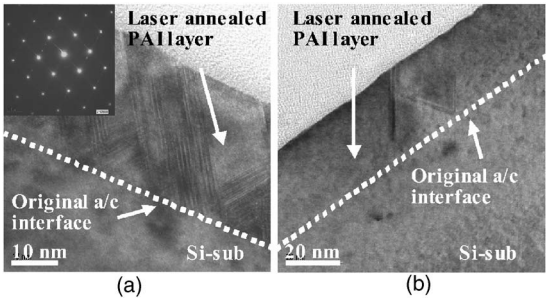

FIG. 3. Cross-sectional transmission electron microscopy micrographs of unpatterned PAI samples subjected to a single-pulse LA at (a) 0.5 J/cm^2 only and (b) 0.5 J/cm^2 with a post-LA RTA at 600 °C for 60 s. The inset in (a) is the electron diffraction pattern showing epitaxial silicon (001) obtained from the recrystallized region that contains crystalline defects. The implantation conditions are the same as those used in Fig. 1.

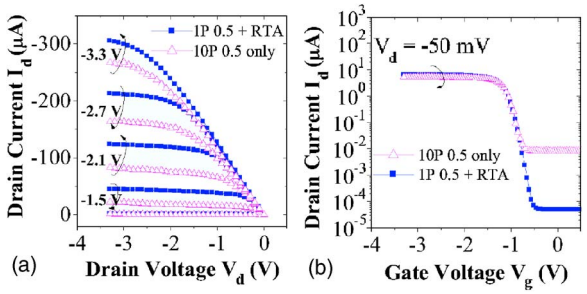

FIG. 4. (Color online) (a) Drain current (I_d) vs drain bias (V_{ds}) and (b) drain current (I_d) vs gate bias (V_{gs}) characteristics of a 0.5 μm p-MOSFET subjected to a single-pulse LA at 0.5 J/cm^2 with a post-LA RTA at 600 °C for 60 s or only to a ten-pulse LA at 0.5 J/cm^2. The low drive current is due to unsilicided source/drain and gate regions. The implantation conditions are the same as those used in Fig. 2.

ten-pulse LA is achieved by annealing out the crystalline defects by the low temperature RTA [see Fig. 3(b)]. This signifies the presence of residual defects upon the highly nonequilibrium and fast LA process, especially for the single-pulse LA.[6,9] On the other hand, dissolution or removal of the crystalline defects occurs when subjected to the relatively more equilibrium process of low temperature RTA. RTA at 600 °C for 60 s alone does not cause significant activation of boron dopants, and the junction remains leaky. A sheet resistance measurement indicates that at 600 °C RTA, a moderate activation of dopants through solid-phase epitaxial regrowth[18,19] of the preamorphized layer only occurs at a longer annealing duration of at least 180 s.

Figures 4(a) and 4(b) show the I_d-V_{ds} and I_d-V_{gs} characteristics, respectively, of a 0.5 μm p-MOSFET subjected to a single-pulse LA at 0.5 J/cm^2 with a post-LA RTA at 600 °C for 60 s and a ten-pulse LA at 0.5 J/cm^2. The low drive current is due to unsilicided source/drain and gate regions. An annihilation of the crystalline defects in the annealed junctions gives rise to a higher drive current and lower leakage current of two orders in the p-MOSFET subjected to post-LA low temperature RTA. Similar results were obtained for other p-MOSFETs fabricated by LA followed by RTA process [i.e., Fig. 2(b)]. On the other hand, no transistor characteristics can be obtained from the p-MOSFETs fabricated by only single-pulse LA [i.e. Fig. 2(a)]. This is due to an excessive junction leakage current resulting from the single-pulse LA. Although a higher fluence (i.e., greater than 0.6 J/cm^2) suppresses the junction leakage current, undesirable effects, such as physical gate degradation[17] and deeper junction depth, are still present. Therefore, laser fluence used for MOSFET fabrication should be kept low to prevent these undesirable effects while maintaining a low junction leakage current through annihilation of residual defects. As shown in Fig. 4, this can be achieved by applying a post-LA low temperature RTA. It should be noticed that an optimal laser fluence obtained on an unpatterned sample or on a patterned device may vary due to the presence of oxide isolation and gate stacks.[5,16,17,20] Nevertheless, the results show that the post-LA low temperature RTA is an important process and effective in suppressing junction leakage for a wide range of laser fluences and conditions used for MOSFET fabrication.

Melting of Si^+ preamorphization implantation layer down to or just beyond the a/c interface by pulsed laser annealing may not be sufficient to remove the crystalline defects generated during the implantation and fast regrowth of LA, resulting in a high leakage current despite a highly activated p^+/n junction. Post-LA low temperature RTA process has been shown to be critical for the further elimination of the crystalline defects in the laser annealed preamorphized p-MOSFET. Good p-MOSFET characteristics can be obtained using a combination of LA and a post-LA low temperature RTA, which is suitable for low thermal budget Si process.

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