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Formation of SrTiO₃ nanocrystals in amorphous Lu₂O₃ high-*k* gate dielectric for floating gate memory application

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We have developed a method based upon pulsed laser deposition to produce SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ high-*k* dielectric. The high resolution transmission electron microscopy study revealed the complete isolation of SrTiO₃ nanocrystals embedded in Lu₂O₃ matrix with 4 nm diameter and well distributed with an area density estimated to be about $8 \times 10^{11} \text{ cm}^{-2}$. A pronounced capacitance-voltage hysteresis is observed with a memory window of $\sim 1.5 \text{ V}$ under the 6 V programming. In addition, the retention characteristics are tested to be robust. © 2006 American Institute of Physics. [DOI: 10.1063/1.2234302]

The limitations in terms of scaling in the traditional floating gate (FG) nonvolatile memories (NVM) have spurred the development of nanocrystal-based memories. The application of NVM is predominant in many portable devices such as mobile phones, PDAs, etc.¹ These devices require NVMs with low power consumption and high density. As compared to the traditional floating gate memory, a structure having nanocrystals embedded in the dielectrics has exhibited the high potential to produce a memory with low operating voltage, high endurance, fast write-erase speeds, and better immunity to soft errors.^{2,3} The memory operation of these devices has been associated with the charge exchange between the nanocrystals and the inversion layer. Significant improvement with regard to the programming efficiency and data retention in the nanocrystal nonvolatile memories was observed when high-*k* dielectric is used in place of the conventional SiO₂.^{3–6} In the present research works, most groups focus on the formation of Ge nanodots embedded in high-*k* gate dielectric. The formation of Ge nanocrystals embedded in high-*k* dielectric matrix has been explored by Lee *et al.*, Wang *et al.*, and Lu *et al.* in which the Ge nanocrystals are embedded in high-*k* material matrices such as HfAlO and LaAlO₃.^{7–9} In addition, many metal nanodots have also been fabricated in high-*k* dielectrics. Wang *et al.* fabricated silver nanodots on/embedded in Al₂O₃ gate dielectric.¹⁰ The formation of tungsten nanocrystals on HfAlO/Al₂O₃ tunnel oxide has also been fabricated by Samanta *et al.*¹¹ Other metal nanodots embedded in high-*k* matrix were also demonstrated in the work of Lee *et al.*, where nickel nanocrystals are formed in HfO₂ high-*k* dielectric,¹² and Sargentis *et al.*, where Pt nanoparticles were incorporated in a HfAlO high-*k* dielectric.¹³ However, these semiconductors and metals are not the only nanodot materials being researched. Chen *et al.* has fabricated the high-density Al₂O₃ nanodots in SiO₂ where good retention property was obtained.¹⁴

Compared with these candidate storage node materials, strontium titanate (SrTiO₃) in the perovskite structure exhibits high charge storage capacity, good insulating behavior, and paraelectricity (no fatigue or aging problem) in the operating temperature range of these devices.^{15,16} As potential

high-*k* candidates, Lu₂O₃ is predicted to be thermodynamically stable on Si,^{17,18} and it has a good conduction-band offset (CBO) with Si.¹⁹ Good insulating properties and *k* of around 11 were reported for Lu₂O₃ films grown by high-temperature oxidation of metallic films,²⁰ ultrahigh vacuum electron-beam deposition,²¹ and atomic-layer deposition.²² Among the lanthanide oxides, Lu₂O₃ has the highest lattice energy ($-13\,871 \text{ kJ/mol}$) and the largest band gap (5.5 eV).^{23–26} It is hence expected to show not only better hygroscopic immunity but also lower leakage current than other lanthanide oxide thin films.

In this letter, we produced SrTiO₃ nanocrystals in amorphous Lu₂O₃ high-*k* dielectric matrices using a pulsed laser deposition method. Good performances in terms of large memory window and long data retention were also observed.

A KrF pulsed laser beam of 248 nm wavelength and energy density of 1.4 J/cm^2 with frequency of 5 Hz was used to ablate the target in an ultrahigh vacuum chamber. The targets to be laser ablated consisting of one piece of high-purity (99.999%) Lu₂O₃ (diameter $D=25 \text{ mm}$) round target and a piece of small square single crystal SrTiO₃ (of about 3 mm in length) target were first prepared. The SrTiO₃ target was glued onto the surface of the Lu₂O₃ target making a two-material assembly with only physical, but not chemical, contact between them. During the pulsed laser deposition (PLD) process, for the tunneling oxide layer deposition, we kept the target stationary while allowing the laser to ablate the Lu₂O₃. Then, to form the nanocrystals embedded in Lu₂O₃ matrix, the SrTiO₃–Lu₂O₃ target assembly was set to spin slowly about its central axis and the laser beam vaporized the two component materials alternately. Finally, the laser beam was focused onto Lu₂O₃ for the control oxide layer deposition.

The ablated materials were deposited on *p*-type (100) Si wafer substrates which were first cleaned using SC1 and SC2 mixture, and then dipped in a 1% HF solution to remove the native oxide. The deposition and growth of the films on the substrate were carried out in a high vacuum system with a background pressure of about $3.8 \times 10^{-7} \text{ Torr}$ with the target rotating at about 20 rounds/min at room temperature. After deposition, the thin film was subjected to a postdeposition annealing (PDA) at 400 °C for 60 s in nitrogen ambient. By controlling the exposed area ratio of Lu₂O₃:SrTiO₃ under

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FIG. 1. (a) Planar TEM image of SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ dielectric matrix. On the top left corner, we show the electron diffraction pattern for SrTiO₃ nanocrystals. (b) Cross-sectional TEM image of SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ dielectric matrix.

the laser ablation along with the target rotation speed, the film so produced was composed of tiny SrTiO₃ nanocrystals with diameters of about 4 nm embedded in amorphous Lu₂O₃ thin film. The film structure was examined using high resolution transmission electron microscope (HRTEM) with JEOL 2010 microscope. Top electrodes of Au with a dimension of 0.5×0.5 mm² were evaporated for electrical measurement. The electrical characteristics of the fabricated metal-insulator-semiconductor (MIS) devices, capacitance-voltage (*C-V*), and capacitance-time (*C-t*) were measured using a precision LCR meter (HP 4284A).

Figure 1(a) shows the planar TEM image of the synthesized SrTiO₃ nanocrystals, with its corresponding electron diffraction pattern on the top left corner. The diffraction pattern was matched against a simulated diffraction pattern for SrTiO₃ generated using a TEM simulator Java electron microscopy simulation (JEMS) software.²⁷ Comparing the experimental and the simulated diffraction patterns, it can be deduced that the nanocrystals are SrTiO₃ nanocrystals with cubic perovskite structure. The average diameters of the SrTiO₃ nanocrystals are approximately 4 nm and the area density of the nanocrystals is estimated to be about 8×10^{11} cm⁻². Figure 1(b) shows a cross-sectional HRTEM image of the Lu₂O₃ thin film on the Si substrate. The SrTiO₃ nanocrystals embedded in Lu₂O₃ can be clearly seen between the tunnel oxide and the control oxide, and the shape of the SrTiO₃ nanocrystals is almost spherical. In this sample with SrTiO₃ nanocrystals, Lu₂O₃ is used as the control and tunneling oxide layer in the trilayer memory structure of Lu₂O₃/SrTiO₃/Lu₂O₃. The total physical thickness, the thicknesses of control and tunneling oxide layers are about 20, 4, and 10 nm, respectively. It can also be confirmed that the Lu₂O₃ thin films still remain amorphous after PDA at

FIG. 2. High-frequency (1 MHz) capacitance-voltage hysteresis of sample with SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ dielectric and reference sample without SrTiO₃ nanocrystals.

400 °C and there is no observable interfacial layer between Si substrate and Lu₂O₃ film.

Figure 2 shows the typical high frequency (HF) (1 MHz) *C-V* measurements of two MIS capacitors with and without SrTiO₃ nanocrystals after the bidirectional bias sweeps. It can be seen that under a low operating voltage of 6 V, a significant threshold voltage shift (~ 1.5 V) is observed from *C-V* hysteresis of the sample with SrTiO₃ nanocrystals. As the swept voltage is increased to 8 V, a more pronounced *C-V* shift is observed. It is perceived that the hysteresis is counterclockwise which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate.²⁸ In contrast, the controlled sample without SrTiO₃ nanocrystals shows no obvious flat band voltage shift, suggesting that the large memory effect observed in the sample with SrTiO₃ nanocrystals is caused by the charges stored in the SrTiO₃ nanocrystals. Generally, the hysteresis may be introduced by the mixed effects of injected charges stored in the nanocrystals, essential trap charges existing in the oxide, or interface states.²⁹ Since we have used the same processes to produce the two samples with the exception of the presence of SrTiO₃ nanocrystals, the hysteresis effect produced by the essential trap charges and interfacial states should be the same for the two samples. Therefore, it can be concluded that the large hysteresis observed in the sample with SrTiO₃ nanocrystals is caused by the injected charges stored in the nanocrystals and/or at the interface of the nanocrystals.²⁸

The memory data retention characteristics at room temperature for this nanocrystal floating gate memory capacitor were also studied in Fig. 3. The memory capacitor is first charged for 10 s at a bias voltage of 10 V. Then, the decayed capacitance measurement was carried out under a -3 V bias voltage. It can be seen that after 700 s of stress, the decayed capacitance for the memory capacitor is only about 3%, suggesting very good charge retention characteristics. According to the work of Kim *et al.*, the storage charges in the localized nanocrystals exhibit long-term retention property.³⁰ In our experiments, SrTiO₃ nanocrystals are well localized at the middle of the dielectric (Lu₂O₃) matrix, hence, the only possibility of charge loss is the tunneling out via the tunneling barrier. Therefore, the stored charges in the localized nanocrystals exhibit long-term retention properties.

FIG. 3. Normalized capacitance decay characteristics for SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ dielectric memory device.

In summary, we have developed a method to fabricate the memory structure of SrTiO₃ nanocrystals embedded in amorphous Lu₂O₃ high-*k* dielectric using pulsed laser deposition. The mean size and area density of the SrTiO₃ nanocrystals are estimated to be about 4 nm and $8 \times 10^{11} \text{ cm}^{-2}$, respectively. Good performances in terms of large memory window and long data retention were observed. Using this proposed method, we are also able to control the size and the density of nanodots to be deposited by slight modification to the target.

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