Anomalous polarization switching in organic ferroelectric field effect transistors

Nguyen, Chien A.; Lee, Pooi See; Ng, Nathaniel; Su, Haibin; Mhaisalkar, Subodh Gautam; Ma, Jan; Boey, Freddy Yin Chiang

2007

Nguyen, C. A., Lee, P. S., Ng, N., Su, H., Mhaisalkar, S. G., Ma, J., et al. (2007). Anomalous polarization switching in organic ferroelectric field effect transistors. Applied physics letters, 91(4).

https://hdl.handle.net/10356/95006

https://doi.org/10.1063/1.2757092

Anomalous polarization switching in organic ferroelectric field effect transistors

C. A. Nguyen,[a] P. S. Lee,[b] N. Ng, H. Su, S. G. Mhaisalkar, J. Ma, and F. Y. C. Boey
School of Materials Science and Engineering, Nanyang Technological University, Singapore 639798, Singapore

(Received 19 April 2007; accepted 19 June 2007; published online 27 July 2007)

The authors demonstrate organic ferroelectric field effect transistors using poly(vinylidene fluoride-trifluoroethylene) as dielectric in bottom common gate and patterned gate devices. Drain current hysteresis is resulted from the dipole switching at channel region due to gate-source bias. For common gate device, an additional anomalous polarization switching is observed due to gate-drain bias. This switching has no effect on the hysteresis direction yet incurs a strong peak in the off drain current leading to unstable and uncontrollable off state in memory device. Reduction of gate-drain overlapping using patterned metal gate shows diminishing the anomalous switching hence improves performance of the ferroelectric transistors. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2757092]

Organic electronics have been expected to emerge as an alternative besides Silicon technology for simple circuitry devices.[1,2] It enables device fabrication at low temperature, on flexible substrates and with high throughputs. For ferroelectric field effect transistor (Fe-FET) devices,[3,4] organic ferroelectric materials are usually sought after to be compatible with the processing of the organic semiconductors. One of the most studied materials are poly(vinylidene fluoride-trifluoroethylene) P(VDF-TrFE) copolymers due to good remnant polarization and stable Curie temperature.[5,6] Recently, Fe-FETs with P(VDF-TrFE) have been reported with promising memory on/off ratio,[7] low voltage operation,[8] and possibility of large-scale production by lithography.[9]

Most of the reported devices were fabricated with a common gate structure that creates overlapping regions between gate and source/drain electrodes.[7–10] These regions of polymer-metal sandwiching make perfect capacitors for polarization switching. As a result, the source-drain bias (V_{SD}) is always applied at much smaller amplitude than the gate-source bias (V_{GS}) so that the potential difference from gate to source (V_{GS}) and drain (V_{GD}) is minimal. Polarization switching will then be similar throughout the bulk dielectric. When V_{SD} increases to reach channel pinch-off regime of the transistor, the difference of V_{GS} and V_{GD} is equal to V_{SD} value. As gate bias is swept, V_{GS} and V_{GD} will overcome the ferroelectric coercive fields and switch the dipoles at two different gate biases for each forward and reversed sweeping cycles. This will result in "double switching" by the gate-source and gate-drain sandwiching regions which eventually leads to degradation in off state behavior.

In this letter, we investigate the existence of an anomalous polarization switching in the common gate organic Fe-FET and study its effects to the retention and hysteresis of drain current. We also demonstrate the organic Fe-FET using a patterned metal gate, which shows minimization of double-switching due to reduction in overlapping of gate and source/drain electrode with improved memory performance.

To understand different types of polarization switching, we first measure the polarization hysteresis with potential applied to the vertical direction (gate to source/drain) and horizontal direction (source to drain) using a common bottom-gate device structure, as shown in Fig. 1(a). The metal-polymer-metal capacitor was fabricated by spin-coating P(VDF-TrFE) solution [with methyl ethyl ketone (MEK) solvent and concentration of 50 mg/ml] at 1000 rpm on a precleaned indium tin oxide (ITO) glass, as described in Ref. 10. The polymer film was subsequently annealed in Nitrogen ambient at 140 °C and followed by depositing the

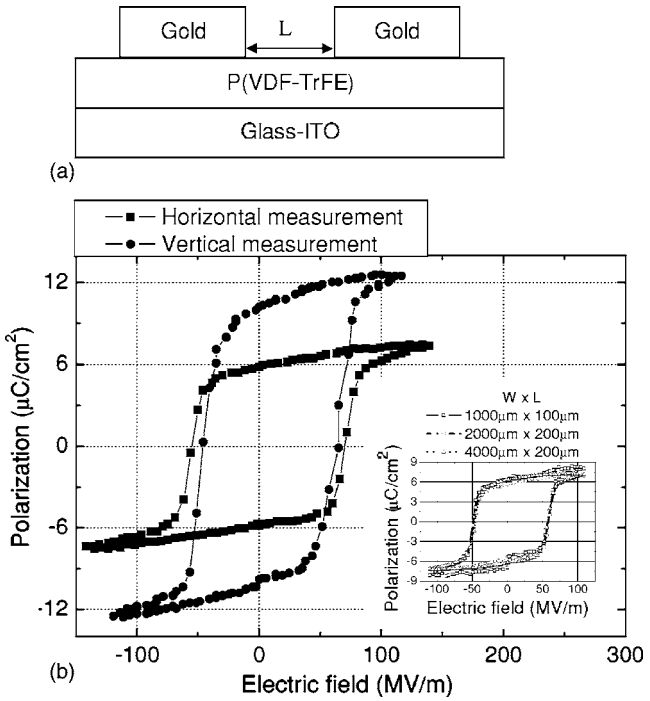

FIG. 1. (a) Electrode structure for hysteresis measurement. P(VDF-TrFE) film thickness is 1.2 μm. Bias was applied to bottom ITO and one of gold electrodes for vertical test and to both gold electrodes for horizontal test. (b) Saturated polarization hysteresis of horizontal and vertical measurements. The inset shows hysteresis curves for different electrode and channel dimensions: *L*—channel length and *W*—channel width.

[a]Electronic mail: acnguyen@pmail.ntu.edu.sg
[b]Electronic mail: pslee@ntu.edu.sg

gold (source/drain) electrodes by thermal evaporation. The electrodes are of 500 μm in width and various lengths, as shown in the inset of Fig. 1(b). The polarization hysteresis was measured by Radiant HV6000 ferroelectric tester. Biases were applied to either source or drain electrode and the ITO gate in the "vertical" measurement and to both source and drain electrodes with floating gate in the "horizontal" measurement.

Figure 1(b) shows the saturated polarization hysteresis for both of the vertical and horizontal measurements. The vertical data are consistent with the reported values for P(VDF-TrFE) (70–30 mol %) copolymer with coercive field of $\sim|50|$ MV/m and remnant polarization of $\sim|10|$ μC/cm^2.[5,6] The horizontal measurement data show similar coercive values while the remnant values are about 60% of the vertical ones. The similar coercive values indicate that the polarization switching in both cases has the same characteristics with bulk polymer. Based on these observations, we conclude that the tested device should behave as two identical capacitors in back-to-back series connection during the horizontal measurement. As a result the measured remnant polarization was almost half of the bulk value. To further confirm, we applied the horizontal measurement to devices with various electrode and channel dimensions [inset of Fig. 1(b)]. The obtained coercive and remnant data are independent of the separating gap lengths or widths. Hence, this confirms the possibility of polarization switching caused by varied bias between source and drain electrodes in transistor device.

To examine this phenomenon in transistor operation, 80 nm thick pentacene was thermally evaporated (pressure of 5×10^{-7} torr and speed of 0.1–0.2 Å/s) onto the P(VDF-TrFE) layer, followed by deposition of source/drain electrodes as described earlier. Channel length and width are 1000 and 100 μm, respectively. The transistor was characterized using Keithley 4200 semiconductor analyzer in a dark vacuum chamber. The I_D-V_G measurement was done by cyclically sweeping the gate bias while keeping constant drain potential with respect to the source. Figures 2(a) and 2(b) show I_D-V_G and I_G-V_G data for the ferroelectric transistor measured at three drain voltages (V_{SD}). There are two switching current profiles existing in the I_G-V_G curve observed as current peaks in Fig. 2(b). The one with two peaks locating at ±80 V is caused by the vertical potential between gate and source electrodes (V_{GS} switching) and independent of V_{SD}. The other two peaks shifted to more negative bias accordingly to the increased V_{SD}, which was caused by the anomalous polarization switching resulting from the gate-drain potential difference V_{GD} with a dependence on the magnitude of V_{SD} (V_{GD} switching). The current peaks' values are shown in Table I. The relationship of V_{SD}, V_{GS}, and V_{GD} can be generalized as

$$V_{GD} = |V_{GS}| + V_{SD},$$

with $V_{GS}<0$, for positive-to-negative switching and $V_{GS}>0$, for negative-to-positive switching.

Figure 3 shows plots of equipotential contours determined in the P(VDF-TrFE) layer sandwiched by gate and source/drain electrodes under various fields applied at gate. The results were obtained by solving Maxwell equation (Gauss law) using finite difference method.[11] In considering only the distribution of electric field in the dielectric layer, polarization, and charge density terms were ignored. The

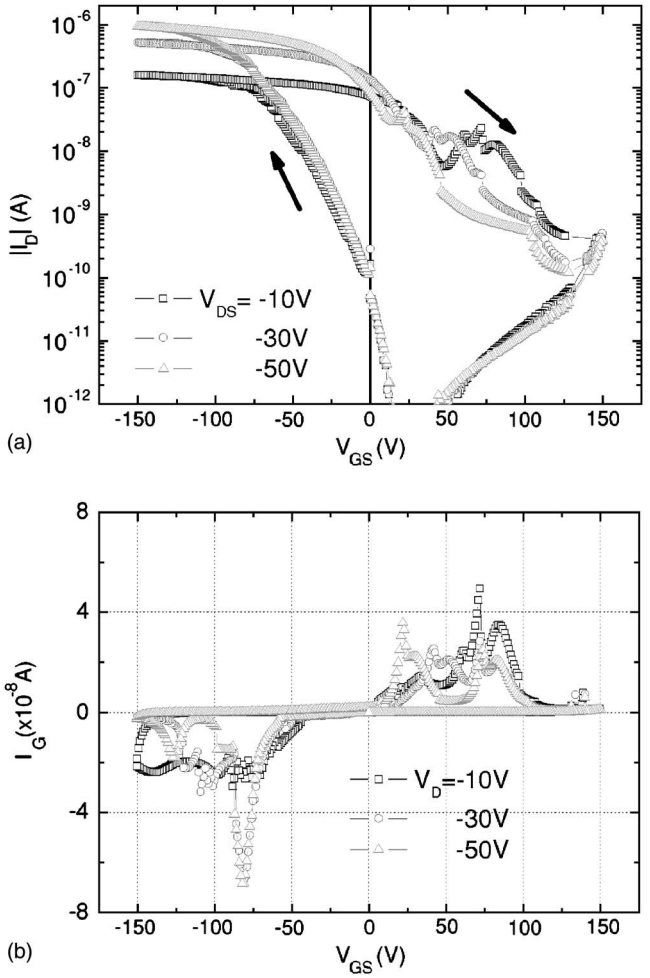

FIG. 2. Electrical characterization of common bottom gate Fe-FET device with 1.6 μm thick P(VDF-TrFE) dielectric layer (a) I_D-V_G. Arrows show the direction of drain current hysteresis. (b) I_G-V_G.

simulated biases are relatively scaled to the real testing voltages. The potentials are kept constant at source (V_S=0) and drain (V_D=−0.5 or −0.1). As the gate is operative with bias reaching −1 (on state) or +1 (off state), the contour density is distributed more densely at the region under the source or the drain, respectively, in the case of V_D=−0.5. For the case that V_{DS} is much smaller than V_{GS} (V_D=−0.1), the contour density is almost uniform in the dielectric layer during the operative stages of sweeping gate bias. This agrees with our experiment data (in Table I) for the order of V_{GS} and V_{GD} switchings in the negative and positive sweeping cycles, as discussed above. It is also seen that as gate bias approaches zero and switches its polarity, the contour density is only redistributed below the drain electrode. Hence this likely caused the earlier switching to the opposite polarization of the region between gate drain and reduced the accumulation

TABLE I. Tabulated switching current peaks for data shown in Fig. 2(b).

Source-drain bias V_{SD} (V)	Switching peaks by V_{GS} (V)	Switching peaks by V_{GD} (V)
−10	−80/+80	−88/+70
−30	−80/+78	−106/+48
−50	−80/+75	−126/+26

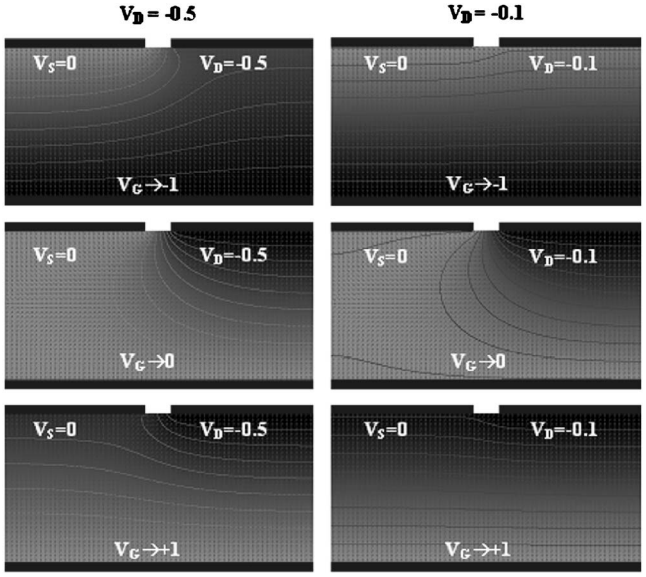

FIG. 3. Plots of equipotential contours calculated for transistor electrode structure, as shown in Fig. 1(a).

of charges in the channel, which led to reduction in I_D retention.

To remove the anomalous V_{GD} switching, as observed in Fig. 2, bottom patterned gate device was fabricated, as shown in Fig. 4(a). Patterned gold gate was formed by thermal evaporation through a shadow mask on cleaned glass substrate. The overlapping between the gate-drain electrodes is minimized by keeping the gate and channel gap of same dimensions and aligning the gate electrode edges to those of source and drain. Similar I_D-V_G tests were applied to the device. The data presented in Fig. 4(b) clearly show the removal of the shifting V_{GD} switching peaks in the gate current I_G-V_G profile as well as in the off state of I_D-V_G current. The maintenance of hysteresis and direction of drain current indicates that the polarization switching mainly establishes in the channel region. The device performance is improved with the good I_D retention as well as a more constant and low leakage current during off state.

In summary, we have studied two different types of polarization switching in an organic ferroelectric field effect transistor using bottom common gate. One is resulted from biases between gate and source that contribute to drain current hysteresis, while the other is caused by potential difference between the gate and drain that closely follows drain voltages. Field distribution in the ferroelectric layer with regards to the potential differences at the electrodes is directly responsible to the sequential polarization switching, which leads to unstable high off leakage current hence resulting in uncontrollable off state of the memory device. Reduction of electrode overlapping to minimize the gate-drain polarization switching can result in an improved device performance,

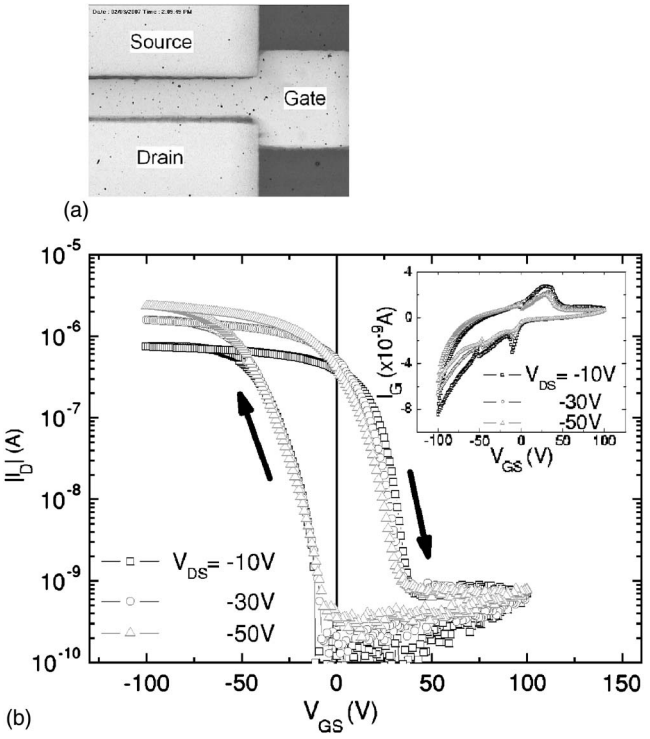

FIG. 4. (a) Optical micrograph of patterned gate Fe-FET device. (b) I_D-V_G characteristic. Arrows show hysteresis direction. The inset shows I_G-V_G data.

which is applicable to integrated nonvolatile memory devices.

One of the authors (C.A.N.) would like to acknowledge the research scholarship awarded by Nanyang Technological University. This work is supported by A^*Star under Grant No. 0521170032 and NTU Acrf Grant No. RG26/05.

[1] J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, and P. Drzaic, Proc. Natl. Acad. Sci. U.S.A. **98**, 4835 (2001).
[2] D. M. de Leeuw, G. H. Gelinck, T. C. T. Geuns, E. van Veenendaal, E. Cantatore, and B. H. Huisman, Tech. Dig. - Int. Electron Devices Meet. **2002**, 293.
[3] J. F. Scott, *Ferroelectric Memories in Advanced Microelectronics* (Springer, Berlin, 2000), Chap 12, p. 175.
[4] A. Sheikholeslami and G. Gulak, Proc. IEEE **88**, 667 (2000).
[5] A. J. Lovinger, Science **220**, 1115 (1983).
[6] T. Furukawa, Science **71–72**, 183 (1997).
[7] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. de Leeuw, Nat. Mater. **4**, 243 (2004).
[8] R. C. G. Naber, B. de Boer, P. W. M. Blom, and D. M. de Leeuw, Appl. Phys. Lett. **87**, 203509 (2005).
[9] G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. de Leeuw, R. C. G. Naber, and P. W. M. Blom, Appl. Phys. Lett. **87**, 092903 (2005).
[10] C. A. Nguyen, P. S. Lee, and S. G. Mhaisalkar, Org. Electron. **8**, 415 (2007).
[11] W. Zhang and K. Bhattacharya, Acta Mater. **53**, 199 (2005).