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Kwong, Dim Lee

2012

Singh, P., Park, W.- T., Miao, J., Shao, L., Kotlanka, R. K., & Kwong, D. L. (2012). Tunable piezoresistance and noise in gate-all-around nanowire field-effect-transistor. Applied physics letters, 100(6), 063106.

<https://hdl.handle.net/10356/95436>

<https://doi.org/10.1063/1.3683516>

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Citation: *Appl. Phys. Lett.* **100**, 063106 (2012); doi: 10.1063/1.3683516

View online: <http://dx.doi.org/10.1063/1.3683516>

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Tunable piezoresistance and noise in gate-all-around nanowire field-effect-transistor

Pushpapraj Singh,^{1,2} Woo-Tae Park,^{2,a)} Jianmin Miao,^{1,2} Lichun Shao,² Rama Krishna Kotlanka,² and Dim-Lee Kwong²

¹*School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore 639798*

²*Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Science Park-II, Singapore 117685*

(Received 16 September 2011; accepted 14 January 2012; published online 7 February 2012)

The piezoresistance and noise of n-type gate-all-around nanowire field-effect-transistor (NWFET) is investigated as a function of gate bias. With narrow gate bias span of 0.6 V near threshold region, the piezoresistive coefficient of NWFET enhances up to seven times from $29 \times 10^{-11} \text{ Pa}^{-1}$ to $207 \times 10^{-11} \text{ Pa}^{-1}$ under compressive and tensile strain conditions. Results reveal that the low frequency noise is reduced when operated in subthreshold region. The higher piezoresistive coefficient and reduced noise improve the sensor resolution (minimum detectable strain) by sixteen times. NWFET operates at low bias with higher piezoresistance and signal-to-noise ratio and offers promising applications in strain sensors. © 2012 American Institute of Physics. [doi:10.1063/1.3683516]

Piezoresistive effect of silicon has been extensively used for numerous applications in physical transducers.^{1–3} Recent advances in technology have made it possible to realize nano-devices and many efforts have been made to increase the piezoresistive coefficient by shrinking the dimension. Piezoresistive measurements have been carried out on nanowires and giant piezoresistance was claimed due to the reduced dimensions ($70 \text{ nm} < \text{diameter} < 370 \text{ nm}$) and larger surface/volume ratio effects.^{4,5} The higher piezoresistance was also reported in partially depleted nanowires, and substrate bias voltage is used to reduce the carriers inside nanowire channel.⁶ The anomalous piezoresistive effect has been interpreted as a combined effect of electric field and mechanical stress on constricted current channel. Though higher sensitivity was preferred, there have been large differences in piezoresistive coefficient obtained by different researchers and giant piezoresistance in nanowires was not successfully reproduced. It was accounted that the apparent giant piezoresistance^{4,6} was not because of applied stress but due to the charge trapping and subsequent relaxation at the exposed SiO₂ layers on the wire surfaces.⁷ The combined effect of low-dimension and biasing-voltage on nanowire piezoresistance and intrinsic noise is an unknown physical phenomenon, motivating a separate study before claiming nanowire as better sensing element.

In this letter, gate-all-around nanowire field-effect-transistor (GAA NWFET) is proposed as piezoresistive sensing element and its electromechanical properties are characterized. Gate surrounds the nanowire channel in GAA structure, which provides easier carrier depletion with the use of low gate bias. The surrounding gate also provides complete shielding from environmental charges and prevents the humidity effects to change the drain current⁷ that are independent of stress. The strain-induced change in drain current is

experimentally verified, and the gate bias effects on piezoresistance and drain current noise are analyzed. Results reveal that GAA NWFET can be used as miniaturized and ultrasensitive sensing element for nanomechanical sensors.

GAA n-type NWFETs were fabricated on 8 in. (100) silicon-on-insulator (SOI) wafers with a top device layer of 117 nm and 145 nm buried oxide (BOX). Silicon fins of width 50 nm were defined through deep ultraviolet (DUV) patterning followed by resist trimming. These silicon fins were oxidized at 875 °C for 5 h, which results in twin nanowires (Fig. 1(a) inset). After the nanowire formation, 4 nm SiO₂ was thermally grown followed by 130 nm amorphous silicon (α -Si) by LPCVD. The α -Si was further patterned and used as gate electrode (Fig. 1(a)). Next, source and drain implantation was carried out followed with activation annealing to allow the dopants to diffuse through the gate electrode and thick source and drain regions below the gate. Finally, standard metallization process completed the formation of gate-all-around nanowire FET device.

The piezoresistive properties of JL-NWFET were investigated using a four point bending set-up equipped with probe station. The fabricated wafer was diced to rectangular wafer slices and transistors channel direction was placed accordingly to generate the mechanical strain in the desired direction. A wafer slice was positioned on two bottom blades and identical weight (W) was applied on top of the two blades to bend the chip (Fig. 1(b)). By switching the position of the top and bottom blades, either tensile or compressive strain can be generated while bending the wafer upwards or downwards. Devices (on the test chip) between the inner blades experienced uniform and uniaxial strain after loading the weight. Strain gauge was attached on the test chip to measure the actual strain during the weight loading.

NWFETs with 120 nm channel length are tested and the dependence of the electrical characteristics on mechanical strain is investigated using a semiconductor parameter analyzer (HP4156B). When the gate bias (V_{GS}) exceeds the

^{a)} Author to whom correspondence should be addressed. Electronic mail: parkwt@ime.a-star.edu.sg.

FIG. 1. (Color online) (a) SEM picture of completed GAA NWFET. 120 nm-long twin Si NWs attached with source/drain (inset image before gate formulation). (b) Schematic diagram of the four-point bending apparatus designed for the measurements.

threshold voltage (V_{TH}), an inversion layer forms at Si-SiO₂ surface and drain current (I_{DS}) flows once a voltage is applied between source and drain. The electrical characteristics were measured and NWFET devices exhibit subthreshold slopes of ~ 75 mV/dec with $V_{TH} \sim -150$ mV.

Piezoresistive coefficients of the NWFET device is found by applying a sequence of controlled strains and measuring the corresponding changes in the drain current ($\Delta I_{DS}/I_{DS}$). Under the same strain, drain current change (%) is found higher at the lower gate bias (Fig. 2(a)). Consequently, the linear square fit slope also increases for lower gate bias, indicating a higher gauge factor ($K = (\Delta I_{DS}/I_{DS})/\epsilon$) in subthreshold region (Fig. 2(b)). The longitudinal piezoresistive coefficient (π_l) is defined as the relative change in drain current per unit strain

$$\pi_l = \frac{1}{E} \left(\frac{\Delta I_{DS}/I_{DS}}{\epsilon} \right) = K/E, \quad (1)$$

where E (169 GPa) is the silicon Young's modulus. As higher gauge factor is measured in subthreshold region ($V_{GS} < V_{TH}$), π_l enhances up to seven times $\sim 207 \times 10^{-11}$ Pa⁻¹ ($V_{GS} = -0.4$ V) compared to $\sim 29 \times 10^{-11}$ Pa⁻¹ for inversion region ($V_{GS} = 0.4$ V).

Piezoresistance in silicon surface inversion layers have been interpreted due to the strain-induced changes in energy-band structure and inter-valley scattering effects.⁸ The energy of conduction-band minima changes under the applied strain and carriers redistribute among the valleys of dissimilar effective masses.⁹ The strain-enhanced electron mobility originates mainly from two factors (1) the reduction in the average effective mass due to the carrier redistribution and (2) the change in the carrier scattering rate due to the

energy-band splitting.¹⁰ With increasing gate voltage, the surface electric field confines carrier motion perpendicular to the surface, which also influence electron population and scattering of electrons. Reduced gauge factor is observed at higher gate bias (Fig. 2(b)) and possible reason can be the reduction in effective carrier mobility, which may be attributable to stronger confinement effects at high vertical electric field.

Strain may change the NWFET drain current from two aspects: such as change in carrier mobility and threshold voltage. For inversion region, the drain current change dependence on the carrier's mobility and threshold voltage (V_{TH}) is described as¹¹

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \mu}{\mu} - 2 \frac{\Delta V_{TH}}{V_{TH}} \left(\frac{V_{TH}}{V_{GS} - V_{TH}} \right), \quad (2)$$

where μ represents the effective electron mobility in the channel. Fig. 3 shows that the V_{TH} reduces ~ 4 mV under the strain equal to $385 \mu\text{m/m}$. As the conduction band structure shifts under the mechanical strain, the V_{TH} reduction is attributable to the reduced band bending required to attain inversion region.¹² At the onset of strong inversion ($V_{GS} > V_{TH}$), NWFET drain current becomes linearly dependent on the $(V_{GS} - V_{TH})$ and small variation in threshold voltage (~ 4 mV) can be neglected for the drain current change. Drain current change is then considered mainly from mobility variation and second term in Eq. (2) can be neglected.

However in subthreshold region, the drain current increases exponentially ($I_{DS} \approx I_0 e^{(V_{GS} - V_{TH})/mV_T}$) with $(V_{GS} - V_{TH})$, where I_0 = drain current at $V_{GS} = V_{TH}$, the thermal voltage $V_T = kT/q$, and m is the slope factor. The drain

FIG. 2. (Color online) (a) Drain current variations vs longitudinal strain under different biasing conditions (inversion and subthreshold region). (b) Gauge factor and MDS variation at different biasing condition. MDS is minimum detectable strain of the sensor and ϵ is the applied strain.

FIG. 3. (Color online) I_{DS} - V_{GS} characteristics of n-NWFET for 0 to 385 $\mu\text{m/m}$ uniaxial longitudinal tensile strain at $V_{DS} = 100$ mV.

current change dependence on the threshold voltage can be described as

$$\frac{\Delta I_{DS}}{I_{DS}} = e^{(\Delta V_{TH}/mV_T)} - 1. \quad (3)$$

The calculations from Eq. (3) indicates that the small reduction in threshold voltage (~ 4 mV) can enhance the drain current significantly ($\sim 16\%$ for $m=1$, $\sim 8\%$ for $m=2$) in subthreshold region.

To investigate the gate bias effect on drain-current fluctuation, low frequency noise (LFN) measurements were performed using a battery-powered SR570 low-noise current preamplifier and a HP35670A dynamic signal analyzer. Fig. 4 shows the frequency dependence of the measured drain current noise spectral density (S_{ID}) at different gate bias. Noise spectral density shows significant variation up to five orders of magnitude within 0.6 V gate bias spans.

In inversion region ($V_{GS} > V_{TH}$), higher gate voltage confines the channel carriers closer to the nanowire surface, which results carriers trapping and detrapping at silicon oxide interface (number fluctuation- ΔN theory). These trapped carriers generate scattering with channel carriers near to nanowire interface and influence the mobility (mobility fluctuation- $\Delta\mu$ theory), and thus produce higher LFN at increas-

FIG. 4. Drain-current noise power spectral density (S_{ID}) versus frequency in the n-NWFET transistor with nanowire width ~ 10 nm and channel length = 120 nm.

ing gate bias.¹³ In sub-threshold ($V_{GS} < V_{TH}$), alternatively, the surface scattering remains low due to the physical separation of carriers from the interface and ΔN has no influence on the LFN. Fig. 4 shows significant spectral noise reduction in subthreshold region, indicating that the lower drain current noise is caused due to $\Delta\mu$ theory.¹⁴

To measure the performance of the strain sensor, we use the term minimum detectable strain (MDS). The MDS is the noise equivalent strain, which is defined as the drain current noise amplitude (A) divided by the strain sensitivity

$$MDS = \frac{A}{(\Delta I_{DS}/\epsilon)} = \frac{A}{KI_{DS}}. \quad (4)$$

From the measurements of the spectral current noise at 2 Hz, I_{DS} and the gauge factor, the MDS is calculated to be $\sim 2.4 \times 10^{-6}$ for inversion mode ($V_{GS} = 0.4$ V) as shown in Fig. 2(b). However, with higher gauge factor and the lower $1/f$ noise, MDS is found sixteen times lower $\sim 1.5 \times 10^{-7}$ for subthreshold mode ($V_{GS} = -0.2$ V). For $V_{GS} = -0.4$ V, the gauge factor is higher but the A/I_{DS} term also increases making the MDS bigger compared its value when $V_{GS} = -0.2$. For small strains, the signal-to-noise ratio (SNR) is defined as the sensor signal power divided by incorporated noise power¹⁵

$$SNR = \frac{K^2 \epsilon^2}{A}. \quad (5)$$

The results suggest that both gauge factor and noise amplitude depend on the applied gate voltage, provide an easier way to enhance SNR by operating NWFET at particular gate bias. Compared to the reported SNR values for carbon-nanotubes FET ($SNR \sim 10^2$)¹⁵ and planar MOSFET ($SNR \sim 10^4$),¹⁶ GAA NWFET based sensing element exhibits much higher SNR ($\sim 10^9$) with superior MDS value in subthreshold mode.

Since the report from He and Yang,⁴ researchers investigated the giant piezoresistance of nanowires. The reported gauge factor values were as high as 6674 for $\langle 111 \rangle$ silicon. Neuzil *et al.* used the biasing effect to pinch-off the current channel and reported maximum gauge factor of 5400.⁶ Recently, Milne *et al.* revealed no large gauge factor in nanowires and the previous reported values are most likely due to dielectric surface relaxation effect independent of applied stress. In this work, using gate-controlled nanowire FETs, we also did not measure any giant piezoresistance in nanowires in dimensions as low as 10 nm width. However we have measured and verified the “tuning” effect of piezoresistance, and first reported the low noise that changes with gate bias. Because of this low noise, the MDS of the sensor remains as an attractive choice for physical sensors. Further optimization of channel geometry and doping will further enhance strain resolution.

The authors are grateful to Dr. Navab Singh for helpful discussions. The authors acknowledge the financial support from Nanyang Technological University and Institute of Microelectronics (A*Star science and research council Grant 0921480069) for the project.

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