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Effect of Ge Diffusion on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ High Electron Mobility Transistors on a Thin Silicon-On-Insulator

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In this letter, the effect of Ge diffusion at the gate area of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistors (HEMTs) on a thin silicon-on-insulator (SOI) substrate has been investigated. The pinch-off voltage shifted toward enhancement mode type operation behavior due to the Ge diffusion through the surface of the thin GaN cap layer. An anomalous hump observed in high frequency C-V plot is due to the electron confinement at the Ge-GaN/AlGaN interface. The threshold voltage reduces by 0.8 to 1.0 V after Ge diffusion. The drive current and the transconductance further reduced as compared to the control sample due to the parallel channel formation at the top Ge-GaN/ $\text{Al}_x\text{Ga}_{1-x}\text{N}$ interfaces.

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The AlGaN/GaN-based high electron mobility transistors (HEMTs) are suitable for high power and high frequency electronic applications. The GaN-based power amplifiers offer superior performances than GaAs or Si-based transistors. The state of the art Si wafer processing platform with a lower cost and coupled with mature back-end technologies have driven the research direction for GaN integration onto Si substrate. However, the high lattice and thermal mismatch between Si and GaN lead to epilayer cracking, high density of threading dislocations and severe wafer bowing due to in-plane strain formed by the AlGaN/GaN heterostructures.¹⁻³ The wafer bowing of GaN/AlGaN structures on 150 to 200 mm floatzone high resistive Si substrate generates bowing-induced electrical non-uniformities which limit large scale commercial applications.

To overcome the issues of wafer bowing, usually thick Si substrates are used to compensate the in-plane stress for thicker GaN on silicon wafer development.⁴ The alternative approach is to use a thin silicon device layer on an SiO_2 substrate for the growth of GaN/AlGaN layers. In the case of GaN growth on a very thin silicon-on-insulator (SOI) substrate (top Si thickness <50 nm), the crystalline quality of initial AlN nucleation is influenced by the high growth temperatures (typical surface temperature about 1100°C), where the softening and viscous nature of buried oxide contributes to the propagation of dislocations at the heterointerfaces. Compared to bulk Si, dislocation movement by thin Si template on viscous of buried oxide layer,⁵ leads to a change in the structural quality of overgrown nitride layers. When substrate diameter is larger, the strain balance mechanism could lead to a reduce wafer bowing compared to the case of growth of GaN directly on high resistive bulk Si substrates. A low bow epiwafer may lead to much uniform electrical property of two-dimensional electron gas (2DEG) interfaces. The 2DEG-based AlGaN/GaN HEMTs are generally normally-on depletion-mode (D-mode) devices. But normally-off enhancement-mode (E-mode) operation is necessary to overcome the circuit design complexity. There are a few ways to tune the threshold voltage to achieve E-mode HEMTs such as recessed-gate,⁶ fluoride plasma treatment,⁷ and p-type AlGaN cap⁸ or InGaN cap.⁹

In this letter, we report on the innovative approach of realization of 2DEG AlGaN/GaN heterostructures on 150 mm diameter thin SOI(111) substrate where Si overlayer thickness is about 35 nm. The HEMT fabrication process of threshold voltage tuning toward the E-mode type behavior is achieved by using the Ge diffusion in top thin GaN and AlGaN barrier layers. The carrier confinement, the threshold voltage shift measured from high frequency C-V, and the device drain currents are studied.

The $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ -based heterostructures are grown on 150 mm diameter floatzone SOI(111) substrates by metal organic chemical vapor deposition. The SOI(111) substrates, with the thin top Si overlayers of about 30–35 nm and buried oxide thickness of about 70–75 nm, were prepared on handle Si substrates of thickness 650–675 μm (starting Si resistivity of $\sim 2500 \Omega \text{ cm}$) by the separation by implantation of oxygen (SIMOX) process. About 100 nm of AlN buffer was first grown on top of the thin SOI overlayer, followed by $\sim 2.1 \mu\text{m}$ of intermediate Al(GaN)/GaN superlattice layers. About $\sim 1.0 \mu\text{m}$ carbon-doped semi-insulating GaN was overgrown followed by the active layers consist of about 1.0 nm AlN spacer, ~ 20 –25 nm $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer and a thin ~ 1.5 nm GaN cap layer. Wafer bowing measured from GaN on SOI and GaN on bulk-Si substrates is about 40 μm and 80 μm , respectively. Despite similar growth conditions of epilayers, the heterostructures on SOI substrates show a much uniform sheet resistivity profile with a variation within 20% with an average sheet resistance of about 350 Ω/sq estimated from Hall effect, whereas we observed a variation of about 27% for the case of bulk Si with an average value of 430 Ω/sq . The average sheet carrier concentration of such 2DEG layers is about $9.5 \times 10^{12} \text{ cm}^{-2}$ with a mobility of 1920–1940 $\text{cm}^2/\text{V s}$ at the wafer center.

The device fabrication process consists of several steps: (i) active area was defined by optical lithography. (ii) After active lithography the mesa isolation etch was formed using Cl_2/BCl_3 dry plasma etching. (iii) The gate level photolithography and Ge deposition followed by lift-off process was carried out to deposit 10 nm thick Ge at gate area. (iv) Then the S/D was patterned by photolithography and ohmic metal Ti/Al/Ni/Au (15/120/40/150 nm) stack was deposited using electron beam evaporation. (v) After metal lift-off, the wafers were annealed using RTA at 825°C for 60 s in an N_2 ambient to prepare ohmic contacts at S/D and the diffusion of Ge at top GaN cap and AlGaN layer in gate area, respectively. (vi) Schottky gate with several channel length were formed by Ni/Au E-beam evaporation and subsequent lift off process. For a comparative study, both Ge gated and control samples were fabricated in a same process run. To analyze the layer quality of the as-grown film, high-resolution X-ray diffraction (HRXRD) and cross-sectional scanning transmission electron microscopy (STEM) experiments were carried out. The cross-sectional TEM micrographs of the AlGaN/GaN heterostructure grown on SOI substrate are shown in Fig. 1, where the z-contrast STEM images with top GaN/AlGaN/AlN interfaces show accurate thicknesses of layers. Figures 1b and 1c show HRXRD reciprocal space maps (RSM) of full HEMT structure. The Al content in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is about 24–25% in our HEMT barrier layer as estimated by the RSM maps.

To utilize such high electron mobility structure, both standard D-mode and Ge-diffused HEMTs are fabricated. The high frequency

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Figure 1. (a) The TEM image of full structure showing the thickness of individual epilayers and buffers with embedded GaN on AlN/SOI(111) interface. (b) The high-resolution STEM image of the top active GaN/AlGaIn/AlN/GaN layers. The HRXRD reciprocal space maps representing (c) (114) asymmetric and (d) (004) symmetric reflexes of the full HEMT structure.

gate to channel capacitance voltage (C-V) was used to study the effect of Ge. Fig. 2a shows the high frequency CV-GV for both Ge (W/Ge) and without Ge (W/O Ge) samples. The diffusion of Ge is confirmed from secondary ion mass spectroscopy analysis. The CV curve of a Schottky gate on AlGaIn/GaN looks similar to the CV characteristics from a metal insulator semiconductor structure with a significant long flat terrain region from both the samples. The higher bandgap AlGaIn behaves as a dielectric and such 2DEG is formed in GaN at AlGaIn/AlN/GaN interface. Thus a high electron concentration beneath the AlGaIn/AlN layers is responsible for the constant long flat terrain capacitance for a wide range of gate bias. The length of the C-V curve plateau is longer for W/O Ge sample compared to W/Ge. Osvald¹⁰ reported that higher sheet carrier concentration leads to longer plateau region. After annealing at 825°C the Ge diffuse into the AlGaIn layer. Group IV material Ge is the n-type dopant for GaN/AlGaIn and hence AlGaIn layer to be n-type doped after Ge diffusion at the gate region. We believe that Ge compensating some degree of positive sheet charge on the AlGaIn surface which reduces the polarization effect. The lowering of polarization at gate region leads to lower carrier concentration (2DEG) at AlGaIn/GaN heterointerface. The effective AlGaIn thickness also slightly reduces due to the Ge diffusion at the gate region. Thus the combination of lower 2DEG concentration and effective thinner AlGaIn contribution shorten the flat terrain region of CV curve for W/Ge sample compared to control sample. The maximum capacitance (C_{max}) is higher for W/Ge sample is due to the lower thickness contribution of AlGaIn layer. The slope of CV curve for both samples is similar which indicates that the doping level at GaN layer is remaining unchanged. The minimum capacitance is observed for control sample at -4.65 V, which is the pinch-off voltage, V_{th} . A special feature in CV curve observed for W/Ge sample. The capacitance value started to reduce from constant flat region due the depletion of AlGaIn and GaN layer. As the bias is more and more negative, the electrons are drifted away from the surface and eventually observed a minimum capacitance. But W/Ge sample shows a first minimum at -3.15 V and then a hump at -3.45 V before reducing to final minimum value. The origin of hump in CV curve is probably due to the combination of interface state density

Figure 2. The high-frequency capacitance voltage (C-V) and conductance voltage (G-V) curves (a), frequency dispersion characteristics of (C-V) (b) and (G-V) (c) for W/ Ge and W/O Ge samples of AlGaIn/GaN heterostructure with Ge and without Ge at gate space.

and charge build up at the band offsets region for this voltage. The deposited Ge thickness is 10 nm and distribution of Ge through the depth of the film was determined using the secondary ion mass spectrometry (SIMS) in a time-of-flight spectrometer (ToF-SIMS-IV from ION-ToF GmbH) with detection of negative ions. The sputtering beam used was Cs 1 keV and 10 nA current; pulsed analysis beam was Bi 25 keV and 0.5 pA current. The sputtering rate during spectral recording was about 3.6 nm/min and about top 3 nm SIMS data is influenced by the experimental limitations. The ToF-SIMS analysis results in Fig. 3 show that Ge diffuses to GaN/AlGaIn layer and a thin Ge cap layer remains after diffusion. The remaining Ge on top of GaN/AlGaIn layer modifies the band structure as shown in Fig. 4. The diffused Ge will cause n+ doping at GaN cap/AlGaIn layer and the presence of Ge cap layer would cause threshold voltage change toward enhancement mode type due to the combined effect of lower bandgap of top Ge cap layer with n+ doping at GaN/AlGaIn layer. The presence of a lower bandgap Ge on GaN cap or AlGaIn layer causes a large conduction band offset. As the bias increases from positive to negative, the electron start to deplete from metal/semiconductor interface but large conduction band offset creates a barrier for pile up of electrons up to a certain bias range. The consequence of charge build up is the increase of capacitance as shown in Fig. 2a for W/Ge sample at -3.4 V. Further increase of negative bias provides sufficient energy to the electrons to tunnel through this barrier height at band offset and thus increases the depletion width, which reduces capacitance value.

Figure 3. Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) analysis of Ge and O₂ diffusion profile at GaN/AlGaIn layer after annealing at 825°C for W/Ge and W/O Ge samples. The dashed line in the upper curve is the SIMS background limit of Ge.

Figure 4. Band bending of AlGaIn/GaN heterostructure with presence of Ge layer. The electrons piled up at large conduction band offset region at Ge/GaN heterointerface.

The extrapolated pinch-off voltage, V_{th} is -3.5 V observed for W/Ge sample. Fig. 2a also shows the G-V characteristics of both samples appearing at depletion region. Depletion charges are interfacial 2DEG at AlGaIn/GaN and Ge/GaN cap interface. The electron confinement observed in W/Ge sample is due to Ge/GaN conduction band offset, which is prone to comprise of higher interfacial carrier concentration than W/O Ge sample and such higher density gives rise to a stronger G-V peak intensity at the depletion region. The high interface state density (D_{it}) is also responsible for frequency dispersion of CV-GV characteristics, hump in C-V and G-V peak but the frequency dispersion of G-V is more sensitive than C-V method. Both the samples reveal a very weak G-V dispersion behavior as shown in Figure 2c which demonstrates the presence of moderate level of D_{it} even though strong CV dispersion observed for W/Ge sample as seen in Figure 2b. The density of interface states (D_{it}) and the interface trap time constant (τ) extracted from the G_p/ω plot using G_p , ω , and τ relationship as expressed in equations 1 and 2.

$$\frac{G_p}{\omega} = \frac{q D_{it}}{2\omega\tau} \ln[1 + (\omega\tau)^2] \quad [1]$$

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{\max} \quad [2]$$

Several interfaces (e. g. Metal-GaN, AlGaIn-GaN) are present in Schottky diodes for both W/O Ge and W/Ge samples. The peak in the G_p/ω versus ω plot is caused by the presence of interface traps at these interfaces. The D_{it} value is achieved for W/O Ge sample is $\sim 2.7 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ which is similar to reported value by Freedman et al.¹¹ but a higher ($4.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) value is obtained for W/Ge sample, respectively. The extracted interface trap time constant (τ) obtain for both the samples about $\sim 3.5 \times 10^{-5} \text{ s}$. We believe that piled up electrons at the Ge/GaN interface are responsible for the hump and the related CV dispersion rather than D_{it} . Apart from Ge diffusion, O₂ diffusion in AlGaIn and surface roughness may also lead to the pinch-off voltage shift and high D_{it} . ToF-SIMS analysis of O₂ depth profile (Fig. 3) from W/Ge and W/O Ge sample shows negligible oxygen diffusion during annealing. Surface morphology has been studied using atomic force microscopy (AFM) after Ge deposition, annealing, and pre-gate cleaning. The AFM of the surface topography are shown in Figs. 5a and 5b. Our study shows that surface roughness increases after annealing significantly due to the agglomeration of Ge on top of GaN/AlGaIn. However, it reduces after pre-gate clean, which consists of acetone, IPA and HCl chemistries as evident in Fig. 5b. The slight lowering of surface roughness after pre-gate clean is probably due to the chemical etching of residual Ge. The surface morphology change observed for W/Ge sample probably responsible for a higher D_{it} . Also the presence of a lower bandgap Ge cap at top coupled with Ge diffusion at GaN/AlGaIn expected to lead higher gate leakage current. Figure 6 shows the gate to drain leakage characteristics for both W/Ge and W/O Ge samples. The reverse gate leakage is higher for

Figure 5. Surface morphology observed after Ge deposition (a), and pre-gate clean (b) on the sample surface by atomic force microscopy.

Figure 6. Gate to drain leakage characteristics for both W/Ge and W/O Ge samples.

Figure 7. I_{DS} - V_{GS} and transconductance (g_m) characteristics of HEMT devices with a drain voltage of 8 V.

W/Ge sample as expected as mentioned above. However, the forward current is comparable for both these samples.

The I_{DS} - V_{GS} and transconductance (g_m) characteristics of fabricated HEMT devices W/Ge and W/O Ge cap at gate area are shown in Fig. 7. The threshold voltages extracted from I_{DS} - V_{GS} curves using linear extrapolation method are very close to the pinch-off values obtained from the high frequency CV plot. I_{DS} and g_m values are lower for W/Ge compared to control sample due to the formation of dual channel as observed in CV curve. The electron mobility in Ge/AlGa interface expected to be much lower than AlGa/GaN 2DEG channel and therefore, reduces the drive current and g_m .

In summary, the effect of Ge diffusion on electrical properties of GaN/AlGa HEMT on SOI has been demonstrated. The gate to channel high-frequency CV characteristics show electron confinement at Ge/AlGa interface that causes n-type doping at AlGa after diffusion. The presence of residual Ge top cap layer and diffusion to GaN/AlGa creates threshold voltage shift toward enhancement mode type behavior. The reduction of drain current and transconductance for Ge-diffused sample is due to the reduction of 2DEG carrier concentration by Ge diffusion at AlGa layer.

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