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DC Marine Power System: Transient Behaviour and Fault Management Aspects

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Abstract—DC marine vessels with medium voltage compact dc power systems are dominated by a significant amount of active loads and a finite number of generation sources. In such scenarios, the network configuration of the dc power system is expected to get dynamically altered to fulfil the required generation and load demands for the desired marine mission. Such varying network configurations make the transient responses significantly different from the conventional ac grids and the prospective dc grids. In this regard, this paper performs systematic transient studies to devise fault management strategies for the dc marine vessels. Platform supply vessel (PSV) is taken as an example of the marine vessel, due to its complex operating scenarios and wider applicability in the marine industry. Pole-to-pole short-circuit faults are considered owing to its severity. A novel current-only directional protection for the dc PSV is proposed based on the directional zonal interlocking and short-time Fourier transform. The efficacy of the proposed method is substantiated by confirming against a range of fault impedances initiated at the generator terminals, load terminals, lines and buses of the dc PSV. All the analysis are conducted in the real-time simulation model of the dc PSV.

Index Terms—Directional Protection, Fault Studies, Marine Vessels, MVDC Power System, Platform Supply Vessel, Shipboard Power System, Short-Time Fourier Transform.

NOMENCLATURE

IED	Intelligent electronic device
S_D	Short-time Fourier Transform in discrete domain
S_C	Short-time Fourier Transform in continuous domain
f_u	Update frequency or zero-crossing frequency bin
$ S_D _{f_u}$	Magnitude of S_D at f_u
$ S_C _{f_u}$	Magnitude of S_C at f_u
RO_{IED_n}	Regenerative operation detected at n^{th} IED
RF_{IED_n}	Fault in reverse direction detected at n^{th} IED
NO_{IED_n}	Normal operation detected at n^{th} IED
FF_{IED_n}	Fault in forward direction detected at n^{th} IED

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I. INTRODUCTION

DC MARINE vessels are believed to be a feasible alternative to the conventional ac marine vessels owing to its significantly lower fuel consumption and emission. This fuel-efficient operation of dc marine vessel is achieved by operating the interfaced diesel generators (DGs) at optimized speed according to the load demand. Such operation has resulted in fuel savings up to 19% [1]. Moreover, lower system losses, easier integration of the emerging energy storage systems and relaxed synchronization requirements have increased the interest in the onboard dc marine vessels [2, 3]. In spite of such noteworthy advantages, the lack of systematic transient analysis and design of comprehensive short-circuit protection algorithms for the full-fledged dc marine vessels have been the major drawbacks for its widespread adoption.

Selection of the protection system is dependent on the class of marine vessel. In recent years, battery operated dc ferries have been commercially deployed, which operate covering short distances [4]. Loss of power in such vessels is expected to be tolerated as it would result in stalling of the vessel, and delay in operation with no major financial repercussions. As a result, low-complexity, low-cost fuse-based protection is contemplated to be suitable for such vessels. Conversely, continuity of power is of utmost importance for shipboard systems such as platform supply vessels (PSVs) undertaking complex marine missions such as dynamic positioning (DP) or supporting offshore supply vessels [5, 6]. For such applications, the delay in restoration of generation system due to ineffective protection algorithms resulting in inadvertent system blackout, might result in loss of position of the PSV [7]. Further, for the PSV involved in critical activities such as oil exploration etc., these events would lead to serious consequences causing a huge financial setback and environmental concerns such as spillage of oil. Thus, to harness the benefits of dc distribution with variable speed generation system in marine vessels, a robust and comprehensive protection system is needed so that uninterrupted power flow is ensured under all contingencies.

A. Background Information

Transient analysis for the full-fledged dc marine vessels such as dc PSVs is missing in the past literature. As compared with the land based dc microgrids, the dc PSV is compact with lower cable lengths and has higher penetration of active loads. In spite of these differences, the design of the protection system of the dc PSV is anticipated to be inspired from the system-level protection studies of the multi-terminal dc (MTDC) microgrids [8, 9]. Monadi *et al.* [10] proposed a

centralized differential protection scheme in which the entire MTDC microgrid is divided into several sub-microgrids. During the fault, the affected sub-microgrid is disconnected from the rest of the dc system which is later restored after the fault has been isolated. Although this scheme works satisfactorily for MTDC microgrids, this would not be suitable for dc PSVs undergoing DP operation where the power outage for the sub-microgrid section could not be tolerated. Fault detection based on the rate of change of current has been widely used for protective relaying in the MTDC microgrids [11],[12]. This method however is limited by stringent threshold settings for the selective fault discrimination. Differential protection has been utilized for the protection of MTDC microgrid at the mine site [13] and photo-voltaic powered dc microgrid [14]. Impedance estimation based protection of dc zonal marine vessel has been proposed, but it is limited by its longer operating time [15].

Most of the fault studies and protection systems are focused on bigger land-based power system models which have different fault characteristics than the compact dc PSV. The shorter line lengths in dc PSV results in severe low-impedance short-circuit fault currents of similar magnitude at almost all locations occurring at the same time instant. Such surge in the fault currents can damage the interfacing converters as well. In addition to the generation sources, the active propulsion loads of the dc PSV will also discharge to the fault point further aggravating the fault conditions. In such situations, dc PSV would require unit protection techniques where the faulty section is quickly identified and isolated. Differential based unit protection would demand accurate measurement and transmission of the time-stamped current/voltage signals requiring high-bandwidth communication infrastructure thus adding cost to the system [10, 13, 14]. Instead, a zone-based directional protection could be implemented which relies on a low-bandwidth communication infrastructure.

Directional protection has been a popular choice in the ac systems [16, 17]. On the other hand, there has been limited but increasing number of research investigation on the applicability of the directional protection to the dc networks [18]–[21]. The existing approaches have been studied on networks that rely majorly on the operation of the directional element ($\mathbb{D}$). Operating only with $\mathbb{D}$ might result in protection malfunctions in the dc PSVs comprised of multiple generation systems and active loads. In ac systems, directional protection is the combination of $\mathbb{D}$ (for fault localisation) and the time-domain based over-current (OC) relay to detect the faulty section. In the land-based ac systems, the amount of generation systems and loads are known before hand, thus the OC tripping set-points are optimized accordingly [22]. On the other hand, loading in a dc PSV is constantly changing and is dependent on the type of mission profiles. The DGs are expected to operate in optimized speed and some of them might be taken out of service depending on the load demand [7]. Thus, the application of the OC relay in directional protection with optimized protection settings might prove to be restrictive for such changeable system configurations in the dc PSVs.

B. Proposed Protection Algorithm

Instead of time-domain based OC detection, frequency domain based fault detection can be embedded in the directional protection for the application in dc PSVs. It detects the fault conditions by analyzing the presence of high frequency components and does not require optimized tripping set-points. With this regard, wavelet transform or short-time Fourier transform (STFT) could be implemented. Wavelet transform detects the presence of high frequency components in terms of detailed coefficients, which is dependent on the selection of the wavelet [23, 24]. STFT however, allows for the quantitative analysis of the high frequency components during the faults [18, 25]. As compared to wavelet transform, STFT is fast and easier to implement in the embedded platform [25]. For enhanced selective fault detection, the entire dc PSV is divided into several zones with the coordinated operation of the IEDs. $\mathbb{D}$ is computed in the IEDs of a specific zone and thus is termed as directional zonal interlocking (DZI).

This paper proposes a modified directional protection for dc PSVs that works by synergistic operation of the DZI and STFT. Both DZI and STFT are computed with the current signals thus making it low-cost and less complex. Such ‘current-only’ algorithms have been developed for the protection of generation and load systems, lines and buses. The generation and load systems are protected independently, whereas the protection of lines and buses is achieved by a low-bandwidth communication infrastructure.

The paper is divided into six sections. Section II briefly describes the real-time simulation model of the representative dc PSV. Section III covers the system level transient analysis and evaluation of the protection requirements. The need of DZI and STFT are also discussed in this section. Section IV covers the detailed modeling of the DZI and Section V covers the detailed analytical evaluation of the STFT based fault detection method. Section VI applies the proposed directional protection for the faults at the generators and loads terminals, lines and bus-bars. The protection method is validated by inspecting its operation against the fault currents of varying intensities at all locations. This is obtained by increasing fault resistances from low to high-impedance. The efficacy of the proposed method is supported by the comparative analysis with the existing methods and is covered in Section VII. The conclusions of this work are summarized in Section VIII.

II. MVDC PSV POWER SYSTEM CONFIGURATION

Fig. 1 depicts the real-time simulation model of the MVDC PSV intended for the short-circuit fault study and subsequent protection design. It comprises of four 2-MW variable speed DGs interfaced with the 1.5 kV dc bus using two-level voltage source converter (2L-VSC). MP is the 2.5-MW main propulsion drive responsible for cruising operation. TT and RT are 883-kW tunnel thruster and retractable thruster drive, respectively, to undertake DP operation. ESS is the energy storage system interfaced with the dc bus using a bi-directional dc/dc converter. The operation of dc PSV in the real-time simulation interface incorporating detailed modeling and control approaches have been adopted from [1]. Computation

Fig. 1. Representative dc PSV for dc fault studies [1].

of the real-time simulation system is carried out by state-space-nodal analysis in an RT-Lab platform based on Opal-RT. The components of the dc PSV are interfaced with the dc bus using intelligent electronic device (IED) and solid state circuit breaker (SSCB). The IED detects and SSCB isolates the respective section when fault ' F_j ' (for j -th segment of the line) happens. The dc PSV is divided into several zones ' Z_k ' (for k -th zone) based on their common functionalities. The fault analysis, description of the IEDs and the selection of zones are described in Section III.

III. TRANSIENT ANALYSIS AND PROTECTION REQUIREMENTS

A. Time-Domain Fault Analysis

The dc PSV is expected to be high-impedance grounded (at the mid-point of the dc-link capacitor) or ungrounded

to seamlessly operate for single earth fault thus improving the survivability [1]. Thus, the pole-to-pole short-circuit fault becomes the most severe kind of fault which might critically impact the operation of the dc PSV and has been considered in this paper. The analysis of the short-circuit fault is essential to investigate the nature of the fault transients. This is needed to understand the protection requirements and to find proper solutions. The plausible short-circuit faults F_1 , F_2 , F_3 and F_4 are initiated at the generator terminals, load terminals, lines and the busbar, respectively as shown in Fig. 1.

At low-impedance fault, the dc-link capacitor of the dc generation systems and the inverter-fed loads discharge immediately and forms the dominant part of the dc short-circuit current. This is followed by the fault current contribution from the ac side. The nature of the fault current can be underdamped (*u.d.*) or overdamped (*o.d.*) depending on the fault impedance and location of the fault etc. This has been explained using a transient dc circuit of a single dc generation system in Fig. ?? where the *u.d.* condition is achieved when $1/\sqrt{LC} > (2R + R_f)/4L$ and the *o.d.* condition is achieved when $(2R + R_f)/4L > 1/\sqrt{LC}$. The fault current for the *o.d.* and *u.d.* fault currents are shown below [25]:

$$i_{o.d.}(t) = \left[\frac{V(0+)}{2\mathcal{B}.L} + \frac{I(0+)}{2} \right] e^{-(\mathcal{A}-\mathcal{B})t} - \left[\frac{V(0+)}{2\mathcal{B}.L} - \frac{I(0+)}{2} \right] e^{-(\mathcal{A}+\mathcal{B})t} \quad (1)$$

$$i_{u.d.}(t) = e^{-\mathcal{A}.t} \left[\frac{V(0+)}{\omega_d.L} \cdot \sin \omega_d t + I(0+) \cos \omega_d t \right] \quad (2)$$

where, $\mathcal{A} = \frac{2R+R_f}{4L}$, $\mathcal{B} = \sqrt{\mathcal{A}^2 - \frac{1}{LC}}$ and $\omega_d = \sqrt{\frac{1}{LC} - \mathcal{A}^2}$. $V(0+)$ is the initial voltage of the dc-link capacitor (C) and $I(0+)$ is the initial current flowing through line inductance (L). The contribution of the capacitive discharge as per (1) and (2) to the dc fault current is shown in Fig. 2. It shows a good agreement between the simulation and analytical results confirming the dominance of capacitive discharge at low-impedance faults. However, at high-impedance faults, the generation system may see it as load change with no significant contribution from the dc-link capacitor which is explained in Section III-B.

B. Influence of Fault Resistance and Location

The study on the effect of the fault current due to varying fault resistance and location is imperative to formulate the fault detection algorithms while identifying their limitations. This study has not been widely addressed in the existing literature, as the study on the bolted short-circuit has predominantly been the prime focus. The faults of varying resistances are initiated at locations F_1 , F_2 , F_3 and F_4 , as shown in Fig. 1.

For the fault F_1 , the peak current and time to reach the peak current for various fault resistances observed by VSC-1 are shown in Fig. 3(a). The fault currents for low-impedance faults are dominated by the transient discharge of the dc-link capacitor, thus taking less time to reach the peak as shown in Fig. 3(a). As the fault resistance is increased, the magnitude of the capacitive discharge is lower than the fault current

Fig. 2. DC fault current and contribution of the capacitive discharge in dc fault current for (a) underdamped fault condition (0.01 Ω fault resistance) and (b) overdamped fault condition (0.1 Ω fault resistance). The highlighted area shows the time till which the capacitive discharge current is dominant in the dc fault current.

Fig. 3. (a) Peak fault current and time required to reach the peak current for fault F_1 , as seen from Conv-1. (b) Peak current and (c) time required to reach the peak current for various fault resistances for fault locations F_2 , F_3 and F_4 .

supplied from the ac side (G1) and thus it takes longer time to reach the peak fault current. Although the time required to reach the peak capacitor discharge is similar to that of low-impedance faults; it is the time to reach the peak fault current that increases. As seen from Fig 3(a), the transition from the low-impedance to high-impedance fault is observed by the increased time required to reach the peak fault current. Compared to low-impedance faults, there is a jump in peak fault current detection of magnitude of 10 for high-impedance fault currents.

The variations of the magnitude and time to reach the peak fault current as observed by VSC-1 for various fault resistances at different fault locations F_2 , F_3 and F_4 are depicted in Figs. 3(b) and 3(c), respectively. The magnitude of the peak fault current decreases as the fault location is further from the G1 generating source. As compared to the characteristic of fault F_1 in Fig. 3(a), the transition from low- to high-impedance fault is reached earlier at lower fault resistance values due to the impact of the line lengths. As expected, the faults at generator terminals are more detrimental as compared to the faults elsewhere in the system due to lower line lengths and higher fault current magnitudes.

C. Effect of the Loads and System Configuration

The loads of the dc PSV are comprised of the inverter-fed propulsion and hotel loads. Such loads have input dc-link capacitor that discharges during the low-impedance faults. The number of interconnected loads depends on the marine mission and system configuration. Different cases of marine missions such as DP, cruising and dock conditions are shown in Table I, which have different combinations of generators and loads. Fault F_3 of fault resistance 0.1Ω is initiated and the magnitude and time to reach the peak fault current flowing through IED5 and IED15 are listed in Table II.

The peak fault current for Case 4 (Table II) is higher than that of Case 1, as it depends on the number of connected generation and load systems. The time required to reach the peak fault current is dependent on the number of capacitors being discharged along with their rise time. The adverse impacts of the fault current can be reduced, provided the fault current contributions from the active loads are blocked, which is seen by a significant reduction in the peak fault current, as

TABLE I
SYSTEM CONFIGURATION FOR DIFFERENT MARINE MISSIONS

No.	Operating Mode & Load(kW)	Generator Combination	Load Combination
1	DP: 1500 kW	G1	RT,HL1,HL2
2	DP: 2500 kW	G1,G2	TT1,TT2,RT, HL1, HL3
3	Cruising: 5000 kW	G1,G2,G3	MP1,MP2,HL1,HL2
4	Cruising: 6000 kW	G1,G2,G3,G4	MP1, MP2,HL1,HL3
5	At Dock: 100 kW	G1	HL1, HL2
6	At Dock: 500 kW	G1	HL1, HL2, HL3

shown in Table II [19, 20]. To block the fault currents, the fault isolating devices for the load systems should have a different architecture as compared to the generation, lines and bus-bar ones. This is discussed in Subsection III-E.

It can be deduced from Table II that the fault current is dependent on the system configuration. The OC protection with adaptive tripping setpoints would be suitable for such scenarios. However, this approach is limited by the optimisation requirements of the tripping setpoints for each marine missions. It is thus necessary to implement a protection system with preferably fixed setpoint. Thus, STFT based frequency domain analysis is considered in this paper which detects the presence of high frequency components in the fault current. Such method is also independent of the system configuration which will be described in detail in Section IV.

TABLE II
FAULT CURRENT FLOWING THROUGH IED5 AND IED15 BEFORE AND AFTER THE ACTIVE LOADS ARE BLOCKED

Case	Mode	IED5		IED15	
		i_{peak} (kA)	t_{peak} (ms)	i_{peak} (kA) **	t_{peak} (ms)
1(a)	Before Blocking	35.57	0.59	-11.78	0.59
1(b)	After Blocking	17.56	3.00	-5.34	2.90
2(a)	Before Blocking	39.72	3.20	-27.74	3.40
2(b)	After Blocking	30.23	2.80	-9.78	2.80
3(a)	Before Blocking	62.79	3.00	-20.54	3.00
3(b)	After Blocking	40.60	2.70	-13.13	2.70
4(a)	Before Blocking	63.31	2.90	-24.97	0.59
4(b)	After Blocking	48.12	2.60	-16.04	2.60
5(a)	Before Blocking	33.90	0.59	-11.24	0.59
5(b)	After Blocking	17.45	3.00	-5.30	2.90
6(a)	Before Blocking	34.62	0.59	-23.59	0.49
6(b)	After Blocking	17.33	3.10	-8.15	0.09

** : Current direction through IED15 changes during fault.

Fig. 4. Diagram of directional selectivity in ac system [17].

D. Choosing the Selectivity for Protection Coordination

1) *Selectivity in ac systems:* In ac power systems, the protection set-points are determined using the steady-state fault currents. Traditionally, the IEDs are chronometrically coordinated, i.e., time-current based selectivity is employed. This is in accordance with the IEC 60255-3 [26] and is prevalent for longer inductive lines where the close-in and far-end faults have significantly different magnitudes. On the other hand, fixed current and time set-point based ‘definite mean time’ tripping of IEDs are implemented for smaller ac systems having shorter line lengths. Additionally, directional element has been popularly integrated for enhanced selective operation in such smaller systems comprised of multiple generation units and loads [17]. This combination of directional element working in conjunction with the OC scheme is popularly termed as directional protection. During the fault, directional relay determines the fault direction while the fixed set-point OC relay issues the trip command either in the forward or reverse direction. For illustration, the ac system with the direction of prefault current is depicted in Fig. 4. When the fault (F) is at busbar, the IED of CB3 detects forward fault and blocks the CB2 and CB5 in forward and reverse direction, respectively. Thus, the CB3 trips in the time set by its forward time delay. The directional selectivity prevents from false-tripping of the CBs but rather dictates the CBs to operate within its time settings defined by forward or reverse operation mode.

2) *Selectivity in dc systems:* As the transient discharge from the dc-link capacitor is dominant for the low-impedance faults in dc systems, such transient responses can be utilized for fault detection and protection settings of the IEDs. For the dc PSV with shorter line lengths and inductances, the time to reach the peak fault current is expected to be in the similar range for both close-in and far-end faults resulting in similar tripping times. Thus, it becomes difficult to coordinate the multiple IEDs considering such time constraints. This is illustrated by the operation of IED5 and IED15 in Fig. 5. IED5 should be able to discriminate between the faults F_2 and F_3 while the IED15 should be able to discriminate between the faults F_1 and F_3 . The time required to reach the peak fault current by IED5 and IED15 (Fig. 1) is shown in Figs. 5(a) and 5(b) respectively. It is noted that the IEDs must be able to discriminate the faults in the range of few milliseconds, which is almost in the same time range. Thus, a directional zonal interlocking (DZI) based selective operation is proposed for the dc PSV. Unlike in ac systems where the directional element triggers the forward

or backward operation of multiple IEDs, DZI in dc systems triggers the IEDs of a particular zone. The complete operation of the DZI is covered in Subsection IV-A. Further, instead of OC protection utilised in the ac systems, STFT is proposed for the dc PSV, which is discussed in Subsection V.

E. Fault Isolation Requirements and Architecture of IEDs

Fault isolation in the dc PSV is primarily challenged by the absence of current zero crossing. Hence, solid state circuit breakers (SSCBs) are conceived to be advantageous for such applications, which have additional advantages of lack of arcing process and well-defined pre-existing control techniques [27]. The relatively higher on-state resistance of SSCBs and the requirement of isolator for galvanic isolation are some of the issues that need to be mitigated. The on-state resistance could be reduced by connecting the SSCB blocks in optimized series-parallel combination [27]. An IGBT/IGCT based SSCB is considered in this paper as it has lower turn-off time $< 400 \mu s$ and higher current interrupting capability [27]. Apart from the fault isolation, a modified topology of SSCB should be used to block the load side dc-link capacitor discharge, as discussed in Subsection III-C. Hence, the load side SSCBs would have different structure as compared with those at the generator, line or busbar sides. Based on the decision of IED, the TRIP/BLOCK command is issued to the respective SSCBs. The structure of the IED and SSCB is shown in Fig. 6.

IV. PROTECTION ALGORITHM DESIGN

From the earlier discussions, it can be inferred that the time-domain based OC protection with directional element requires optimised tripping set-points, as the magnitude of the fault current changes with the system configuration and marine missions. Thus it is required to devise an algorithm which would depend on a fixed tripping set-point while being selective at the same time. With this regard, a DZI and STFT based protection of dc PSVs is proposed in this paper. The directional element in DZI should only determine the direction of the fault current while the tripping decision is initiated by the STFT based fault detection algorithm. The detailed operation of the DZI and STFT algorithm is discussed below.

A. DZI of DC PSV

DZI is the operation of the directional element ($\mathbb{D}$) within a defined zone ($f(\mathcal{Z})$). Selection of $f(\mathcal{Z})$ is ensured by the common functionalities marked in Fig. 1 and defined as:

$$f(\mathcal{Z}) = \begin{cases} \mathcal{Z}_{Gi}, i = 1 : 5 & : \text{generation systems} \\ \mathcal{Z}_{Lj}, j = 1 : 11 & : \text{loads} \\ \mathcal{Z}_{Bk}, k = 1 : 6 & : \text{buses} \\ \mathcal{Z}_{ACm}, m = 1 : 4 & : \text{ac systems} \\ \mathcal{Z}_{Cn}, n = 1 : 2 & : \text{lines / cables} \end{cases} \quad (3)$$

The directional element, $\mathbb{D}$, has not been widely explored for the protection of dc systems. In the existing methods, direction

Fig. 5. Fault impedance of 0.1Ω for F2 and F3. Time required by (a) IED5 and (b) IED15.

Fig. 6. Diagram of the IED along with the SSCBs for interfacing (a) loads and (b) generator, lines and bus-bar.

of the prefault current is fixed while the direction of the fault current is determined by (4) [18]–[21].

$$\mathbb{D} = \begin{cases} 1, & \text{if } i[n] \geq 0 \\ 0, & \text{if } i[n] < 0 \end{cases} \quad (4)$$

Modeling $\mathbb{D}$ as per (4) results in satisfactory operation for low-impedance faults. For high-impedance faults, the current might not reverse thus limiting the operation of $\mathbb{D}$. This is illustrated in Fig. 7(a) where the increasing fault resistance at F_1 does not reverse the current direction of IED1. To mitigate such limitations, $\mathbb{D}$ could alternatively be modeled as:

$$\mathbb{D} = \begin{cases} 1, & \text{if } i[n] - i[n-1] \geq +\delta \text{ (Forward Direction)} \\ 0, & \text{if } i[n] - i[n-1] \leq -\delta \text{ (Reverse Direction)} \\ X, & \text{if } i[n] - i[n-1] < |\delta| \text{ (No Change)} \end{cases} \quad (5)$$

This modified $\mathbb{D}$ compares the present ($i[n]$) and past current sample values ($i[n-1]$) to determine the direction of the fault current. Here, δ is a nonzero constant while $\mathbb{D}$ retains the previous operating value ($X = \{0, 1\}$) when the current difference lies between $\pm \delta$. Comparison of (5) is done with (4) to illustrate its effectiveness and is shown in Figs. 7(b) and Fig. 7(c). The conventional method, i.e. (4), is ineffective in the high-impedance fault region while the modified method (5) is dependent on the selection of δ . δ should be higher than the ripple content of the dc current otherwise $\mathbb{D}$ might give erroneous outputs. It is noted that $\mathbb{D}$ is merely an indication of the current flow direction that not only

changes during faults, but it might also change during load switching, regenerative actions, sudden generator/load outage and so on. Hence, $\mathbb{D}$ would be useful to determine the location of zone ($\mathcal{Z}$) when a change in current direction has occurred. The fault condition is confirmed by the STFT algorithm thus eventually issuing the TRIP command. On the contrary, in ac systems (Subsection III-D1), OC based fault detection is employed which would not be suitable for dc PSVs due to the limitations analyzed in Subsection III-C.

B. STFT Based Fault Detection

STFT is a frequency-domain analysis that helps in the quantitative analysis of the frequency components present in the input signal. This is determined by computing the discrete Fourier transform of the signal over a pre-defined window function. In the discrete domain, it is expressed as follows:

$$\mathcal{S}_{\mathcal{D}[m,k]} \{i[n]\} = \sum_{n=0}^{n=N-1} i[n]w[n-mH]e^{-j\frac{2\pi nk}{N}}, \quad (6)$$

where, $i[n]$ is the input signal, $w[n]$ is the window function, N is the number of FFT points, n is the time-domain index of $i[n]$, m is the position of $w[n]$ around which it is real and symmetric, H is the hop size between the successive windows and k is the frequency index. n is decided by the length of $w[n]$. Hanning window function is chosen in this paper as it is neither too sluggish nor is sensitive to smaller load changes [25]. The parameters used for computing $\mathcal{S}_{\mathcal{D}}$ are listed in Table III [25, 28]. Under prefault conditions, $\mathcal{S}_{\mathcal{D}}$ of dc current signal results in a sinc function which has very less magnitude at zero-crossing frequency bins (f_u). The locations of f_u for Hanning window function and for given parameters are shown in Table IV. During the faults in dc PSV, the rapid discharge from the dc-link capacitor is expected to be comprised of high frequency components. This ingress of the high frequency components in the fault current is expected to be identified by the magnitude at f_u , i.e. $|\mathcal{S}_{\mathcal{D}}|_{f_u}$. Thus along with DZI, this STFT algorithm will be embedded in the IED and will operate according to:

$$\mathcal{S}_{\mathcal{D} fault} = \begin{cases} 1, & \text{if } |\mathcal{S}_{\mathcal{D}}|_{f_u} \geq \sigma \text{ dB} \\ 0, & \text{otherwise} \end{cases} \quad (7)$$

Fig. 7. (a) Peak current through IED1 when fault F_1 resistance is varied from 0.001Ω to 100Ω . (b) Comparison of the proposed $\mathbb{D}$ (with various δ in (5)) against conventional $\mathbb{D}$ in (4). (c) Time required and $\mathbb{D}$ output for IED1 when $\delta=10$ A in (5) is employed.

TABLE III
PARAMETERS USED IN STFT ALGORITHM

Sampling Frequency (f_s)	H	N	Time Res. ($=H/f_s$)	Freq. Res. ($=f_s/N$)
10 kHz	2	32	0.1 ms	312.5 Hz

TABLE IV
UPDATE-FREQUENCY BINS FOR 32 SAMPLE HANNING WINDOW

Window Type	Win. Length [n]	Update Frequency Bins (f_u)		
		$2f_s/n$	$3f_s/n$	$4f_s/n$
Hanning Window	32	625 Hz	937.5 Hz	1250 Hz

Fig. 8. STFT operation to detect the high frequency components in the fault current.

where, σ is the fixed setpoint (in dB). The detailed operation of STFT, determination of STFT setpoint (σ) is described in detail in Section V.

V. EVALUATION OF STFT BASED ALGORITHM

A. Application of STFT to Constant DC Current

Fig. 8 depicts the operation of STFT based fault detection algorithm. $W1, W2, W3, \dots$ are the 32 sample Hanning window applied to the current signal under investigation. The DFT is then computed for each window (DFT_{W_n}) as per (6). This process is repeated by moving the window by H samples and again computing the DFT. The frequency resolution of the computed DFT is governed by f_s and N while the time resolution is governed by H . To understand the operation and characteristics of STFT algorithm during load change and fault

conditions, an analogous expression of (6) in the continuous domain will be evaluated which is expressed as:

$$\mathcal{S}_C\{i(t)\} = \int_0^\tau i(t)w(t-t_1)e^{-j\omega t}dt. \quad (8)$$

In the continuous domain, 32 sample window function is represented by window function of 3.2 ms length. And equivalently H in continuous domain is 0.2 ms. Under the prefault condition, a generalised representation the STFT of the constant dc current operating over time τ_1 to τ_2 is given as:

$$\begin{aligned} \mathcal{S}_C\{I_o\} &= \int_{\tau_1}^{\tau_2} I_o.w(t).e^{-j\omega t}dt \\ &= I_o(\tau_2 - \tau_1) \left(0.5e^{-j\omega(\tau_1+\tau_2)/2} \text{sinc} \frac{\omega}{2\pi}(\tau_2 - \tau_1) \right. \\ &\quad - 0.25e^{-j(\omega+\omega_\tau)(\tau_2+\tau_1)/2} \text{sinc} \frac{\omega + \omega_\tau}{2\pi}(\tau_2 - \tau_1) \\ &\quad \left. - 0.25e^{-j(\omega-\omega_\tau)(\tau_2+\tau_1)/2} \text{sinc} \frac{\omega - \omega_\tau}{2\pi}(\tau_2 - \tau_1) \right) \end{aligned} \quad (9)$$

where ω is the frequency when varied from $0 : f_s/2$, having resolution of f_s/N (Table III). The ω_τ in (9) is $2\pi/\tau$ where τ is the window length (3.2 ms).

B. Application of STFT to Step Change in DC Current

The STFT is applied to the step change in current as shown in Fig 9. The dc current changes from I_{in} to I_f which in

Fig. 9. Step change in dc current and moving window for STFT operation.

Fig. 10. STFT of the stepped current signal of Fig. 10; (a) before load step change. STFT of the stepped current signal after: (b) 0.2 ms (c) 0.8 ms (d) 1.2 ms, (e) 1.6 ms, (f) 2.0 ms, (g) 2.4 ms and (h) 3.2 ms of load change.

this case is 500 A and 600 A, respectively. The expression of current becomes important while applying STFT for the window at any time instant. For instance, in $W5$ the equivalent dc current can be represented by the following:

$$I_{dc} = A(\text{for } t_1 < t < t_1 + \tau) - B(\text{for } t_1 < t < t_2) + C(\text{for } t_2 < t < t_1 + \tau) \quad (10)$$

where, $A = [(t_2 - t_1)I_{in} + (t_1 + \tau - t_2)I_f]/\tau$, $B = [A - I_{in}]$ and $C = [I_f - A]$. The $\mathcal{S}_C$ of the step change in current is given by:

$$\mathcal{S}_C\{I_{dc}\}\Big|_{t_1}^{t_1+\tau} = \mathcal{S}_C\{A\}\Big|_{t_1}^{t_1+\tau} + \mathcal{S}_C\{B\}\Big|_{t_1}^{t_2} + \mathcal{S}_C\{C\}\Big|_{t_2}^{t_1+\tau} \quad (11)$$

The $\mathcal{S}_C\{A\}$, $\mathcal{S}_C\{B\}$ and $\mathcal{S}_C\{C\}$ are calculated as per (9). The comparison of the $\mathcal{S}_D\{I_{dc}\}$ and $\mathcal{S}_C\{I_{dc}\}$ is shown in Fig. 10. For the prefault condition, the magnitude at f_u (Table IV) is very less as discussed in Section IV-B. This is because the

$\mathcal{S}_C\{B\}$ and $\mathcal{S}_C\{C\}$ is zero. As a result the output of $\mathcal{S}_C\{I_{dc}\}$ is sinc function which is only dependent on τ . When the window is moved by H , the stepped up signal will also be encompassed by it. Thus, the output will be the sinc function depending on τ , $(t_2 - t_1)$ and $(t_1 + \tau - t_2)$ as per (11). This results in relatively higher magnitude at the defined f_u . This variation in the $\mathcal{S}_C\{I_{dc}\}$ and $\mathcal{S}_D\{I_{dc}\}$ for the window functions with various degree of overlapping between the I_{in} and I_f is shown in Fig. 10. The magnitude of $\mathcal{S}_C\{I_{dc}\}$ and $\mathcal{S}_D\{I_{dc}\}$ at f_u is highest when the window encompasses 50% of I_{in} and 50% of I_f (Fig. 10(e)). The $\mathcal{S}_C\{I_{dc}\}$ and $\mathcal{S}_D\{I_{dc}\}$ comes to normal condition when the window encompasses the I_f completely as shown in Fig. 10(h). It is further observed that the higher order f_u are distorted even for smaller overlapping between I_f and I_{in} where as the first order f_u i.e. 625 Hz is relatively robust and distorts for maximum overlapping condition. As a result, $f_u = 625$ Hz is taken in this paper for the setpoint to detect the transient conditions.

C. Determining Threshold for STFT based Fault Detection

It has been described in (7) that the STFT algorithm is dependent on σ for effective fault identification. The variation of this σ is described in Fig. 10 when step change of dc current is initiated. Since, the STFT quantifies the frequency components present in the input signal; the magnitude at f_u i.e. σ is expected to be modified by the ripple content of the dc current under investigation. As a result, the STFT of the dc current would not resemble to the sinc function as described in Section V-B and Fig. 10(a), 10(h). Since ripples are present in the current of dc PSV, the current can be represented by:

$$I_{dc} = I_o + \sum_{n=2,3,4,\dots} I_n \sin \omega_n t. \quad (12)$$

The I_{dc} comprises of the dc component, I_o and very small contributions from the ripples $I_n \sin \omega_n t$. In such case, the STFT computation will be modified to:

$$\mathcal{S}_C\{I_{dc}\} = \int_0^\tau \left(I_o + \sum_{n=2,3,4,\dots} I_n \sin \omega_n t \right) w(t) e^{-j\omega t} dt \quad (13)$$

$\mathcal{S}_C$ of I_o will take form of (9) and to get the essence of the ripple components, the $\mathcal{S}_C$ of the ripples can be expressed as:

$$\begin{aligned}\mathcal{S}_C\{I_n\} &= \int_0^\tau \sum_{n=2,3,4\dots} I_n \sin \omega_n t w(t) e^{-j\omega t} dt \\ &= \sum_{n=2,3,4\dots} \left[\left\{ \frac{I_n \tau}{2j} \left[(e^{-j(\omega-\omega_n)\tau/2} \text{sinc} \frac{\omega-\omega_n}{2\pi} \tau) \right. \right. \right. \\ &\quad \left. \left. - 0.5 \left(e^{-j(\omega-\omega_n-\omega_\tau)\tau/2} \text{sinc} \frac{\omega-\omega_n-\omega_\tau}{2\pi} \tau \right) \right. \right. \\ &\quad \left. \left. - 0.5 \left(e^{-j(\omega-\omega_n+\omega_\tau)\tau/2} \text{sinc} \frac{\omega-\omega_n+\omega_\tau}{2\pi} \tau \right) \right] \right\} \\ &\quad \left. - \left\{ \frac{I_n \tau}{2i} \left[(e^{-j(\omega+\omega_n)\tau/2} \text{sinc} \frac{\omega+\omega_n}{2\pi} \tau) \right. \right. \right. \\ &\quad \left. \left. - 0.5 \left(e^{-j(\omega+\omega_n-\omega_\tau)\tau/2} \text{sinc} \frac{\omega+\omega_n-\omega_\tau}{2\pi} \tau \right) \right. \right. \\ &\quad \left. \left. - 0.5 \left(e^{-j(\omega+\omega_n+\omega_\tau)\tau/2} \text{sinc} \frac{\omega+\omega_n+\omega_\tau}{2\pi} \tau \right) \right] \right\} \right] \quad (14)\end{aligned}$$

The magnitude of the $\mathcal{S}_{C_{I_n}}$ is given as following:

$$|\mathcal{S}_{C_{I_{dc}}}|_{\omega=0:f_s/2} = 20 \log_{10} \left| \frac{\mathcal{S}_C\{I_o\} + \mathcal{S}_C\{I_n\}}{0.5 \tau} \right| \text{ dB} \quad (15)$$

To illustrate the effect of the ripples, $n = 6$ and $n = 30$ is considered as per (14) and is shown in Fig. 11(a) and Fig. 11(b) respectively. To understand the effect of ripples, the magnitude of I_6 and I_{30} has been set to 1. It is seen from Fig. 11(a) that the lower order harmonic (360 Hz) severely influences the magnitude at $f_u = 625$ Hz. The magnitude at 360 Hz increases to -4.27 dB while it is expected to be very less. For the higher order harmonics in Fig. 11(b), the magnitude is higher in the vicinity of the corresponding higher order frequencies. As a result, the magnitude at $f_u = 625$ Hz is quite low. This is further illustrated in Fig. 11(c) which depicts the impact of 2^{nd} , 6^{th} and 12^{th} harmonic on the STFT magnitude of I_{dc} at 625 Hz when I_n/I_o is varied in (13). There is increasing trend in the magnitude at 625 Hz when I_n/I_o is increased. The I_o is the base current which depends on the power level of the system. In this paper I_o is taken to be 1300 A thus additional $20 \log_{10} I_o$ would be added to the magnitude at desired ripple content (Fig. 11(c)). Following this procedure, σ for tripping has been chosen to be 20 dB.

D. Application of STFT to Fault Condition

As per (1) and (2), the fault current signals comprises of exponential component for overdamped conditions and sinusoidal component for the underdamped conditions respectively.

TABLE V
MAGNITUDE AT UPDATE FREQUENCY BINS OF 625 HZ FOR THE STFT OF i_{IED5} AND i_{IED15} AND TIME TO REACH

Case	Mode	IED5		IED15	
		$ S_D _{f_u}$ (dB)	$t_{ S_D _{f_u}}$ (ms)	$ S_D _{f_u}$ (dB)	$t_{ S_D _{f_u}}$ (ms)
1	Before Blocking	22.2567	0.2	37.866	0.4
	After Blocking	22.2567	0.2	32.6968	0.4
2	Before Blocking	45.6311	0.4	21.2959	0.2
	After Blocking	22.5083	0.2	39.6161	0.4
3	Before Blocking	24.7209	0.2	40.2659	0.4
	After Blocking	24.6852	0.2	36.293	0.4
4	Before Blocking	24.2759	0.2	44.8228	0.4
	After Blocking	24.2759	0.2	40.4097	0.4
5	Before Blocking	21.9615	0.2	37.5648	0.4
	After Blocking	21.9615	0.2	32.3493	0.4
6	Before Blocking	23.234	0.2	44.804	0.4
	After Blocking	23.234	0.2	39.0298	0.4

$\sigma = 20$ dB, $f_u = 625$ Hz

The STFT of the overdamped fault takes the form of :

$$\begin{aligned}\mathcal{S}_C\{I_{od}\} &= \int_0^\tau i_{od} w(t) e^{-j\omega t} dt \\ &= \mathcal{X} \left[\frac{1 - e^{-(A-B+j\omega)\tau}}{A-B+j\omega} - 0.5 \frac{1 - e^{-(A-B+j(\omega-\omega_\tau))\tau}}{A-B+j(\omega-\omega_\tau)} \right. \\ &\quad \left. - 0.5 \frac{1 - e^{-(A-B+j(\omega+\omega_\tau))\tau}}{A-B+j(\omega+\omega_\tau)} \right] - \mathcal{Y} \left[\frac{1 - e^{-(A-B+j\omega)\tau}}{A-B+j\omega} \right. \\ &\quad \left. - 0.5 \frac{1 - e^{-(A-B+j(\omega-\omega_\tau))\tau}}{A-B+j(\omega-\omega_\tau)} - 0.5 \frac{1 - e^{-(A-B+j(\omega+\omega_\tau))\tau}}{A-B+j(\omega+\omega_\tau)} \right] \quad (16)\end{aligned}$$

where $\mathcal{X} = \left[\frac{V(0+)}{2B.L} + \frac{I(0+)}{2} \right]$ and $\mathcal{Y} = \left[\frac{V(0+)}{2B.L} - \frac{I(0+)}{2} \right]$. $\mathcal{A}$ and $\mathcal{B}$ are according to (1). The STFT of the underdamped fault current signal takes the form of (14). The STFT analysis of the fault currents would follow the similar procedure as described in Section V-B. In both cases, the magnitude at the $f_u = 625$ Hz is altered as by $(\omega + \omega_\tau)$ and $(\omega - \omega_\tau)$ for overdamped signal and $(\omega + \omega_d + \omega_\tau)$, $(\omega + \omega_d - \omega_\tau)$, $(\omega - \omega_d + \omega_\tau)$, and $(\omega - \omega_d - \omega_\tau)$ for underdamped fault current signal. The variation of STFT magnitude of dc fault current at 625 Hz for 0.1 Ω fault resistance is shown in Fig. 12. It can be observed that the STFT magnitude at 625 Hz is very less for prefault dc current. As the Hanning window encompasses the fault current, the STFT magnitude at 625 Hz rises as shown in Fig. 12. STFT is applied for the fault currents with different system configurations, as listed in Table II, where the OC protection would be challenging to implement. In spite of the changing system configuration and blocking/unblocking of the loads, the STFT is able to detect the fault condition as per the threshold described in Section V-C and is illustrated in Table V.

VI. CASE STUDIES

The direction of prefault current in the dc PSV is predetermined as indicated by thick arrows in Fig. 1. The STFT is combined with $\mathbb{D}$ to devise the protection logic of the dc PSV. The logical output of the STFT, i.e. $\mathcal{S}_D$ (based on (6) and (7)) and $\mathbb{D}$ (based on (5)), are calculated in the IEDs. Based on such outputs, the various possible outcomes of the IEDs are listed in Table VI. This information has been used for devising protection logic for faults at various locations which is discussed below.

Fig. 11. STFT of (a) 360 Hz, (b) 1800 Hz signal. (c) Normalised magnitude of SC_{Idc} at 625 Hz for various I_n/I_o .

Fig. 12. Variation of the STFT magnitude at $f_u = 625$ Hz as the Hanning window progressively captures the fault current signal.

TABLE VI
TRUTH TABLE OF IED DEPICTING VARIOUS POSSIBILITIES

$\mathbb{D}$	$\mathcal{S}_{D,fault}$	State	Notation
0	0	Regenerative Operation	RO
0	1	Faults at Reverse Direction	RF
1	0	Normal Operation	NO
1	1	Faults in Forward Direction	FF

A. Protection of Generators and Loads

1) *Faults at generator terminal (F_1):* The faults at generator zone $\mathcal{Z}_G$ is identified by RF , i.e. the reversal of current through the respective IED with the presence of high frequency components in it. For illustration, fault F_1 at Gen-1 terminal (Fig. 1) is detected by RF_{IED1} , which is given by:

$$RF_{IED_{Gen}} \implies \mathbb{D} = 0 \ \&\& \ |\mathcal{S}_{\mathcal{D}}|_{f_u} > \sigma_{gen} \text{ dB}. \quad (17)$$

The relay diagram for generator IED incorporating (17) with notations consistent with Table VI is shown in Fig. 13. Operation of the IED1 for fault F_1 with increasing fault resistances is shown in Table VII. For low-impedance faults, IED1 is able to detect the fault condition and initiate TRIP command. However, for extremely high-impedance faults, STFT is high but since $\mathbb{D}$ is not able to detect the change in current direction, IED is set to ALARM output.

2) *Fault at load terminal (F_2):* The faults at load zone $\mathcal{Z}_L$ is identified by FF through the respective load IEDs. Such

Fig. 13. Logic diagram for generator protection.

TABLE VII
DECISION TIME OF IED1 AS PER FIG. 13 FOR DIFFERENT VALUES OF FAULT RESISTANCE F_1

Fault Resistance (Ω)	$\mathbb{D}$	t_D (ms)	$ \mathcal{S}_{\mathcal{D}} _{f_u}$ (dB)	$t_{ \mathcal{S}_{\mathcal{D}} _{f_u}}$ (ms)	Trip/Alarm	Decision Time (ms)
0.001	0	0.2	27.41	0.4	TRIP	0.4
0.002	0	0.2	35.73	0.4	TRIP	0.4
0.005	0	0.2	30.54	0.4	TRIP	0.4
0.01	0	0.2	32.33	0.4	TRIP	0.4
0.02	0	0.2	21.27	0.2	TRIP	0.2
0.05	0	0.2	28.33	0.4	TRIP	0.4
0.1	0	0.2	25.01	0.4	TRIP	0.4
0.2	0	0.2	28.73	0.4	TRIP	0.4
0.5	0	0.2	23.54	0.4	TRIP	0.4
1	0	0.2	21.58	0.4	TRIP	0.4
2	0	0.2	23.32	0.6	TRIP	0.6
5	0	0.2	22.29	0.8	TRIP	0.8
10	0	0.2	17.44	0.8	TRIP	0.8
20	1	ND*	16.32	0.8	ALARM	0.8
50	1	ND*	15.60	43	ALARM	43
100	1	ND*	15.88	543	ALARM	543

ND*: No Detection, $\sigma_{gen} = 20$ dB, $f_u = 625$ Hz.

cases are identified by:

$$FF_{IED_{Load}} \implies \mathbb{D} = 1 \ \&\& \ |\mathcal{S}_{\mathcal{D}}|_{f_u} > \sigma_{load} \text{ dB}. \quad (18)$$

where the current direction is similar to that of the prefault current along with the presence of high frequency components. The faults outside $\mathcal{Z}_L$ is characterized by RF as:

$$RF_{IED_{Load}} \implies \mathbb{D} = 0 \ \&\& \ |\mathcal{S}_{\mathcal{D}}|_{f_u} > \sigma_{load} \text{ dB}. \quad (19)$$

In such conditions, the IEDs might block the SSCBs as discussed in Section III-C.

The relay diagram for load IED is shown in Fig. 14 and the operation of IED17 for fault F_2 with increasing fault resistances is shown in Table VIII. As the current direction remains the same, the protection algorithm is dependent on

Fig. 14. Logic diagram for load protection.

TABLE VIII
DECISION TIME OF IED17 AS PER FIG. 14 FOR DIFFERENT VALUES OF FAULT RESISTANCE F_2

Fault Resistance (Ω)	$ S_D _{f_u}$ (dB)	$t_{ S_D _{f_u}}$ (ms)	Trip/Alarm	Decision Time (ms)
0.001	20.05	0.4	TRIP	0.4
0.002	28.84	0.4	TRIP	0.4
0.005	29.87	0.4	TRIP	0.4
0.01	26.35	0.4	TRIP	0.4
0.02	28.9	0.4	TRIP	0.4
0.05	20.2	0.4	TRIP	0.4
0.1	24.58	0.4	TRIP	0.4
0.2	27.51	0.4	TRIP	0.4
0.5	29.9	0.4	TRIP	0.4
1	21.17	0.4	TRIP	0.4
2	26.86	0.6	TRIP	0.6
5	24.19	0.8	TRIP	0.8
10	21.17	0.8	TRIP	0.8
20	22.02	1.4	TRIP	1.4
50	21.01	1.4	TRIP	1.4
100	21.71	43	ALARM	43

$\sigma_{load} = 20$ dB; $f_u = 625$ Hz.

the STFT output for fault detection. In such cases, the IED is unable to detect the extremely high-impedance faults.

B. Protection of Lines and Buses

Compared to the generator and load systems; protection of the lines and buses would require operation of multiple IEDs. For instance, fault F_3 in Fig. 1 would be detected and isolated by the operation of IED5 and IED15, while the fault F_2 will be decided by the outcome of IED1, IED3, IED11, IED5, IED7 and IED9. Hence, there is a need of communication interface among the IEDs for fault detection in the lines and buses. Centralised protection could be implemented, which is expected to be adopted from the IEC 61850 based ac systems [29]. Due to stringent time requirements in dc systems (Subsection III-B), direct adoption of the communication infrastructure from the ac system would not be suitable for such applications. Hence, high speed optical fibre based communication could be selected for faster exchange of data. Further, adopting low-bandwidth communication would limit the hardware requirements [30]. Thus, instead of the time-stamped current samples, the IED decisions (i.e. the binary outputs) could be exchanged to compute the decision. With these considerations, the architecture of the IEDs communicating with the central computer could be selected similar to the 5th generation architecture for the centralized protection of the ac substation in [29], which has high reliability and thus making it suitable for the protection of dc PSV.

1) *Faults at Lines (F_3):* For the low-impedance fault at F_3 (Fig. 1), TRIP command is issued by the central computer

Fig. 15. Logic diagram of for protection of fault F_3 in line of Zone-3.

when FF_{IED5} and RF_{IED15} are activated. For very high-impedance faults, the current through IED15 might not reverse thus it might indicate *NO* instead of *RF*. This condition can be accommodated by the ALARM output. These conditions are shown in the relay diagram in Fig. 15. Table IX shows the outcome of IED5 and IED15 for increasing fault resistances. It is seen that the proposed method is able to fairly identify faults and initiate TRIP command. For very high-impedance faults, the method gives ALARM output.

2) *Fault at Bus-Bar (F_4):* As per Fig. 1, the bus-bar fault F_4 would result in tripping of all the SSCBs associated with IED1, IED3, IED7, IED9, IED5 and IED11. The outputs of all the IEDs would be sent to the central computer for computation before the TRIP signals are initiated. The low-impedance fault at F_4 would be characterised by FF_{IED1} , FF_{IED3} , RF_{IED7} , RF_{IED9} , RF_{IED5} and RF_{IED11} . Current direction and STFT of IED11 is of prime importance for protection of IED11. Similar to Subsection VI-B1, ALARM is initiated for fault F_4 when IED11 is able to detect the fault while the rest of the IEDs cannot. The detailed operation of the various associated IEDs for fault F_4 is listed in Table X.

C. Dependence on Loading Transients

The proposed protection algorithm should be immune to the sudden load transients in the dc PSV. As per Fig. 1, sudden change in the propulsion load and operating the pulsed load at regular intervals are taken into consideration which is shown in Fig. 16(a). Correspondingly in Fig. 16(b) the magnitude at $f_u = 625$ Hz is illustrated for the load transients in Fig. 16(a). Due to higher inductance of the propulsion system, the rate of

TABLE IX
DECISION TIME OF IED5 AND IED15 AS PER FIG. 15 FOR DIFFERENT VALUES OF FAULT RESISTANCE F_3

Fault Resistance (Ω)	IED5		IED15		Trip/Alarm	Decision Time (ms)
	$t_{ S_D _{f_u}}$ (ms)	t_D (ms)	$t_{ S_D _{f_u}}$ (ms)	t_D (ms)		
0.001	0.2	0.1	0.2	0.1	TRIP	0.2
0.002	0.4	0.1	0.4	0.1	TRIP	0.4
0.005	0.2	0.1	0.2	0.1	TRIP	0.2
0.01	0.2	0.2	0.2	0.2	TRIP	0.2
0.02	0.2	0.2	0.2	0.2	TRIP	0.2
0.05	0.2	0.1	0.2	0.1	TRIP	0.2
0.1	0.2	0.1	0.2	0.1	TRIP	0.2
0.2	0.4	0.1	0.2	0.1	TRIP	0.4
0.5	0.4	0.2	0.4	0.2	TRIP	0.4
1	0.6	0.1	0.4	0.1	TRIP	0.6
2	0.6	0.2	0.6	0.2	TRIP	0.6
5	0.8	0.2	0.8	0.2	TRIP	0.8
10	1	0.1	0.8	0.1	TRIP	1.0
20	1.4	ND	1	ND	ALARM	1.4
50	393	ND	393	ND	ALARM	393
100	413	ND	413	ND	ALARM	413

ND: No Detection, $\sigma_{line} = 20$ dB; $f_u = 625$ Hz.

TABLE X
STATUS OF THE IEDS IN ZONE $\mathcal{Z}_{B1}$ FOR FAULT F_4

Fault Resistance (Ω)	IED1	IED3	IED7		IED9		IED5		IED11		Trip/Alarm	Decision Time (ms)
	$t_{SD f_u}(ms)$	$t_{SD f_u}(ms)$	$t_D(ms)$	$t_{SD f_u}(ms)$	$t_D(ms)$	$t_{SD f_u}(ms)$	$t_D(ms)$	$t_{SD f_u}(ms)$	$t_D(ms)$	$t_{SD f_u}(ms)$		
0.001	0.4	0.4	0.1	0.4	0.2	0.4	0.1	0.2	0.1	0.2	TRIP	0.4
0.002	0.4	0.4	0.2	0.4	0.2	0.4	0.2	0.2	0.2	0.2	TRIP	0.4
0.005	0.4	0.4	0.2	0.4	0.2	0.4	0.2	0.2	0.2	0.2	TRIP	0.4
0.01	0.4	0.4	0.2	0.4	0.2	0.4	0.1	0.4	0.1	0.2	TRIP	0.4
0.02	0.4	0.4	0.2	0.6	0.2	0.6	0.1	0.2	0.1	0.2	TRIP	0.6
0.05	0.4	0.4	0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	TRIP	0.4
0.1	0.6	0.6	0.2	0.4	0.2	0.4	0.1	0.2	0.1	0.2	TRIP	0.6
0.2	0.6	0.6	0.2	0.6	0.2	0.6	0.1	0.4	0.1	0.4	TRIP	0.6
0.5	0.8	0.8	0.2	0.6	0.2	0.8	0.1	0.6	0.1	0.4	TRIP	0.8
1	0.8	0.8	ND	1	ND	1	0.2	0.4	0.2	0.4	TRIP	1
2	1.2	1.2	ND	ND	ND	1.2	0.2	0.6	0.2	0.4	TRIP	1.2
5	ND	ND	ND	ND	ND	ND	ND	1	0.2	0.6	ALARM	1
10	ND	ND	ND	ND	ND	ND	ND	0.8	ND	1	ALARM	1
20	ND	ND	ND	ND	ND	ND	ND	31	ND	1	ALARM	31
50	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	-	-
100	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	-	-

ND: No Detection; $\sigma_{gen}, \sigma_{load}, \sigma_{line} = 20$ dB; $f_u = 625$ Hz.

Fig. 16. (a) Time-domain characteristics of propulsion and pulsed load. (b) STFT magnitude at $f_u = 625$ Hz for propulsion and pulsed load.

rise of current is slower which as a result does not significantly alter the magnitude at 625 Hz. On the contrary the pulsed load resembles a sequential step change operation as described in Section V-B which results in increased magnitude at 625 Hz for every transition of dc current which is shown in Fig. 16(b). While designing the protection logic for such pulsed loads, the δ would be set above the normal switching range so as to satisfy (18) and provide selectivity between the loading transients and fault conditions.

D. Generalised Flowchart for Proposed dc Protection

The consolidated flow chart of the proposed dc protection algorithm for dc PSV is depicted in Fig. 17. The flowchart is for generalized application and can be configured for the IEDs of any location.

VII. COMPARISON WITH EXISTING DIRECTIONAL PROTECTION APPROACHES

The existing approaches in directional protection is dependent mostly on the communication among the IEDs. As the short-circuit fault is characterized by rapid increase in current and undervoltage in the system, the IEDs exchange signals when the voltage falls below undervoltage threshold (V_{Thresh}). In these approaches $\mathbb{D}$ is modeled as per (4) which are then compared for all the IEDs. The fault location is confirmed when there is contrasting occurrence of $\mathbb{D}$ between the IEDs.

Tripping command to the respective SSCB is executed when the current threshold (I_{Thresh}) is exceeded. This can further be divided into Method 1 and Method 2 depending on the I_{Thresh} values. Method 1 uses overcurrent as tripping criteria [20, 21], for which I_{Thresh} value in this paper has been set at 2 pu. Method 2 is independent of the magnitude of I_{Thresh} and is only dependent on the $\mathbb{D}$ and V_{Thresh} [18, 19]. The comparison of the Method-1 and Method-2 with the proposed directional

Fig. 17. Generalised flowchart of the proposed protection of generator, load, line and bus-bar of dc PSV.

Fig. 18. Current of IED5 for 0.02 Ω and 0.05 Ω fault at F_3 . Fault detection time by the existing and proposed dc protection methods are also highlighted.

protection is shown in Table XI.

The operation of existing methods is dependent on the system configuration, fault level, I_{Thresh} and V_{Thresh} . Setting suitable I_{Thresh} is difficult for dc PSV application which has been described in Section III-C. Moreover, the undervoltage limit, V_{Thresh} can be achieved with ease for the low-impedance faults. As the fault impedance rises, the I_{Thresh} and V_{Thresh} (for Method-1) are difficult to satisfy thus limiting its operation which can be seen in Table XI where Method-1 cannot work after 0.1 Ω fault impedance. Method-2 is able to detect the fault till I and V_{Thresh} criteria are satisfied. It seems to work better than Method-1 but has limitations which has been described earlier in Fig. 7(b) and cannot work 0.2 Ω onwards. The advantage of the proposed dc protection method is further illustrated in Fig 18 where both protection algorithms are compared at IED5 for fault F_3 with fault impedances 0.02 Ω and 0.05 Ω . From the current measured at IED5 (Fig. 18), it can be seen that the proposed protection is much faster than the existing approaches. Thus the required energy to be dissipated by the fault isolation devices would be much less.

VIII. CONCLUSION

This paper has presented DZI and STFT based directional protection for the application in dc marine vessels. The results are promising as the proposed method is able to selectively identify the faults. The proposed technique could also be applied to other compact dc power systems such as more-electric aircraft and the compact land-based dc microgrids.

- 1) Short-circuit transient analysis with increasing fault resistances are carried out at the generator terminals and load, lines and bus-bar. The variation of peak fault current and time to reach the peak fault currents have been studied. It is seen that the coordination between the IEDs becomes the major problem as the time difference is in the range of few milliseconds.
- 2) DZI based directional element has been proposed in this paper which is modeled by dividing the dc PSV into several zones. Its efficacy is supported by the comparative studies with the existing directional elements.
- 3) The fault condition is confirmed by STFT which is also able to detect the fault currents of very high fault impedances. Fault condition is confirmed when both DZI and STFT are activated.

- 4) A method has been introduced to analyse the high-frequency components during step change in the dc current. This step change might also resemble high-impedance faults or sudden switching of the high-bandwidth constant power loads.
- 5) Protection of generators and loads are done independently while the protection of lines and buses would require low-bandwidth communication.
- 6) The IEDs (along with SSCBs) and the communication requirements to realise this protection systems have also been discussed.
- 7) The proposed directional protection works better than the existing methods owing to effective operation of DZI and STFT algorithm. Moreover, with the proposed method, time to detect the fault is within 1 ms which is much lower than the existing methods. This is due to fact that the proposed method is dependent on less number of parameters and communication requirements as compared to the existing methods.

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TABLE XI
TIME TAKEN (ms) TO DETECT FAULT USING CONVENTIONAL AND PROPOSED FAULT DETECTION METHODS

Fault Resistance	Fault F1			Fault F2			Fault F3			Fault F4		
	Method-1	Method-2	Proposed Method	Method-1	Method-2	Proposed Method	Method-1	Method-2	Proposed Method	Method-1	Method-2	Proposed Method
0.001 Ω	13.2	1.7	0.4	17.6	4.3	0.4	12.0	12.0	0.2	12.2	12.1	0.4
0.002 Ω	13.1	1.8	0.4	16.6	6.7	0.4	21.1	21.1	0.4	12.2	12.1	0.4
0.005 Ω	13.4	2.2	0.4	21.2	10.3	0.4	12.2	12.2	0.2	13.5	13.4	0.4
0.01 Ω	13.2	3.3	0.4	23.4	10.4	0.4	13.4	13.3	0.2	13.0	12.9	0.4
0.02 Ω	14.9	4.0	0.2	24.0	10.3	0.4	12.3	12.2	0.2	12.8	12.8	0.6
0.05 Ω	13.2	7.0	0.4	24.2	10.4	0.4	14.0	13.9	0.2	ND	13.5	0.4
0.1 Ω	ND	16.3	0.4	ND	10.3	0.4	ND	13.9	0.2	ND	12.9	0.6
0.2 Ω	ND	ND	0.4	ND	ND	0.4	ND	ND	0.4	ND	ND	0.6
0.5 Ω	ND	ND	0.4	ND	ND	0.4	ND	ND	0.4	ND	ND	0.8
1 Ω	ND	ND	0.4	ND	ND	0.4	ND	ND	0.6	ND	ND	1.0
2 Ω	ND	ND	0.6	ND	ND	0.6	ND	ND	0.6	ND	ND	1.2
5 Ω	ND	ND	0.8	ND	ND	0.8	ND	ND	0.8	ND	ND	1.0
10 Ω	ND	ND	0.8	ND	ND	0.8	ND	ND	1.0	ND	ND	1.0
20 Ω	ND	ND	0.8	ND	ND	1.4	ND	ND	1.4	ND	ND	31
50 Ω	ND	ND	43	ND	ND	1.4	ND	ND	393	ND	ND	ND
100 Ω	ND	ND	543	ND	ND	43	ND	ND	413	ND	ND	ND

ND- No Detection, $V_{thresh} = 0.8$ pu; I_{thresh} (Method-1) = 2 pu.

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