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Triggering voltage for post-breakdown random telegraph noise in HfLaO dielectric metal gate metal-oxide-semiconductor field effect transistors and its reliability implications

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We report a triggering voltage V_{trig} for observing gate leakage current (I_g) random telegraph noise (RTN) in the post-breakdown regime of HfLaO dielectric metal gate stacks. V_{trig} , the onset voltage to observe RTN in degraded dielectrics, is highly dependent on breakdown hardness, which is controlled by the leakage current compliance (I_{gl}). This dependence is qualitatively analyzed using a percolation dilation model, where generation of additional traps either at different energy levels or spatial locations gives lower V_{trig} at higher I_{gl} . The magnitude of V_{trig} can be used as a direct indication of the impact of RTN on the performance of the transistor at device level, when V_{trig} is evaluated by comparing with the device operating voltage. © 2012 American Institute of Physics. [doi:10.1063/1.3676255]

Gate dielectrics in nanoscale transistors are scaled aggressively for performance enhancement, which leads to a significant amount of gate leakage I_g through the gate stack. I_g low-frequency noise (LFN) measurement is a popular tool to characterize traps in gate dielectrics;^{1–4} the components analyzed include 1/f noise, random telegraph noise (RTN) and white noise. In the post-breakdown (post-BD) study of MOSFET gate dielectrics, I_g RTN is directly correlated to the stress-induced traps/defects generated in the dielectrics. Moreover, the RTN fluctuation is believed to be a concern for the performance stability and reliability of the devices, thus challenging the future scaling of the high- κ metal gate stacks.⁵ In addition, it has been reported that RTN may cause erratic behavior in static random access memory (SRAM).⁶ As a result, RTN is becoming ever more important in the study of the defects and degradation of ultrathin dielectrics.

In the recent studies on RTN and its dependence on the gate voltage, V_g ,^{1,3,4} RTN was typically measured within a narrow range of a relatively high V_g , well above the typical device operating voltage V_{op} , where the RTN signal was always clearly observed. For example, in the study of a 3 nm HfO₂ and 1 nm SiO₂ stack, Lee *et al.* reported RTN measurements for $V_g = 1.9 - 2.3$ V.¹ Such studies on RTN characteristics mainly determine the traps energy and spatial locations. However, the “lower limit” of V_g where RTN can be observed, and how this “lower limit” of V_g changes as a function of dielectric degradation are as yet mostly unexplored. We name this V_g “lower limit” as the triggering voltage, V_{trig} , for RTN. In addition, it is important to evaluate the value of V_{trig} by comparing it with the V_{op} . This work studies the LFN (including both 1/f and RTN components) of post-BD HfLaO gate dielectrics at very low V_g range, close to the V_{op} . The focus will be on the I_g measurement at

low V_g range and the evaluation of device instability and reliability concerns from RTN on normal operation of ultrathin high- κ metal gate stacks, using V_{trig} as a parameter of interest.

The studied devices were nMOSFETs with a TiN/HfLaO (~ 2 nm)/p-Si stack and nearly zero interfacial layer (IL). The channel length (L) of the tested transistors was 70 nm, and the channel width (W) ranged from 90 to 200 nm. The samples were first subjected to time-dependent dielectric breakdown (TDDB) by constant voltage stress (CVS) with different gate current compliance levels (I_{gl}) of 0.5 μ A, 1 μ A, 2 μ A, and 5 μ A. CVS was carried out with $V_d = V_s = V_{sub} = 0$ V and the stress voltage $V_{gstress} = 2.7 - 3.6$ V at room temperature. Upon detecting a BD event, a multiple-stage CVS measurement⁷ was carried out for each sample at very low V_g , increasing from 0.1 V up to 1.8 V, with an incremental step of 0.1 V while keeping the measurement duration at each voltage within 100–500 s. The measurements were performed using a Keithley 4200 Semiconductor Characterization System, having a resolution up to femtoampere current level with pre-amplifiers.

The I_g measured versus stress duration for various gate voltages is then analyzed by a fast Fourier transform (FFT) to obtain the power spectral density (PSD)³ in frequency domain. The used frequency range depends on the sampling rate of the I_g measurement during CVS. PSD obtained in this way contains both 1/f noise and RTN, superimposed on the white spectrum noise, which itself includes thermal noise and shot noise.

I. RTN V_{TRIG} EXTRACTION FROM POST-BD I_g IN TIME AND FREQUENCY DOMAINS

Figure 1(a) shows an example of a typical post-BD I_g measured at low V_g after TDDB capped with $I_{gl} = 2$ μ A. The post-BD I_g was measured by multiple-stage CVS for

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FIG. 1. (Color online) (a) An example of post-BD time dependent I_g from a TiN/HfLaO/p-Si nMOSFET after suffering an $I_{gl}=2\mu\text{A}$ BD. Time dependent CVS data of $V_g=0.6\text{V}$ – 1.4V is shown. RTN only starts to dominate at high V_g , as shown in the enlarged view of I_g at $V_g=(b)$ 0.8 V, (c) 1.0 V, (d) 1.1 V, and (e) 1.4 V. V_{trig} is used to define the voltage at which RTN starts to dominate in I_g .

$V_g=0.6\text{V}$ – 1.4V . It can be seen that at very low V_g of less than 1.1 V, I_g shows no clear RTN signal, such as the example of I_g at $V_g=0.8\text{V}$ shown in Fig. 1(b). Figures 1(c), 1(d), and 1(e) show the enlarged view of I_g at $V_g=1.0\text{V}$, 1.1 V, and 1.4 V, respectively, where $V_g=1.0$ – 1.1V is the transitional voltage range, above which RTN signal can be observed. Thus, here $V_g=1.1\text{V}$ is qualitatively extracted as the RTN triggering voltage, V_{trig} . This voltage V_{trig} demarcates I_g into two parts: RTN signal dominates I_g when $V_g \geq V_{trig}$, while other types of noise—such as $1/f$ noise and/or white noise—dominate I_g when $V_g < V_{trig}$. In other words, RTN fluctuations in I_g could possibly affect the performance of this particular degraded device only for $V_g > 1.1\text{V}$.

To confirm the presence of V_{trig} , we performed an FFT analysis to obtain the PSD of I_g . RTN and other components ($1/f$ noise or white noise) of LFN can be distinguished by the slope γ in the $1/f^\gamma$ fitting of the PSD. White noise is characterized by the slope value $\gamma=0$, while $1/f$ noise will show $\gamma=1$. Finally, pure RTN will show a Lorentzian profile with $\gamma=2$, especially at the higher frequency range. For the post-BD I_g shown in Fig. 1, the corresponding $1/f^\gamma$ LFN is obtained, and it will be shown that the γ value highly depends on two parameters: gate bias V_g in CVS and BD hardness I_{gl} .

FIG. 2. (Color online) PSD is fitted with $1/f^\gamma$ for various post-BD V_g , from the series of measurements where the TDDb was capped at $I_{gl}=2\mu\text{A}$. (a) For $V_g=0.8$ – 1.0V , $\gamma < 1.50$. $1/f$ noise dominates at $V_g=0.9$ – 1.0V and is overwhelmed by white noise below 0.9 V. (b) For $V_g=1.1\text{V}$ and above, $\gamma > 1.50$ and increases with V_g . RTN starts to dominate at $V_g=1\text{V}$. Plots have been scaled accordingly (by a factor of 0.1 to 1000 as labeled) so that the PSD data for different gate voltages (V_g) can be seen clearly.

The PSD obtained from the I_g data in Fig. 1 was fitted with $1/f^\gamma$ and the corresponding γ was extracted as shown for each V_g in Fig. 2. Figure 2(a) shows the PSD for low V_g at 1.0 V or less, and the absence of RTN that was implied by Fig. 1 is now confirmed by the corresponding γ values, where γ equals 1.10 or less. At $V_g = 1.0$ V, the slope $\gamma = 1.10$ indicates $1/f$ -noise dominance. For V_g at 0.9 V and 0.8 V, γ decreases to 0.80 and 0.20, indicating strong presence of white spectrum thermal/shot noise. In similar agreement to the observation in Fig. 1 that clearer RTN fluctuations in the time domain can only be observed when V_g is greater than 1.1 V for this sample, the PSD plots in frequency domain in Fig. 2(b) show that γ is 1.55 at $V_g = 1.1$ V and increases further with $V_g > 1.1$ V. In Fig. 2(b), the rising values of γ to over 1.50 indicate that RTN becomes more dominant with increasing V_g . The high dependency of the γ value on V_g in the frequency domain matches well with time domain observations in Fig. 1 that RTN only starts to dominate in I_g beyond a certain critical value of V_g . Therefore, from both the time and frequency domain analysis, we found a consistent value of $V_{trig} = 1.1$ V for this dataset when $I_{gl} = 2 \mu\text{A}$. The plot of PSD slope γ versus V_g as a function of I_{gl} is shown in Fig. 3, where the γ evolution from a sample at each I_{gl} is represented by one line. There is a fast “transit” from low to high values of γ before $\gamma = 1.5$ observed for every I_{gl} . Based on the overall trend of γ and the fast “transit,” $\gamma > 1.5$ is chosen as the criterion to extract V_{trig} .

Experimental procedures similar to those discussed above were repeated on other samples of the same gate stack with I_{gl} ranging from 0.5 to 5 μA , where at least 10 samples were tested for each I_{gl} . The dependence of V_{trig} on I_{gl} , which controls the BD hardness, is summarized in Fig. 4. It can be seen that the mean value of V_{trig} decreases with higher I_{gl} , indicating that RTN starts to occur at lower voltage for more severe BD cases. In fresh devices, only 3 out of 15 tested samples showed RTN signals at $V_{trig} \sim 1.8$ V. V_g was not further raised to avoid stress-induced defects generation during the measurement. At fresh condition, it is believed that RTN arises from process-induced traps or grain boundary defects⁸

FIG. 3. (Color online) Fitting slope γ of PSD vs gate voltage with I_{gl} ranging from 0.5 μA to 5 μA . The value $\gamma = 1.5$ is usually observed after a fast transit from low to high γ values, and therefore $\gamma = 1.5$ is chosen as the criterion to extract V_{trig} .

FIG. 4. (Color online) Box plot for dependence of V_{trig} on I_{gl} for I_{gl} ranging from 0.5 μA to 5 μA . RTN starts to dominate at a lower V_g in BD samples with higher I_{gl} . At least 10 devices were tested per I_{gl} . The dashed line shows V_{op} of around 1 V.

only, where stress-induced traps are not generated yet. For a fair comparison of stress-induced traps generation, only post-BD V_{trig} values are included in Fig. 4.

II. TRANSPORT MECHANISM AND MODEL FOR V_{TRIG} VERSUS I_{GL} DEPENDENCE: PERCOLATION DILATION WITH ADDITIONAL TRAPS GENERATION

Upon dielectric BD, a percolation path⁹ forms in the dielectric, which results in higher conductivity, even for the very soft BD case. In the soft BD, direct tunneling and trap assisted tunneling (TAT) at the percolation path—the weakest spot of the dielectric layer—are considered to dominate the transport mechanism through the 2 nm dielectric layer. The traps located inside or very close to the percolation path can trap/de-trap electrons and induce local changes in barrier height and tunneling probability.¹⁰ Due to coulombic repulsion, an electron trapped inside such a trap could impede the flow of current, giving rise to large current fluctuations.² Strong RTN fluctuations can only be observed under certain V_g when the dielectric traps are aligned close to the Fermi level of the Si channel where strong trapping/de-trapping behaviors occur. It is noted from Fig. 1 that the RTN has a time constant in the range of seconds, inferring that trap relaxation is involved in the TAT process that gives rise to RTN fluctuations.^{11–13} Physical analysis such as scanning transmission electron microscopy/electron energy loss spectroscopy¹⁴ (STEM/EELS) and first-principle density of states calculations¹⁵ support the hypothesis that the traps giving rise to I_g RTN or digital fluctuations in the degraded dielectrics are oxygen vacancies. Note that the size of a dielectric trap is reported to be 0.6–0.8 nm.¹⁶ As the dielectric layer thickness in this experiment is 2 nm, at least one or two traps are needed to form the percolation path, as shown in Fig. 5(a), which is an example of the very soft BD case.

The dependence of V_{trig} on I_{gl} can be treated qualitatively, based on the BD percolation dilation model. The relation between the number of traps and I_{gl} has been reported in the percolation dilation model of the BD path.¹⁴ Physical analyses of the dielectric BD spot by STEM/EELS showed that the oxygen vacancies were radially distributed around

FIG. 5. (Color online) Percolation path dilation process from very soft BD to harder BD with increasing I_{gl} . There are more traps created during the path dilation. (a) At least one or two traps are created to form the percolation path upon soft BD. (b) At higher I_{gl} , the percolation path dilates with more traps created. More traps give more tunneling options and thus make it possible for the trapping/de-trapping behavior to occur at a lower gate bias. (c) An example of harder BD with more traps created at higher I_{gl} .

the center of the BD path. Furthermore, it was reported by Li *et al.*¹⁴ that, with increasing I_{gl} , the size of the BD spot increased with the center being more oxygen-depleted. For example, the diameter of a BD path increased from 30 nm for $I_{gl} = 2 \mu\text{A}$ to 35 nm for $5 \mu\text{A}$ to 60 nm for $35 \mu\text{A}$ in 2.2 nm thick SiON samples.¹⁴ Based on the percolation dilation model, we therefore conclude that higher I_{gl} leads to more traps generated in the BD percolation path, as illustrated in Figs. 5(b) and 5(c).

A recent report based on the trap spectroscopy by charge injection and sensing (TSCIS) technique¹⁷ has extracted the trap density spectrum by analyzing the energy and spatial distributions in stressed dielectrics. In SiO₂, the traps were found to be distributed at 2.2–2.8 eV (density peaks at 2.2–2.6 eV) below the SiO₂ conduction band, while in Al₂O₃ the traps were distributed at 1.8–2.5 eV (density peaks at 1.9–2.1 eV) below the Al₂O₃ conduction band.¹⁷ Based on the TSCIS data in Hf-rich HfAlO,¹⁸ the traps in the dielectric are distributed at energy levels ranging 1.6–1.9 eV below the high- κ conduction band edge, located at 1.2–3 nm distance from the Si-dielectric interface. In addition, a recent proposed trap probing technique called discharge-based multipulse (DMP) technique¹⁹ shows that the traps in HfO₂ dielectrics are distributed at energy levels from –0.4 eV to +0.6 eV with reference to the Si conduction band edge. The above reports on trap energy levels in SiO₂ and different

high- κ dielectrics including Hf-based dielectrics suggest that during the percolation dilation process with increasing I_{gl} , the additional traps were generated at different energy levels and spatial locations inside the dielectrics.

Based on the above analyses, there are two possible scenarios to explain the dependence of V_{trig} on I_{gl} , as observed in Fig. 4. One possibility is that the additional traps are generated at the deeper energy states measured from the dielectric conduction band edge as illustrated in Fig. 6(b). The other possibility is that additional traps are generated at different spatial locations (i.e., traps with longer distance from the interface for carriers to tunnel) as shown in Fig. 6(c). In both of the two cases shown in Figs. 6(b) and 6(c) with an additional trap present, a smaller band bending already can fulfill the requirement to align the trap with the channel Fermi level as compared to Fig. 6(a), therefore a smaller V_{trig} at higher I_{gl} was observed in the experiments. A combination of the above two scenarios may also occur. In either case, increased tunneling options from more traps at higher I_{gl} make it possible for the trapping/de-trapping behavior to occur at a lower gate bias.

In summary, V_{trig} was used as a direct indication of the degradation in dielectrics concerning the impact of RTN on device performance at normal operation voltage to provide a fast evaluation method for reliability assessment. Through both time- and frequency domain analyses of gate leakage

FIG. 6. (Color online) (a) Band diagram of gate stack showing an example of initial degradation with only one trap A generated at lower I_{gl} . Higher V_g bias (e.g., $I_{gl} = 0.5 \mu\text{A}$ & $V_g = 1.3 \text{ V}$) is needed to align the trap with Fermi level for trapping/de-trapping to have RTN signal dominate. There are two possible scenarios to have a lower V_{trig} at higher I_{gl} as shown in (b) and (c). (b) Additional traps are generated as illustrated in Fig. 6(b) with the additional trap B located at a deeper energy state measured from the dielectric conduction band edge as an example. (c) Additional traps are generated at different spatial locations (i.e., traps with longer distance from the interface for carriers to tunnel) with the trap C as an example. In both of the two scenarios, there is less band bending required to align the additional trap with the channel Fermi level comparing with (a), therefore a smaller V_{trig} at higher I_{gl} is observed in experiment. Moreover, the combination of the above two scenarios may also occur.

current from very low to moderate gate bias, the minimum gate voltage to observe RTN in degraded gate dielectrics was extracted at different BD hardness levels (i.e., I_{gl}). An important observation is that V_{trig} was found to be inversely dependent on I_{gl} . This dependence was qualitatively analyzed with the percolation dilation model, leading us to conclude that either additional traps at deeper energy states from the dielectric conduction band or more efficient tunneling pathways are generated at higher I_{gl} .

RTN may give erratic behavior in SRAM operations⁶ and challenge the device functional stabilities and performance.⁵ The observation of an evolution in RTN with respect to various levels of BD hardness is very insightful when operating instabilities in devices and circuits need to be minimized. We suggest that RTN fluctuation will not pose an instability problem, even if the circuit allows a maximum of $0.5\ \mu\text{A}$ leakage from an individual transistor of the current technology, provided that the operating voltage is less than 1 V.

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