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A Super-Resolution CMOS Image Sensor for Bio-Microfluidic Imaging

Tongxi Wang, Xiwei Huang, Qixiang Jia, Mei Yan, Hao Yu, Kiat Seng Yeo

School of Electrical and Electronic Engineering

Nanyang Technological University (NTU)

50 Nanyang Ave, Singapore 639798; yanmei@ntu.edu.sg, haoyu@ntu.edu.sg

Abstract— A super-resolution CMOS image sensor is introduced in this paper for bio-microfluidic imaging. Compared to the traditional scientific CCD or CMOS image sensor, our design achieves the balance between high-sensitivity and high-resolution from system design perspective with the use of single-frame super-resolution. Moreover, the column-parallel image sensor architecture with correlated-double-sampling is deployed for high-speed and low-noise readout. The chip is designed in standard $0.18\mu\text{m}$ CMOS mixed-signal process with area of $2.5\text{mm}\times 5.0\text{mm}$, 128×128 pixel-array and speed of 1750 frames/s. The resolution is improved by 4X by on-chip super-resolution algorithm while large pixel ($10\mu\text{m}\times 10\mu\text{m}$) is employed in image sensor for high-sensitivity.

I. INTRODUCTION

Recently, lensless imaging systems employing scientific CCD and CMOS image sensors have been applied for biomedical imaging applications, such as optofluidic microscopy, cancer cell detection, and medical tomography etc [1-3]. The image sensor for lab-on-chip thereby becomes an emerging need with many design challenges. For bio-microfluidic imaging application, the sample is tested under dime fluidic environment with the needs of low light sensitivity and high-speed readout [2-4]. CCD based image sensor has low speed but high light sensitivity. On the other hand, CMOS based image sensor has high speed but low light sensitivity.

The current CMOS image sensor detector for bio-microfluidic imaging is thereby mainly limited by light sensitivity. In order to improve sensitivity, large pixel size is required, which in turn degrades the resolution. Super-resolution algorithms [5-6] have been explored to improve resolution from system design perspective. The main advantage of super-resolution is to overcome spatial pixel size limitation by leveraging the image information from a few previous frames with improved resolution. The recent demonstration by FPGA-level implementation of super-resolution algorithm [7] is however limited by off-chip data transferring speed and data size.

In this paper, we have designed a high-speed yet high-sensitivity CMOS image sensor with system-on-chip (SoC) integrated super-resolution for high-resolution, which is the first CMOS image sensor chip targeted for bio-microfluidic

imaging application. The larger pixel size ($10\mu\text{m}\times 10\mu\text{m}$) is implemented to improve the low light sensitivity. To recover resolution, super-resolution algorithm is implemented on chip by trading time information for space limitation. As such, the image resolution is improved by 4X as shown by experiment. In addition, a column-parallel readout with correlated-double-sampling (CDS) is deployed for high-speed and low-noise. The super-resolution integrated CMOS image sensor is designed with tape-out in standard $0.18\mu\text{m}$ CMOS mixed-signal process, with area of $2.5\text{mm}\times 5.0\text{mm}$, 128×128 pixel-array and speed of 1750 frames/s.

The rest of this article is organized as follows. In Section II, the high-speed column-parallel sensor design with large pixel size is illustrated, and in Section III, the super-resolution SoC implementation is introduced to overcome the physical pixel size limitation. Section IV shows the circuit simulation result and image processing result for one bio-microfluidic example. The paper is concluded in Section V.

II. COLUMN-PARALLEL CMOS IMAGE SENSOR

A. System Overview

The super-resolution CMOS image sensor is designed in Global Foundries standard $0.18\mu\text{m}$ CMOS mixed-signal process. The CMOS image sensor architecture is shown in Figure 1. The sensor array contains 128×128 3T-APS pixels. When one row of sensor array is active, the total 128-column outputs are amplified, converted and processed simultaneously.

As shown in Figure 2, a single-ended switch-capacitance amplifier is designed here as column amplifier. The amplifier gain is adjustable as 1X, 2X and 4X according to different lighting conditions. There are three advantages of this design: i) to amplify the signal and increase pixel sensitivity; ii) to reduce readout noise as the amplifying stage is close to the pixel; iii) to provide the flexibility to adjust the signal voltage level of A/D conversion (ADC) in next stage. After amplified, the pixel output is converted to digital output by a 10-bit single-slope ADC (SS-ADC) with up-down counter in each column. It not only converts the analog signal to digital but also carries out an additional CDS in digital domain directly [8-10] as shown in the lower part of Figure 2. The converted digital outputs of each row of pixel array are latched and

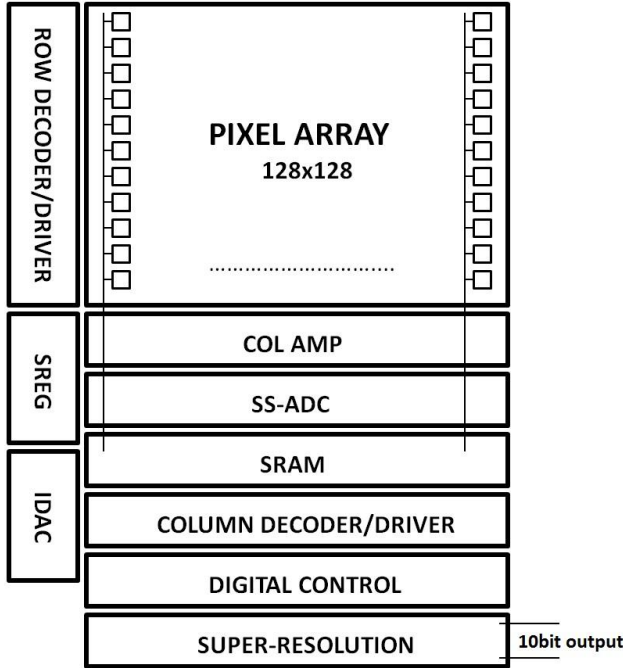


Figure 1. Column-parallel CMOS image sensor architecture with super-resolution processing.

stored in column-wise standard 6T SRAM. Finally, the column decoder selects SRAM data output in serial, read out the data by sense amplifier (SAMP) and then pass the data to super-resolution processing block. This block analyzes the captured imaging data in real-time, and the final processed higher-resolution image data is driven off-chip by a 10-bit bus. Note that all digital timing control signals are implemented on-chip as digital control block.

B. Trade-off for Sensitivity and Resolution

Driven by the lower cost and high resolution, the trend of pixel size is becoming smaller and smaller even into sub-micron range. However, the small pixel size degrades the sensor performance, such as quantum efficiency and SNR sensitivity under the low light condition. For the sake of bio-microfluidic imaging application, a large pixel size (10 μ m pitch) is selected in this paper to achieve superior low-light sensitivity. Meanwhile, the light exposure time for large pixel is much less, which in turn can speed up the frame rate. However, one consequence is that the sensor space resolution is degraded, which cannot recognize the small sample less than 10 μ m. As discussed in the next section, an on-chip super-resolution image processing is implemented to leverage the high-speed CMOS image sensor with large sized pixel. As such, one can overcome the physical size limitation and improve the resolution.

III. SINGLE-FRAME SUPER-RESOLUTION IMAGE PROCESSING

Super-resolution (SR) based imaging reconstruction is a method of leveraging the original low-resolution images into a high-resolution image. There are usually two methods: single-frame and multi-frame based SR. Multi-frame method is based on multiple low-resolution images captured from the same

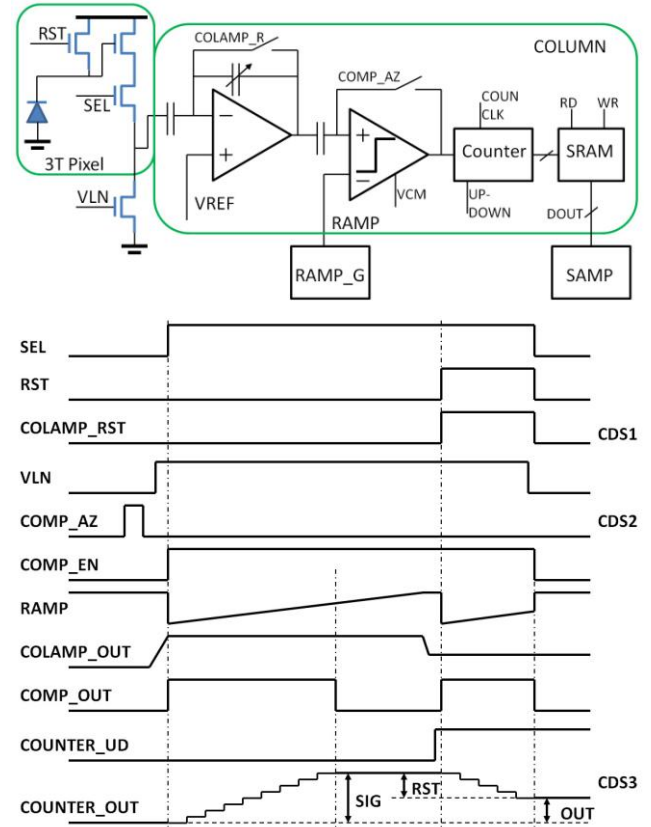


Figure 2. Multiple-CDS readout architecture.

scene by assuming that they can provide different imaging perspectives of the object. Single-frame method is based on a single low-resolution image by assuming that the image of the object is spatially smooth and can be approximately reconstructed by polynomials such as bilinear functions. Since multi-frame SR approach requires huge memory to process data, while single-frame SR processes the data immediately after one row readout, the single-frame SR approach is employed here in this paper for the on-chip SoC integration.

The single-frame SR with bilinear interpolation is designed on chip through the standard ASIC synthesis flow by Verilog. The overall working principle is explained in Figure 3. After A/D conversion, the 10-bit digital output data from the whole sensor array in terms of 128-row and 128-column is transferred in serial into a data buffer within SR block. They are then processed in a ping-pong style as follows.

Phase I Data pumping : As shown in Figure 3 (a), the total 128 pixel output data from the first row ($N_1, N_2 \dots N_{128}$) and the first 2 pixels of the second row ($(N+1)_1, (N+1)_2$) are first pumped into the data buffer array;

Phase II Data processing: During this phase, the targeted original pixel data (N_1) will reconstruct 4×4 "new" high-resolution pixels ($N_1, P_1, P_2 \dots P_{15}$) by bilinear interpolation, as shown in Figure 3 (b). The new 4×4 pixel data are generated based on the original targeted pixel N_1 and 3 reference pixels ($N_2, (N+1)_1, (N+1)_2$); then driven off-chip to represent the original 1-bit data (N_1);

Phase III Data pumping: The data is continuously pumped in and the second original pixel N_2 moves to the processing position. Combined with 3 reference pixels (N_3 , $(N+1)_2$, $(N+1)_3$), it will generate another group of 4×4 pixels in the similar fashion and are driven off-chip after being processed, as shown in Figure 3 (c).

As a result, the original data of 128×128 pixel-array with $10 \mu\text{m}$ resolution will generate processed data of 512×512 with

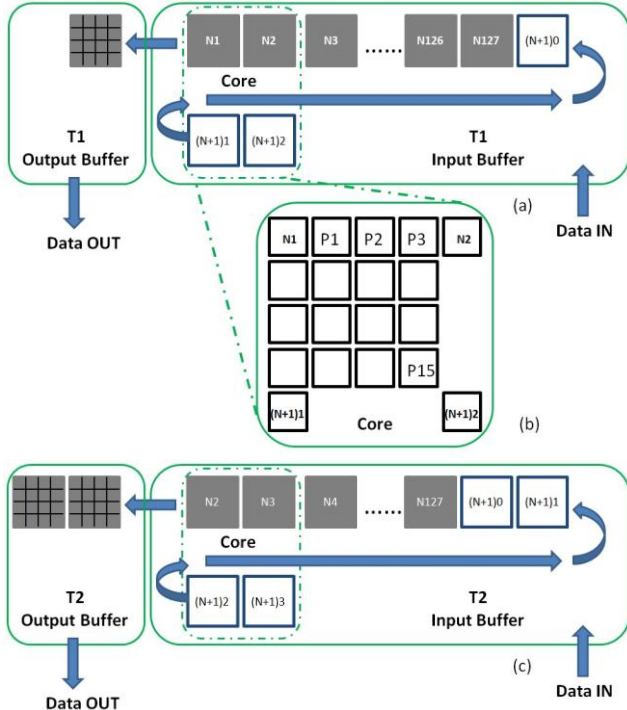


Figure 3. Working principle of bilinear interpolation employed in single-frame super-resolution.

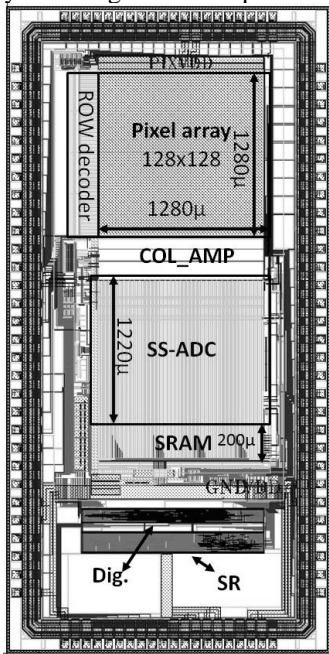


Figure 4. Overview of the super-resolution CMOS image sensor chip layout.

$2.5 \mu\text{m}$ resolution. Note that usually all of three reference pixels are available. However, when special condition occurs that all three reference cells are not available during the interpolation, an average interpolation is employed instead. In addition, the whole processing block only needs one processing core and two data buffers to store the data before and after processing, which can be conveniently demonstrated by on-chip ASIC implementation.

IV. CHIP PERFORMANCE

The chip is manufactured in standard $0.18 \mu\text{m}$ CMOS mixed-signal process (GF 1P6M). The layout of the overall chip is shown in Figure 4. The total chip area is $2.5 \text{ mm} \times 5.0 \text{ mm}$, where the pixel array size is $1.28 \text{ mm} \times 1.28 \text{ mm}$, column readout occupies $1.28 \text{ mm} \times 1.6 \text{ mm}$, and the remaining is for digital core implementation where the on-chip super-resolution processing block only needs area of $0.16 \text{ mm} \times 1.4 \text{ mm}$. A large clock bus with group buffers employed to handle a high frequency of 800 MHz clock, which is the speed of the up-down counter in the ADC. Note that the power consumption is not the focus for the bio-microfluidic imaging application but can be further improved in future work. Table 1 summarizes the achieved design specification for the super-resolution CMOS image sensor, which is the first super-resolution CMOS image sensor in literature based on standard $0.18 \mu\text{m}$ CMOS mixed-signal process.

Figure 5 shows the readout simulation results of the designed CMOS image sensor. The whole row-readout time is $1.7 \mu\text{s}$, where signal V_{sig} readout needs $1.28 \mu\text{s}$ and the reset V_{rst} requires $0.32 \mu\text{s}$. During the row-readout time, the 10-bit single-slope ADC operates at 800 MHz clock in order to convert one whole row data within $1.7 \mu\text{s}$. During the signal readout phase, the pixel output is amplified through column amplifier. The voltage level also moves up to the reference voltage level and is connected to the ADC comparator input. The pixel data of one row is stored in the column-wise SRAM and is then sent to digital processing block. The SRAM readout time can achieve $20 \text{ ns}/\text{column}$. Therefore, the total readout speed from SRAM output can achieve 1750 frame/s .

We also verified the on-chip single-frame SR image processing algorithm for bio-microfluidic imaging application. Colloid particle such as polystyrene bead is a common method to simulate the cell behaviour in bio-microfluidic imaging

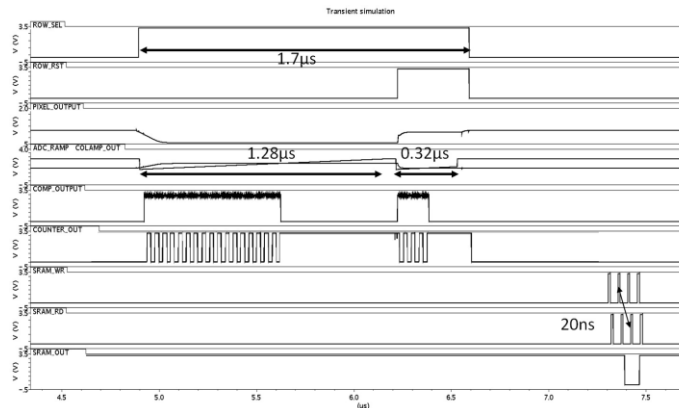


Figure 5. Simulation results of readout by column-parallel image sensor with multiple-CDS.

system (as shown in Figure 6). Figure 7 (a) shows the picture of colloid particle flowing in microfluidic device. The particle has diameter $15.7\mu\text{m}$ similar to the size of a cancer cell. The original image of particle (8×8) is processed, shown in Figure 7 (b), by the on-chip single-frame SR algorithm to generate the processed image of 32×32 . As shown in Figure 7 (c), when compared to the original picture, the image after super-resolution processing shows more details with 4X improved resolution of the particle. Therefore, a high-speed CMOS image sensor with SR on-chip processing ability can significantly improve the measurement throughput with good accuracy when using bio-microfluidic imaging system.

V. CONCLUSION

The design of super-resolution CMOS image sensor chip is presented in this paper for high-resolution, high-sensitivity yet high-speed measurement in bio-microfluidic imaging system. The chip is designed with 128×128 pixel-array and area of $2.5\text{mm} \times 5.0\text{mm}$ in standard $0.18\mu\text{m}$ CMOS process (GF 1P6M). When using the on-chip super-resolution processing, the resolution is improved from $10\mu\text{m}$ physical pixel resolution to $2.5\mu\text{m}$ effective resolution with 4X improvement. The CMOS image sensor readout speed can achieve 1750 frames/s due to column-parallel architecture. The proposed design can be applied in the bio-microfluidic imaging system for cancer cell detection.

TABLE I. SPECIFICATIONS OF SUPER-RESOLUTION IMAGE SENSOR

| | |
|----------------------------|---------------------------------------|
| Technology | 0.18 μm 1P6M standard CMOS |
| Chip area | 2.5mm \times 5.0mm |
| Pixel array | 128 \times 128 |
| Pixel pitch/fill factor | 10 μm /56.35% |
| Power supply voltage | 3.3V |
| Power consumption (Analog) | 105 μA /column |
| Frame rate | 1750 frame/sec |
| ADC | SS-ADC 10-bit |

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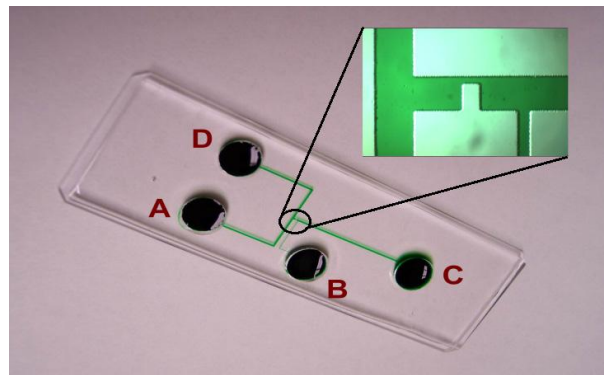
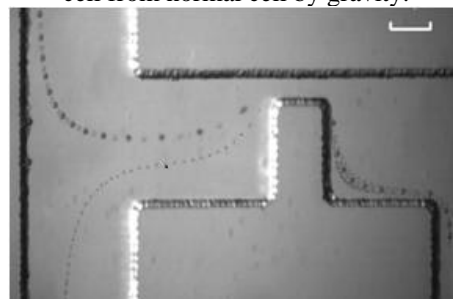
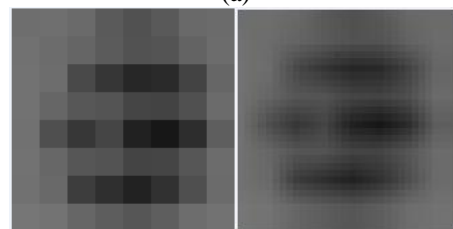


Figure 6. Bio-microfluidic device to separate cancer cell from normal cell by gravity.



(a)



(b)

(c)

Figure 7. Particle image result of single-frame super-resolution algorithm.

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