A signal folding neural amplifier exploiting neural signal statistics

Chen, Yi; Basu, Arindam; Je, Minkyu

2012

Chen, Y., Basu, A., & Je, M. (2012). A signal folding neural amplifier exploiting neural signal statistics. 2012 IEEE Biomedical Circuits and Systems Conference (BioCAS), 304-307.

<https://hdl.handle.net/10356/96881>

<https://doi.org/10.1109/BioCAS.2012.6418456>

© 2012 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. The published version is available at: [<http://dx.doi.org/10.1109/BioCAS.2012.6418456>].

Downloaded on 26 Apr 2023 22:57:24 SGT

A Signal Folding Neural Amplifier Exploiting Neural Signal Statistics

Yi Chen^{*}, Arindam Basu[†] and Minkyu Je[‡]

^{*}[†]School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

[‡]Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685

Email: ^{*}ychen3@e.ntu.edu.sg; [†]arindam.basu@ntu.edu.sg; [‡]jemk@ime.a-star.edu.sg

Abstract—A novel amplifier for neural recording applications that exploits the $1/f^n$ characteristics of neural signals is described in this paper. Comparison and reset circuits are implemented with the core amplifier to fold a large output waveform into a preset range enabling the use of an ADC with less number of bits for the same effective dynamic range. This also reduces the transmission data rate of the recording chip. Both of these features allow power and area savings at the system level. At the receiver, a reconstruction algorithm is applied in the digital domain to recover the amplified signal from the folded waveform. Other features of this proposed amplifier are increased reliability due to removal of pseudo-resistors, less distortion and low-voltage operation. Measurement results from a 65nm CMOS implementation of a prototype are presented.

I. INTRODUCTION

The development of micro-electrode arrays (MEA) has opened up a pathway for directly monitoring large scale neural activity of the brain. Several neural recording and stimulation systems integrated with MEA [1] [2] have been reported recently with possible applications in brain disease detection and prevention, prosthesis and fundamental research in neuroscience. However, these applications put severe constraints on power and area of the neural recording system.

A typical implanted neural recording system, as illustrated in Fig. 1, includes on-site front-end amplifiers for signal conditioning, analog-to-digital convertor (ADC) and wireless transmitter for streaming data out of body. The specifications of the system are derived from the neural signal characteristics which broadly fall in two categories: ‘fast but small’ spikes with amplitudes less than $100 \mu V$ and bandwidth of around 5 kHz and ‘large but slow’ local field potentials (LFP) with amplitudes up to 2 mV but bandwidth less than 100 Hz. Since both signals contain information for the planning of motor activity [3], the number-of-bits (NOB) of the ADC is determined by the dynamic range set by the LFP while the sampling rate is governed by the spike bandwidth. The successive approximation (SAR) topology is a typical choice in neural recording system due to its good tradeoffs between power, speed, area and accuracy. In general, the area and worst-case power consumption of SAR-ADC increase exponentially with increasing NOB [4] making joint acquisition of spike and LFP challenging. Moreover, high channel count of implanted neural recording system create heavy data traffic in wireless transcutaneous transmission and consumes a large amount of power. Obviously, the bit-rate (BR) of data transmission is also proportional to the NOB of the ADC. Finally, creating a high-pass corner at very low frequencies to capture the LFP

Fig. 1: **Proposed Neural Recording System:** The diagram shows signal chain of the proposed neural recording system.

poses some reliability issues [5].

In this paper, a capacitive amplifier topology using comparison and reset circuits is introduced to fold a large output signal into a small range. We exploit the fact that neural signals are not ‘large’ and ‘fast’ at the same time to effectively reduce the dynamic range of signals processed by the ADC. The NOB of the ADC can thus be reduced, saving area and power consumption as well as reducing BR of wireless data transmission. The pseudoresistor (PRes) typically used to bias these capacitive amplifiers, can also be removed since the DC level can be defined by the comparison and reset scheme, leading to improved reliability.

To illustrate this novel signal folding scheme, we consider a neural recording system with a noise floor of $2 \mu V$. Assuming the maximum input voltage range for LFP is 2 mV, the dynamic range is 60dB, leading to a 10-bit ADC resolution. With a gain of 500 provided by the amplifier, input range of the ADC should be 1 V in order to cover whole range of neural signal, between two solid lines as shown in Fig. 2 (a). Reducing the NOB by 2, the input range of ADC narrows to 250 mV. As shown by the horizontal dashed lines in Fig.2 (a), applying this 8-bit ADC directly to neural signal, information beyond the input range is lost. However, in the proposed amplifier, the output signal is reset to a common DC level (vertical dashed lines) whenever it goes higher than a comparison threshold. Setting the threshold to be 250 mV, as shown in Fig. 2 (b), the output signal is folded into a smaller range that fits the input range of an 8-bit ADC. All information can thus be digitized by a ADC with reduced NOB. A reconstruction process is needed to recreate an amplified version of original input signal after the data is transmitted out of the body.

Fig. 2: **Signal Folding Concept:**(a) A 10-bit ADC is needed to cover the whole range of the large output from the amplifier. (b) Applying the proposed scheme, a large signal is folded into a small range that fits the input range of a 8-bit ADC.

Fig. 3: **Proposed Neural Amplifier - Die Photo and Schematic:** The rectangle in left part shows the area of proposed amplifier on die. Comparison and reset circuits are used to fold the output signal of the amplifier. Unlike the conventional AC-coupled capacitive amplifier, pseudo-resistors are not used.

II. PROPOSED DESIGN

Fig. 3 demonstrates the circuit schematic of our proposed fully differential neural amplifier. The core amplifier employs the typical AC-coupled capacitive feedback topology with the closed-loop gain G fixed to C_1/C_2 and the low pass corner of the amplifier set to be $G_m/2\pi AC_L$, where G_m is the transconductance of the OTA and C_L is load capacitance. The outputs are compared with two threshold voltages V_{hi} and V_{lo} . Whenever any one of the outputs is higher than V_{hi} or lower than V_{lo} , a narrow pulse will be generated by the 'reset generator' block, resetting the input and output nodes of the amplifier to V_{incm} and V_{cm} respectively. The amplifier will continue its amplifying function after reset. The output signal of the amplifier is then folded into a voltage range defined by V_{hi} and V_{lo} . Since PRes are removed, the input nodes of the OTA become floating after reset with the DC bias being provided by the charge stored on these nodes. Due to leakage current on this node, the output DC level will shift away from V_{cm} until the reset circuit is triggered again. This scheme allows us to define the input DC level in the absence of PRes. The low-frequency components added to output signal due to the slow ramping can be easily eliminated by a high pass filter after reconstruction in digital domain.

The OTA used in the proposed circuits is a single stage folded-cascode amplifier. The tradeoffs involved in the design of these amplifiers and transistor sizing strategies to minimize noise are elaborately discussed in [6] and [7] and we only mention some salient features of our design. A large current scaling (8:1) between input branch and output branch is

employed to reduce the power consumption. Since this is a fully differential circuit unlike [6] and [7], a common mode feedback circuit is used to define the output DC level to be V_{cm} . Finally, the input devices for the differential pair are chosen to be thick oxide devices to eliminate gate leakage current problems at the input node.

Two different comparators are used in the comparison and reset circuits. In the comparator used for high threshold comparison, $nFET$ s are used as input transistors in order to extend common mode input range of V_{hi} towards V_{DD} . The input stage with two positive inputs provide an OR operation so that the comparator will be triggered whenever one of the positive inputs is higher than V_{hi} . The comparator for low threshold comparison is identical to this one but with all $pFET$ s being replaced by $nFET$ s and vice versa.

There are several benefits of implementing this scheme of comparison and reset with the amplifier:

- **Reducing ADC resolution and transmission bit-rate**
As shown earlier, the proposed scheme can reduce the required input dynamic range of the ADC by folding a large output signal into a small range, leading to area and power savings. This also proportionally reduces the number of bits to be transmitted.
- **Reducing high pass corner for LFP acquisition**
The leakage current at the input nodes of OTA, which can be modeled as a parasitic resistor R_{leak} , forms a high pass filter with the effective capacitance at input node. The corner frequency of this filter, $1/2\pi R_{leak}(C_1 + A_o C_2)$, is much lower than that formed by PRes and feedback capacitor ($1/2\pi R_{leak} C_2$) where A_o denotes open-loop gain of OTA. This guarantees a low enough corner frequency to capture LFP signals.
- **Increasing reliability**
The reliability of resistive elements higher than $10G\Omega$ is still questionable [5]. Higher reliability is achieved in the proposed circuit by replacing PRes with asynchronously operated switches.
- **Reducing distortion and enabling low-supply voltage operation**
The output signal is confined in a small voltage range so that distortion caused by the amplifier is reduced. Also, since a large signal is folded in to a small range, reduced power supplies can still provide high 'effective' dynamic range.

This scheme is general and can be used with any amplifier topology. It can also be used with amplifiers using PRes to relax the ADC design.

III. RECONSTRUCTION

In order to recover the amplified signal, a reconstruction process is applied to digitized signal after ADC. This is the crux of our ability to reduce dynamic range and relax the ADC design without losing any large signals. As illustrated in Fig. 4, the present reconstruction algorithm consists of three steps:

- 1) **Setting the reset flags**

Fig. 4: **Reconstruction Algorithm:** Top: Setting the reset flag. Middle: Interpolation and prediction. Bottom: Correction

To find the times at which a reset event occurred, the derivative of the output signal is computed and compared with a threshold. If it is larger than the threshold, a reset event is declared. This is possible because of the $1/f^n$ characteristic of neural signals whose derivative is much slower than fast reset events.

2) Interpolation and prediction

Due to the bandwidth and slew rate limitation of OTA, the neural amplifier needs a short period of settling time to recover from reset mode back to amplifying mode. So data points in this short period as well as resetting period (if any) will be discarded. In order to predict the value of discarded data, a polynomial interpolation (P) is performed to link the *derivative* of the waveforms before and after reset. Finally, by integrating P, we can predict the value of the discarded data points as well as the first data point after settling.

3) Correction

Every reset introduces a DC level shift between data points before and after it. To recover the original waveform, a 'correction' should be added to all data after every reset. This correction is given by the difference between predicted and original value of the first data after settling. After correction, the waveform before and after resetting will join to form a smooth curve.

This algorithm is currently implemented in MATLAB and can be moved to hardware in the future.

IV. MEASUREMENT RESULTS

The proposed neural amplifier is implemented in UMC 65nm CMOS technology with a V_{dd} of 1.2V. Its die photo is shown in Fig. 3. The PRes is also fabricated on this chip and is selectable by a digital bit allowing us to compare the conventional and proposed topologies. The OTA and the comparators dissipate the bulk of the supply current. The mid-band gain of amplifier is 39.6 dB while the low-pass corner can be tuned by an on-chip DAC. When the bias current is $1.6\mu A$ (including the bias current of comparators), the low-pass corner is 7.7kHz -high enough for neural recording application. As the key innovation for proposed amplifier is the signal folding and reconstruction scheme (which can be used with any amplifier design), we do not compare noise efficiency factor (NEF) here with other designs. The final amplifier design for our system has a gain of 500 and is

Fig. 5: **Measured Signal Folding:** (a) Input signal for amplifier is a 10Hz 6mV peak-to-peak sinusoid. (b) Output waveform of proposed amplifier.

Fig. 6: **Measured Reconstruction Results for 10Hz 6mV peak-to-peak input:** (a) Digitized Differential Output signal. (b) Reconstructed signal waveform.

Fig. 7: **In-vitro Testing Results:** Reconstructed spike signal.

under fabrication; however, we can prove the concept of signal folding with this prototype.

Fig. 5 demonstrates the signal folding of proposed amplifier when the input is a 10Hz 6mV peak-to-peak sinusoid. The V_{lo} , V_{hi} and V_{cm} are fixed at 0.4V, 0.6V and 0.5V respectively. The output waveform of amplifier is shown in Fig. 5(b).

In order to test the proposed reconstruction algorithm, the output signal of amplifier is digitized by a NI measurement platform at a sampling rate of 20kHz. The digitized signal is processed by the Matlab-based reconstruction algorithm to recover the amplified signal. Fig. 6(a) and (b) are the digitized differential output signal and reconstructed waveform respectively when the algorithm is applied to the folded signal.

To validate the ability of this amplifier to record from a high impedance probes, an in-vitro testing is performed by coupling the input to saline solution. A pre-recorded spike waveform is repeatedly played by an arbitrary waveform generator and also coupled in the solution. Fig. 7 shows the recovered spike

Fig. 8: **SNDR Boundary:** Maximum and minimum possible SNDR in the case of (a) $n=2$ and (b) $n=4$.

signal recorded from this setup proving the viability of this scheme.

The reconstruction process introduces some errors in the output signal at every correction step - more the number of resets, more is the error. The spectrum of this error is multiplied by a low-pass transfer function with a corner at the digitally set high pass corner [8]. To quantify this signal dependent error of the proposed neural recording system, input sinusoids with different amplitudes and frequencies are used as input. Based on the spectrum of reconstructed signal, the total noise including reconstruction error can be calculated by integration. We observe that when output signal amplitude is smaller than comparison threshold, the reset is caused by ramping DC level and the resulting error is small and independent of the input sinusoid. In that case, input-referred total noise is around $2.8 \mu V$ in LFP band (1Hz to 150Hz) and $3.8 \mu V$ in spike band (200Hz to 5kHz). When signal amplitude is larger than comparison threshold - corresponding to large LFP signal, the reset can also be caused by signal itself. These signal-triggered reset events then become major error contributors in the LFP band. However, these errors do not affect the noise in spike band due to its low-pass spectrum.

According to the observation above, the total noise of proposed amplifier can be divided into two parts:

$$\overline{V_n}^2 = \overline{V_{n1}}^2 + \overline{V_{n2}}^2 \quad (1)$$

where $\overline{V_{n1}}$ is signal-independent (including source noise, circuits noise and reconstruction error from DC-ramping-triggered reset events) while $\overline{V_{n2}}$ comes from reconstruction error caused by signal-triggered reset event. Intuitively, $\overline{V_{n2}}$ increases with increasing signal amplitude and frequency since both cause more resets. We simply assume that it varies with input frequency (f_{in}) and amplitude (A_{in}) in a form denoted by the equation below:

$$\overline{V_{n2}}(f_{in}, A_{in}) = \begin{cases} Kg_1(f_{in})g_2(A_{in}) & : A_{in} > V_{th}/G \\ 0 & : A_{in} < V_{th}/G \end{cases} \quad (2)$$

where V_{th} is comparison threshold, K is a constant, G is the closed-loop amplifier gain while $g_1(f_{in})$ and $g_2(A_{in})$ are 1st order polynomial functions of f_{in} and A_{in} whose parameters are obtained from fitting measurement data. However, even with this model, the non-linearity of resets make it impossible

to exactly predict the total error ($\overline{V_{n2,LFP}}$) due to LFP inputs. Instead, assuming a spectrum of the LFP signal given by a/f_{in}^n , we can provide an estimate of $\overline{V_{n2,LFP}}$ as follows [8]:

$$max_{LFP}(\overline{V_{n2}}^2(f_{in})) < \overline{V_{n2,LFP}}^2 < \int_{LFP} \overline{V_{n2}}^2(f_{in})df_{in} \quad (3)$$

where the maximum and integral operations are carried out over all possible input frequencies in the LFP band. We can now plot the boundary of SNDR for various amplitudes 'a' as shown in Fig. 8 for $n=2$ and 4. The X-axis is the output swing for varying 'a' normalized to the comparison threshold. When $V_{out}/V_{th} < 1$, SNDR is input signal limited while it is error limited in the other part. From $V_{out}/V_{th}=1$ up to 4, the SNDR remains above 49 dB implying that signal 4 times larger than ADC input range can be reconstructed with at least 8 bits of accuracy.

V. CONCLUSION

We presented an amplifier that reduces the dynamic range requirement of the ADC by exploiting the $1/f^n$ characteristic of neural signals. This is realized by folding the large output waveform into a small range and recovering it back by a reconstruction algorithm in digital domain after data transmission. Measurement results are presented to prove the viability of the proposed signal folding and reconstruction scheme. The reduced NOB and bit-rate contribute to saving area and power consumed by ADC as well as power and bandwidth of data transmission. Other benefits of this scheme include improved circuits reliability and lower high-pass corner due to elimination of pseudoresistors and reduced distortion and power supply requirements due to smaller signal swing.

VI. ACKNOWLEDGEMENT

The authors wish to thank MediaTek's 65nm IC Shuttle Project for providing chip fabrication facility.

REFERENCES

- [1] R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuits for a wireless 100-electrode neural recording system," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.
- [2] R. Sarpeshkar, W. Wattanapanitch, S. K. Arfin, B. I. Rapoport, S. Mandal, Michael W. Baker, M. S. Fee, S. Musallam, and R. A. Adersen, "Low-power circuits for brain-machine interfaces," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 2, no. 3, pp. 173–183, Sept. 2008.
- [3] M. Mollazadeh, V. Aggarwal, A. Davidson, A. Law, and N. V. Thakor, "Spatiotemporal Variation of Multiple Neurophysiological Signals in the Primary Motor Cortex during Dexterous Reach-to-Grasp Movements," *The Journal of Neuroscience*, vol. 31, no. 43, pp. 15331–43, Oct 2011.
- [4] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy adc for smart dust," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, 2003.
- [5] T. Jochum, T. Denison, and P. Wolf, "Integrated circuit amplifier for multi-electrode intracortical recording," *Journal of Neural Engineering*, vol. 6, pp. 012001, 2009.
- [6] R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
- [7] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 2, pp. 136–147, Jun. 2007.
- [8] Yi Chen and Arindam Basu, "Error Analysis for Signal Folding Amplifier," Tech. Rep., Nanyang Technological University, Dec 2011.