A self-rectifying unipolar HfOx based RRAM using doped germanium bottom electrode

Liu, W. J.; Tran, Xuan Anh; Sun, Xiaowei; Yu, Hongyu

2013

Liu, W. J., Tran, X. A., Yu, H., & Sun, X. (2013). A self-rectifying unipolar HfOx based RRAM using doped germanium bottom electrode. ECS solid state letters, 2(5), Q35-Q38.

https://hdl.handle.net/10356/97684

https://doi.org/10.1149/2.006305ssl

ECS Solid State Letters, **2** (5) Q35-Q38 (2013)
2162-8742/2013/2(5)/Q35/4/$31.00 © The Electrochemical Society

A Self-Rectifying Unipolar HfOx Based RRAM Using Doped Germanium Bottom Electrode

W. J. Liu,[a] X. A. Tran,[b] H. Y. Yu,[c,z] and X. W. Sun[b,c,z]

[a]*Department of Materials Engineering, The University of Tokyo, Bunkyo, Tokyo 113-8656, Japan*
[b]*School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798*
[c]*Department of Electronic and Computer Engineering, South University of Science and Technology, Shenzhen, Guangdong 518055, China*

A self-rectifying unipolar RRAM based on HfO*x* dielectrics using highly doped n-type germanium substrate as the bottom electrode is proposed for the first time. The RRAM cells exhibit a stable unipolar resistive switching behavior. Owning to Schottky barrier between defect states in HfO*x* layer and n-Ge substrate, RRAM cells possess a self-rectifying behavior in LRS which eliminates the read-out errors induced by leakage current paths in cross-bar array structure. The demonstrated RRAM device shows high ON/OFF ratio (>5 × 10^2 @ 0.5 V), and its effective Schottky barrier height is also addressed. The demonstrated HfO*x*-based RRAM devices provide a promising candidate as non-volatile memory devices using Ge-based technology.

Manuscript submitted December 18, 2012; revised manuscript received February 21, 2013. Published March 6, 2013.

Resistive random access memory (RRAM) has emerged as a promising candidate for future generation non-volatile memory owing to its ultra-fast switching, excellent endurance, excellent scalability and CMOS compatibility.[1–3] Recently, the cross-bar architecture, in which memory cells are integrated between the word-and bit- lines, realizing a cell size of $4F^2$ has been proposed for potential RRAM application.[3,4] Unfortunately, the cross-talk interference between memory cells caused by leakage current paths through neighboring cells with low resistances state in cross-bar array can induce read-out errors.[5,6] The resistive switching behavior can be classified into two types: bipolar resistive switching (BRS) and unipolar resistive switching (URS). For the former case, several papers have reported various solutions in the form of devices such as transistors, selection devices and complementary resistive switch (CRS) where the logic bit is coded in two different reset (high resistance) states for bipolar-type RRAM cross-bar integration.[5,7–9] Complementary switch (CS) was implemented by connecting two antiserial memristive elements[5] and then demonstrated in a single oxide layer of HfO*x*.[8] Recently, CS effect in single oxide layers was also observed in TaO*x*-based RRAM.[7] For unipolar RS case, to avoid this cross-talk effect, a rectifying diode (1D) or transistor (1T) integrated with RRAM cell to block sneak current path is demonstrated in several reports.[4,10,11] However, integrating a diode and transistor not only increases fabrication cost, but also leads to the increase of operating voltage and reduce memory performance. Recently, the self-rectifying resistive memory has been actively pursued.[12,13] The self-rectifying RRAM has the obvious rectification in LRS, so the crosstalk phenomenon can be alleviated without serially connecting a diode. In this letter, a unipolar RRAM based on HfOx dielectrics on n^+-Ge substrate is reported. With highly doped n^+-type Ge as a bottom electrode, the memory cell exhibits a rectifying current-voltage behavior in n^+-Ge/HfOx/Ni memory cell, showing Schottky diode characteristics which can alleviate the cross-talk effect in cross-point array.

Experimental

The schematic structure and fabrication process of RRAM cells are shown in Figure 1a and 1b, respectively. Firstly, a highly-doped 4-inch Ge wafer is cleaned using RCA process, which was developed by Radio Corporation of America, to remove the native oxide layer. After that, a 4-nm-thick HfO*x* film was deposited using atomic layer deposition (ALD) at 250°C on Ge substrate. Finally, a 100-nm-Ni top electrode was deposited by physical vapor deposition. Ni electrode was deposited using a reactive radio frequency puttering system in Ar gas flow rate of 14 sccm at a base pressure of 1×10^{-6} mBar. The lift off process is carried out to pattern final devices with area of 25 $\times 25\ \mu m^2$. The electrical measurements were performed using a Keithley 4200-SCS semiconductor parameter analyzer. The voltage is applied on Ni top electrode and Ge substrate is connected to ground.

Results and Dicussion

To operate unipolar resistive switching in RRAM device, a forming process and current compliance setting is required, as shown in Figure 2a. A DC voltage sweep ($V_{Forming} \sim 3.5$ V) is applied to switch HfO*x* layer into low resistance state (LRS). Compliance current is set at 10 µA to protect device from permanent breakdown. After forming process, RRAM device is under very low resistance state, which is denoted as logic "1" in memory application. To switch device into high resistance state, another voltage sweep ($V_{reset} \sim 1.5$ V) triggers the abrupt decrease of current and the resistance switches back to high resistance state (HRS), denoted as RESET process shown in Figure 2b. The HRS of RRAM device is present as logic "0". Afterward, a positive voltage sweeps ($V_{set} \sim 2.5$ V) with a current compliance of 100 µA triggering again the conduction abruptly, and the resistance switches from HRS to LRS, shown in Figure 2b. The polarity independence of the SET and RESET transition indicates the unipolar resistive switching (RS) characteristics. In unipolar RRAM, it is believed that the Joule heating effect plays an important role in the rupture of conductive filaments in reset process,[14,15] where the resistance state changes from LRS to HRS, shown in Figure 2b. From Figure 2b, it is also observed that the devices demonstrate a pronounced rectifying effect at LRS. In LRS, the achieved current in positive direction is >500 larger than that of negative direction, at a 0.5 V reading voltage. It is worth noting that the HRS current seems to be overlapped with LRS current in negative direction. It is found that the rectifying characteristic can be maintained well with temperature as shown in Figure 3, where the temperature is from 25°C to 150°C. The result in insets in Figure 3 is the same data from Figure 3 but plotted in linear-linear scales. The distribution of V_{set} and V_{reset}, switch current for SET and RESET processes (I_{set} and I_{reset}) is presented in Figure 4a and 4b, respectively. In our proposed device, the Joule-heating effect

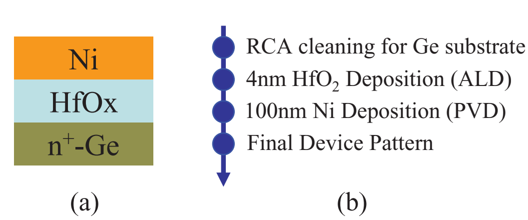

Figure 1. (a) The schematic of the proposed n^+-Ge/HfOx/Ni device. (b) Process flow of fabricated n^+-Ge/HfOx/Ni device.

zE-mail: exwsun@ntu.edu.sg; yu.hy@sustc.edu.cn

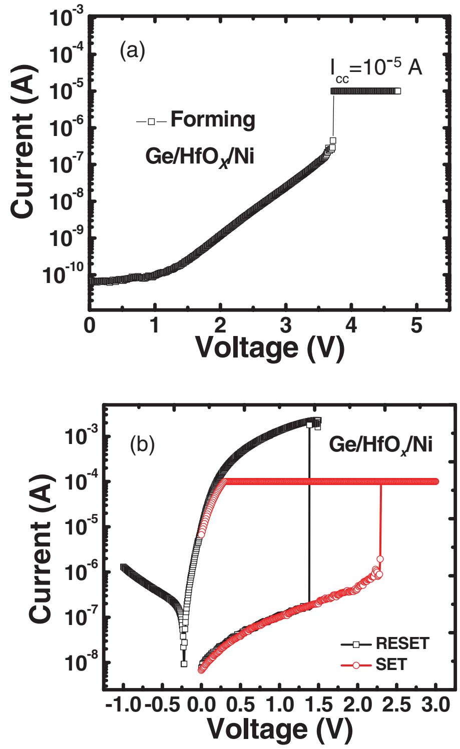

Figure 2. (a) *I-V* characteristics of n^+-Ge/HfO$_x$/Ni cell in RESET Process. (b) *I-V* characteristics of n^+-Ge/HfO$_x$ /Ni cell in SET Process.

is attributed to melt conductive filament in RESET Process. The melting point depends mostly on I_{reset} (V_{reset}). The I_{reset} at 125°C is smaller that that at room temperature (data now shown here), indicating Joule-heating effect plays an important role in resistive-switching process. The distribution of HRS/LRS resistance and endurance characteristic of the memory cell is shown in Figure 5a and 5b, respectively. Good HRS/LRS distribution is achieved and the resistance ratio is larger than 3 orders of magnitude. Retention time for the device were extracted by considering the life time of HRS at different temperature points, and summarized in Figure 5c. It is worth noting that there is no degradation in LRS for 5×10^4 s at 150°C under 0.5 V applied voltage, and the projected retention time at room temperature is around 10^9 s.

Note that the Schottky-diode-like behavior is observed in an n^+-Ge/HfO$_x$/Ni memory cell and the reverse current of n^+-Ge/HfO$_x$/Ni is strongly suppressed and more than 2 orders of magnitude smaller than forward current, shown in Figure 3. The possible mechanism

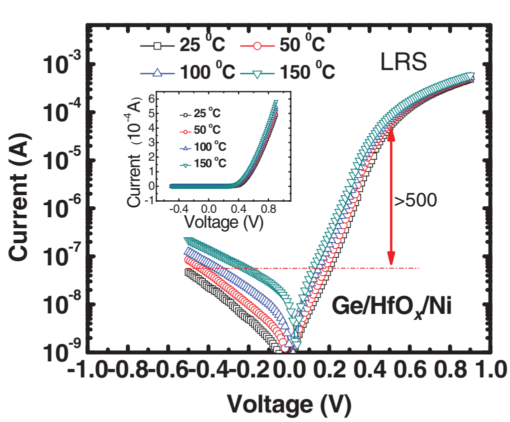

Figure 3. *I-V* characteristics and circuit diagram (inset) of n^+-Ge/ HfO$_x$ /Ni cell in LRS at various temperature.

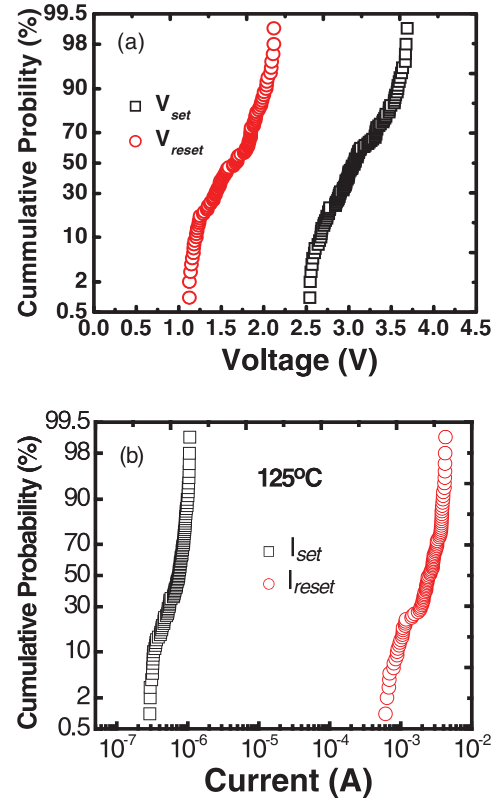

Figure 4. The distribution of SET (V_{set}) and RESET (V_{reset}) voltages (a), SET (I_{set}) and RESET (I_{reset}) current (b).

of self-rectifying effect is described as follows. During SET process, oxygen vacancies (V_o) can be created inside the HfOx dielectric films. These defects may introduce energy level, which initiates percolation paths for electron conduction in HfOx layer. When the device is operated at reverse bias, the injection of electrons from the defect states in HfO*x* into Ge electrode is required. Owing to the Schottky barrier at the Ge bottom electrode and HfO*x* junction, the current transport would be quite suppressed. To exam the self-rectifying *I-V* behavior of n^+-Ge/HfO$_x$/Ni cell in LRS, the transport mechanism of the reverse current is investigated. The thermionic current-voltage (I-V) characteristic of a Schottky barrier diode is given as follows,[16]

$$I = S * A^* * T^2 * \exp\left(-\frac{q\Phi_{B,eff}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad [1]$$

where S is the area of measured RRAM cell, A^* is the effective Richardson constant, k is the Boltzmann constant, $\Phi_{B,eff}$ is the effective Schottky barrier height, T is the absolute temperature, n is the ideality factor. For $V \gg kT/q$, the equation 1 can be written as

$$\ln\left(\frac{I}{T^2}\right) = \ln(S * A^*) - q(\Phi_{B,eff} - V/n)\frac{1}{kT} \quad [2]$$

The $\Phi_{B,eff}$ can be extracted from ln(I/T^2) versus 1/kT (Richardson plot) with a slope of $-q(\Phi_{B,eff} - V/n)$. The n value is 4.7, calculated by fitting the linear region of the I-V curve at room temperature in Figure 3, where the extraction method is the same as the reported.[17,18] The real factor deviates from the ideal value of 1, indicating the formation of inhomogeneous barrier at HfO$_2$/Ge interface, which possibly results from interface states and interfacial layer GeOx between defected HfO$_2$ and Ge.[19] Figure 6 shows the temperature dependence of reverse current of n^+-Ge/HfO$_x$/Ni cell. The 1D1R circuit diagram is schematically shown in inset in Figure 6. The linear expression is done to fit the experimental data and the slope is 0.068. The obtained effective $\Phi_{B,eff}$ at a given voltage of −0.5 V is 0.17e V. Then the Schottky barrier height between the defect states in HfOx dielectric

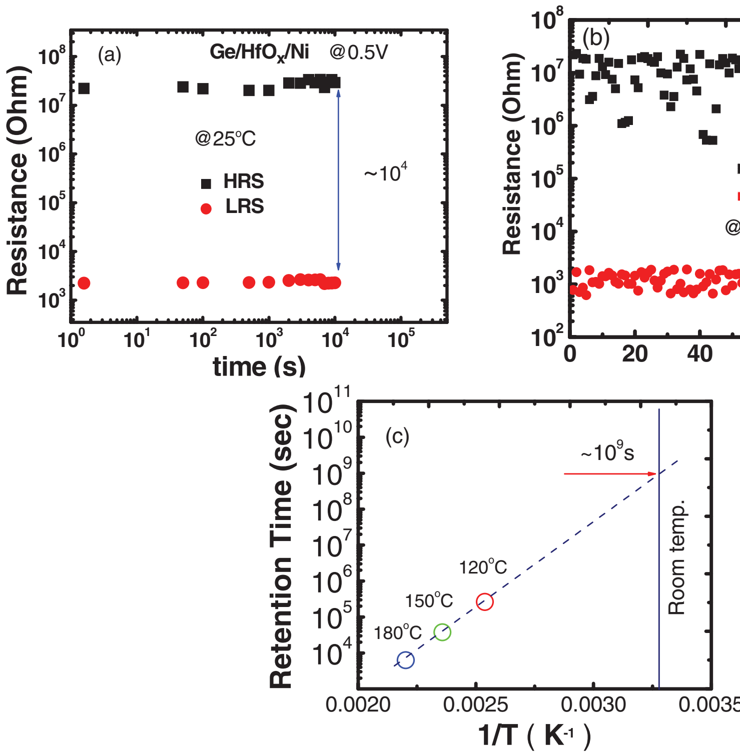

Figure 5. (a) The retention characteristics, (b) endurance characteristic of Ge/HfOx/Ni cell at 125°C, (c) the retention time projected from the life time extracted from HRS at different temperature points.

and Ge substrate is quantitatively addressed. Based on the aforementioned result, the cross-talk effect in the crossbar array structure arrays can be avoided. Leakage sneak paths are reduced significantly compared to the array without the selector device. The circuit simulation showed that the high rectification ratio ensures the crossbar array can function properly even at very large integration.[20] Crosstalk phenomenon can be eliminated if a diode is serially connected to each resistive memory device.

Conclusion

We for the first time demonstrated a self-rectifying unipolar HfOx-based RRAM using highly doped n-Ge substrate as the bottom electrode. The proposed RRAM device exhibits a stable unipolar resistive switching behavior, a self-rectifying characteristic which eliminates the leakage current in a cross-bar array structure. The mechanism of the self-rectifying behavior is investigated using a Schottky diode model and an effective Schottky barrier height is presented. The demonstrated HfOx-based RRAM devices exhibit a promising candidate as non-volatile memory devices using Ge-based technology.

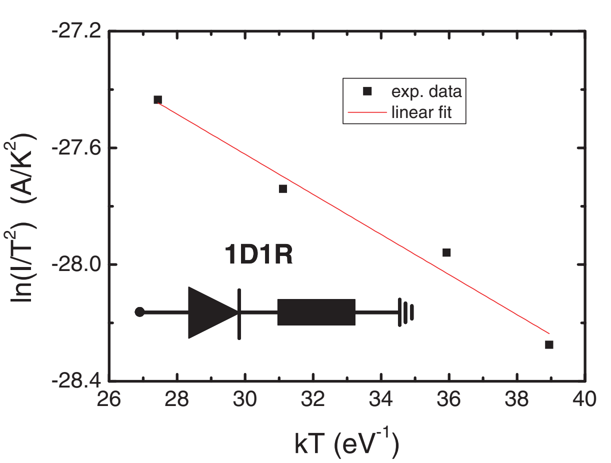

Figure 6. Temperature dependence of reverse current of n$^+$-Ge/HfO$_x$/Ni cell. The schematic of 1D1R is illustrated in inset.

Acknowledgments

This work is supported by Singapore Agency for Science, Technology and Research (A*STAR) (Project No. 092 151 0088). H. Y. Yu acknowledges 1000-plan funding. The work is supported by the National Natural Science Foundation of China (NSFC) (Project Nos. 61006037, 61177014 and 61076015), and Tianjin Natural Science Foundation (Project Nos. 11JCZDJC21900 and 11JCYDJC25800). This work is also partly supported by research fellowship of Japan Society for the Promotion of Science (JSPS).

References

1. B. Gao, H. W. Zhang, S. Yu, B. Sun, L. F. Liu, X. Y. Liu, Y. Wang, R. Q. Han, J. F. Kang, B. Yu, and Y. Y. Wang, *Symp. in VLSI Technology*, 30 (2009).
2. J. Lee, J. H. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park, and H. Hwang, *Tech Dig Int Electron Device Meet.*, 19.5.1 (2010).
3. B. S. Kang, S. E. Ahn, M. J. Lee, G. Stefanovich, K. H. Kim, W. X. Xianyu, C. B. Lee, Y. S. Park, I. G. Baek, and B. H. Park, *Advanced Materials*, **20**, 3066 (2008).
4. B. Lee, S. Seo, D. C. Kim, S. E. Ahn, D. H. Seo, I. K. Yoo, I. G. Baek, D. S. Kim, I. S. Byun, S. H. Kim, I. R. Hwang, J. S. Kim, S. H. Jeon, and B. H. Park, *Advanced Materials*, **19**, 73 (2007).
5. E. Linn, R. Rosezin, C. Kügeler, and R. Waser, *Nature Materials*, **9**, 403 (2010).
6. K. H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, and W. Lu, *Nano Letters*, **12**, 389 (2012).
7. Y. C. Yang, P. Sheridan, and W. Lu, *Applied Physics Letters*, **100**, 203112 (2012).
8. F. Nardi, S. Balatti, S. Larentis, and D. Ielmini, *Tech. Dig. Int. Electron Devices Meet.*, 31.1.1 (2011).
9. G. S. Tang, F. Zeng, C. Chen, H. Y. Liu, S. Gao, C. Song, Y. S. Lin, G. Chen, and F. Pan, *Nanoscale*, **5**, 422 (2013).
10. B. Cho, T. W. Kim, S. Song, Y. Ji, M. Jo, H. Wang, G. Y. Jung, and T. Lee, *Adv. Mater.*, **22**, 1228 (2010).

11. H. Shima, F. Takano, H. Muramatsu, H. Akinaga, I. H. Inoue, and H. Takagi, *Applied Physics Letters*, **92**, 043510 (2008).
12. Q. Zuo, S. Long, Q. Liu, S. Zhang, Q. Wang, Y. Li, Y. Wang, and M. Liu, *Journal of Applied Physics*, **106**, 0737241 (2009).
13. X. A. Tran, W. Zhu, W. J. Liu, Y. C. Yeo, B. Y. Nguyen, and H. Y. Yu, *IEEE Electron Device Letters*, **33**, 1402 (2012).
14. D. Ielmini, C. Cagli, and F. Nardi, *Applied Physics Letters*, **94**, 063511 (2009).
15. W. Shen, R. Dittmann, and R. Waser, *Journal of Applied Physics*, **107**, 094506 (2010).
16. S. M. Sze, *Physics of Semiconductors Devices* (John Wiley & Sons, New York), 258 (1981).
17. M. Jo, D. Seong, S. Kim, J. Lee, W. Lee, J. Park, S. Park, S. Jung, J. Shin, D. Lee, and H. Hwang, *Symp. in VLSI Technology*, 53 (2010).
18. S. Park, S. Jung, M. Siddik, M. Jo, J. park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, B. H. Lee, and H. Hwang, *Phys. Status Solid RRL*, **6**, 454 (2012).
19. D. E. Yıldız, Ş. Altındal, and H. Kanbur, *Journal of Applied Physics*, **103**, 124502 (2008).
20. J. Liang and H. S. P. Wong, *IEEE Transactions on Electron Devices*, **57**, 2531 (2010).