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Design and Scalability of a Memory Array Utilizing Anchor-free Nano-electro-mechanical Non-volatile Memory Device

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Abstract—This letter explains a nano-electro-mechanical (NEM) non-volatile memory (NVM) architecture employing an anchor-free electrode (shuttle) structure. The proposed NEM device utilizes adhesion forces to achieve bi-stable mechanical states for non-volatile data storage. The anchor-free electrode facilitates better scalability compared to conventional anchored NEM devices, which is desirable for circuit applications. The structure is electro-statically actuated and has low operating voltage. A novel memory cell consisting of the proposed NEM memory device and two MOS transistors (1NEM-2T) is proposed for array implementation. Scalability analysis of the proposed NEM NVM array is also presented.

Keywords—Non-volatile memories (NVM), nano-electro-mechanical devices (NEM), Hybrid NEMS-CMOS NVM, Verilog-A, Scalability.

I. INTRODUCTION

CONTINUOUS scaling in MOSFET channel lengths has led to a significant increase in CMOS static energy consumption due to the increase in the sub-threshold leakage current (I_{OFF}). This is a critical concern for both memory and logic devices particularly at high temperatures. In general, scaling of memory cells such as SRAM, DRAM, and FLASH is limited by their tight requirements on the static leakage and immunity to process variations and noise.

Various devices [1]-[3] have been proposed to achieve zero standby leakage, but fail to realize it. To overcome this limit, nano-electro-mechanical (NEM) devices and micro-electro-mechanical (MEM) switches have been investigated [4]-[6] for high temperature (HT) operation. However, conventional anchored MEM structures suffer from poor scalability, which limits the application of them in circuit

implementation. In this letter, we present a NEM NVM array architecture and its scalability based upon the NEM NVM device in [7].

II. DESIGN OF ANCHOR-FREE NEMS NVM

A. Anchor-free NEM NVM device structure and operation

Fig. 1 illustrates the structure of the proposed 3-terminal (D: Drain, S: Source, G: Gate) NEM shuttle memory and its electrical equivalent models [7]. Data retention is obtained by adhesion forces between the shuttle and fixed electrodes. Since the shuttle and the electrodes have smooth and conductive surfaces, Van der Waals force is the dominant adhesion component. A guiding cavity ensures that the free-flying shuttle electrode under vacuum is mechanically switched and has only two stable positions (UP and DOWN). Memory reading is achieved by probing the resistance between the drain and source electrodes, which has an ideally large ratio between ON (resistance: R_{ON}) and OFF (resistance: R_{OFF}) states. The absence of flexural anchors makes the scalability of this NEM structure ($9F^2$) remarkable compared to most anchor-based NEM devices. This is of key importance to achieve reasonable memory density. The mathematical expressions of the key design parameters such as switching voltage and adhesion force are explained in [7].

B. Hybrid NEMS-NMOS memory design

The proposed memory array where each bit cell consists of two access NMOS transistors and one NEM NVM device is illustrated in Fig. 2. For writing, a proper terminal biasing condition has to be loaded in the selected column. After that, a word line is enabled for writing the data into the selected cells. Unlike SRAMs, half-selected cells will not be disturbed by applying the same voltage to all three terminals. For reading, a small signal (V_R) is applied to the selected source line (S1) and is read from the selected drain line (D1) to detect whether the shuttle is in the UP-state or in the DOWN-state. Note that V_R should be smaller than the programming voltage (V_P) to avoid unwanted movement of the shuttle by the electrostatic forces between three terminals (Fig. 3). In order to avoid voltage mismatch issues, the operating voltage of the NEM NVM device must be similar to that of the CMOS circuits for easy

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Fig. 1. Proposed 3-terminal shuttle NEM memory device: (a) top-view layout, (b) AA' 3D cross section in the down-state, (c) AA' 3D cross section in the up-state, (d) electrical equivalent model in the DOWN-state, and (e) electrical equivalent model in the UP-state.

Fig.2. Proposed memory array structure using NEM memory device and two MOS transistors (1NEM-2T).

Fig.3. NEMs NVM cell read and write operations.

integration. Fig. 3 demonstrates simulation results of the NEM NVM array operation including the electrical and mechanical dynamics in [7] and the access transistors in a $0.18\mu\text{m}$ CMOS technology. It can be seen that the small signal can be read only when the shuttle is in the DOWN-state.

III. SCALABILITY ANALYSIS OF THE NEM NVM ARRAY

Miniaturization is desirable for high memory density. A pertinent question is how this continued scaling in dimensions and supply voltage influences the operating characteristics of

TABLE I
SCALING SCENARIOS FOR SHUTTLE NEM NVM DEVICE

Parameter	Full Scaling	General Scaling	Fixed-V Scaling
W, L, d_{gap}	$1/S$	$1/S$	$1/S$
V_{DD}	$1/S$	$1/U$	1
V_P	$1/S$	$1/S$	$1/S$
R_{ON}	$1/S$	U^2/S^3	$1/S^3$
I_{ON}	1	S^3/U	S^3
$t_{\text{mechanical}}$	$1/S^{3/2}$	$1/S^{3/2}$	$1/S^{3/2}$
t_{delay}	$1/S^2$	$1/S^2 U^2$	$1/S^2$
$t_{\text{switching}}$	$1/S^{3/2}$	$1/S^{3/2}$	$1/S^{3/2}$
$P_{\text{switching}}$	$1/S^{3/2}$	$S^{1/2}/U^2$	$S^{1/2}$
$E_{\text{switching}}$	$1/S^3$	$1/SU^2$	$1/S$

the proposed NEM device and the critical design metrics such as switching voltage and power. Various scaling scenarios such as *full scaling*, *general scaling*, and *fixed voltage scaling* have been considered in CMOS technology [8]. Table I summarizes key device parameters of the NEM NVM device after employing each scaling scenario. The device dimension scaling factor is S (with $S > 1$ for a reduction in size) and the voltage scale factor is U . For example, if we assume $1/S = 0.7$ for dimensions (30% scaling per technology generation) and $1/U = 0.85$ for supply voltage (15% scaling per technology generation), V_P scales by 30% in all the three scenarios. Current density increases at a larger rate in the fixed-voltage scaling than the full scaling and general scaling scenarios. The scalability of the cavity limited by lithography overlay is not a major issue since the proposed NEM device is small and planar. An NEM NVM array of 1kb size (32 rows and 32 columns) using the *Verilog-A* model of the proposed NVM device are simulated. Fig. 4(a) demonstrates that the proposed NEM NVM architecture has extremely small leakage with scaling in shuttle gate voltage (V_G). This is primarily due to the steep subthreshold characteristics of the NEM devices. The scaling effect of the shuttle gap thickness (d_{gap}) on NVM array leakage is shown in Fig. 4(b). An increase in leakage can be observed with scaling of gap thickness as the minimum programming voltage (V_P) required for switching the shuttle electrode decreases. Fig. 4(c) presents the effect of the shuttle gap thickness (d_{gap}) on I-V curves of the NEM device. Note that V_P decreases by scaling the shuttle gap thickness, which is corresponding to the switching voltage equation in [7]. Fig. 4(d) illustrates the relationships between switching voltage, adhesion

Fig.4. Simulation results of the proposed NEM NVM array with variations in device parameters: (a) NEM gate voltage, (b) shuttle gap thickness, (c) shuttle gap thickness, and (d) adhesion force.

force, and shuttle gap thickness. Smaller adhesive force lowers V_p as expected from [7]. However, smaller adhesive force degrades the non-volatile capability.

IV. CONCLUSION

A nano-electro-mechanical (NEM) non-volatile memory (NVM) array structure for high temperature data storage is presented from circuit perspective. The proposed NVM architecture utilizes hybrid NEMS-CMOS approach for simple circuit control. Improvements in NEM NVM performance characteristics with scaling was demonstrated (particularly in leakage, which is a larger component of power consumption in CMOS technology at high operating temperature), highlighting the scope of anchor-free NEM NVM architecture compared to anchored NEM structures. Simulation results show that the proposed NEM NVM has great potential to be adopted as a memory solution for high temperature ($T > 250^\circ\text{C}$) applications.

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