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Adaptive Gate Switching Control for Discontinuous-Conduction Mode DC-DC Converter

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Abstract—This work aims to develop a novel adaptive gate switching controller (AGSC) for discontinuous-conduction mode (DCM) DC-DC converters, in an attempt to reduce the power losses caused by non-ideal gate switching operations. The proposed AGSC employs a dead-time controller (DTC) and a zero-current detector (ZCD) to turn on and off the synchronous switch respectively. Both the DTC and the ZCD perform self-calibration according to the converter switching node voltage, allowing the AGSC achieves near-optimal gate switching control regardless of the operating frequency, process variation, power device variation, as well as source voltage and load current variation.

The proposed AGSC can have useful applications in many DCM DC-DC converters, e.g., buck, boost and buck-boost converters. For proof of concept, in the current work, a boost converter was implemented with the proposed AGSC in a 0.18 μm 3.3V CMOS process with an area of 1.5mm². The experimental results demonstrate precise control of the gate switching operations, and the boost converter at 1.2V/2.5V nominal input/output achieves a peak efficiency of 86% at 30mA load current.

Index Terms—Adaptive gate switching control, DC-DC converter, dead-time controller, discontinuous-conduction mode, zero-current detector.

I. INTRODUCTION

To reduce the size of the power management unit (PMU) in portable devices, the discontinuous-conduction mode (DCM) operation is preferred because it allows the use of small inductors. As the conversion efficiency under DCM is normally lower than that can be achieved in continuous-conduction mode (CCM) [1], synchronous design is widely adopted in low voltage switching converters due to its lower conduction loss with the synchronous switch as compared to the diode rectifier. Despite the low power consumption, the synchronous design is usually difficult to be realized in DCM due to the possible inductor reverse current under non-ideal gate switching operations. Therefore, it is desirable to develop a precise gate switching controller (GSC).

An ideal GSC should be able to eliminate the shoot-through current, the power transistor body-diode conduction current, and the inductor reverse current. In both CCM and DCM operations, the shoot-through current may be induced during the turning-on transition of the synchronous switch (M_P in Fig. 1(a)). To avoid this, a dead-time controller (DTC) [2-8] is normally employed to hold the turning on of M_P , until the control switch M_N is fully turned off. In practice, the M_P body-diode conduction is usually resulted if the dead time is provided in excess; thus, proper control of the dead time must be ensured. In DCM operation, the inductor reverse current may occur if M_P is turned off too late. To ensure a one-way inductor current flow, a zero-current detector (ZCD) as illustrated in Fig. 1(b) is required to trigger M_P turning-off transition at the zero crossing point. Accordingly, M_P is also called a synchronous rectifier. Most high-efficiency converters utilize both the DTC and the ZCD concurrently to minimize power losses. Yet, the DTC is absent in some applications as a slow ZCD can also provide sufficient dead time for M_P .

turning-on transition (Fig. 1(c)) [9]. In either case, the design of the ZCD is critical as its relatively low speed may result in large power losses.

A ZCD can be modified from an on-chip current sensor [3], [10], or realized by a dedicated voltage comparator with its two input terminals crossing the synchronous switch [5], [9], [11-13]. The latter approach normally provides better accuracy. For example, in the CMOS-control rectifier (CCR) in [9], the ZCD is a high speed wide input-range comparator that utilizes a common-gate input pair. It reduces the switching delay of the synchronous rectifier to several 10ns, effectively suppressing the body-diode conduction and inductor reverse conduction. However, with the reduced inductor size in modern high frequency DC-DC converters, a short delay (~10ns) can still lead to a significant inductor reverse current (several 10mA) [3], [11]. A possible solution is to design the comparator with a small fixed offset [14] to enable an early output to compensate for the response delay of the comparator and the gate driver. Yet, this is impractical as both the offset and the response delay are PVT (process-voltage-temperature) dependent.

In the current work, an adaptive gate switching controller (AGSC) is proposed, which consists of a DTC and a dedicated ZCD utilizing a special comparator designed with a tunable unbalanced input pair. The proposed DTC and ZCD perform self-calibration according to the converter switching node voltage [15], and therefore ensuring precise gate switching regardless of the operating frequency, process variation, power device variation, as well as source voltage and load current variation.

For proof of concept, a monolithic boost DC-DC converter with the proposed AGSC is implemented and tested. The design and measurement details are presented in this paper in the following organization. Section II discusses some general characteristics of the boost converter operating in DCM. By utilizing these characteristics, an adaptive gate switching control method is

proposed. Section III presents the circuit implementation of the proposed AGSC in a boost converter, with the measurement results presented in Section IV. Finally, the conclusions will be drawn in section V.

II. CHARACTERISTICS OF DCM OPERATION AND THEIR UTILIZATION ON GATE SWITCHING CONTROL

In order to design an AGSC to improve the efficiency of a DCM boost converter, the characteristics of ideal and non-ideal gate switching operations and their corresponding effects on power losses have to be investigated.

The boost converter shown in Fig. 1(a) is used for analysing the characteristics of the switching transitions. The converter input and output voltages are denoted as V_{IN} and V_{OUT} . Capacitor C_X is the sum of all parasitic capacitance associated with the switching node, whose voltage is denoted as V_X .

A. Characteristics of DCM Boost Converter

A switching cycle of the DCM boost converter shown in Fig. 1(a) starts when M_N turns on to ramp up the inductor current I_L . Upon turning off of M_N , the inductor current will continue to flow through the body diode of M_P for a short dead-time period. After this period, M_P channel conducts and the switching node voltage can be expressed as

$$V_X = V_{OUT} + I_L \cdot r_{on(MP)}, \quad (1)$$

where $r_{on(MP)}$ is the transistor channel resistance. Voltage V_X will decrease as the inductor current I_L drops. Ideally, once the current reduces to zero, V_X will be equal to V_{OUT} , and M_P will be turned off by the output of the ZCD. Both power switches will remain off until the next cycle, and the ringing characteristics of DCM operation can be observed at V_X . The waveform pattern of V_X is a critical performance indicator of the power switches, which is closely associated with the

converter's efficiency. Assuming M_N is always turned on and off according to the pulse-width-modulation (PWM) duty signal, the switching performance of the boost converter is thus dependent on the on/off control of M_P and can be categorized into several cases based on the waveform patterns of V_X as illustrated in Fig. 2.

1) *Ideal switching*: In the ideal case as shown in Fig. 2 (a), after M_N is turned off, M_P should be turned on exactly at the time when the voltage across it becomes zero, and it should be turned off exactly at the time when the current flowing through it drops to zero [6]. When M_P is turned off at zero current, V_X is equal to V_{OUT} . Therefore, if the energy loss in the inductor equivalent series resistance (ESR) is ignored, V_X will ring between V_{OUT} (peak) and $2V_{IN} - V_{OUT}$ (trough) until the start of the next cycle.

2) *M_P is turned on **too early***: Under this condition, there will be a moment when both of the power switches conduct, hence shorting V_{OUT} to ground and introducing a surge current. This current will deteriorate the output regulation, inducing severe power loss, which may cause damage to the switches. Therefore, this is considered as a forbidden condition. The corresponding waveform is not included in Fig. 2.

3) *M_P is turned on **too late***: To prevent the previous condition, a sufficient dead-time period is normally introduced between turning off M_N and turning on M_P , as shown in Fig. 2 (b). The dead time can be generated mainly by two types of circuits: a dedicated DTC [6], [15-22], or a CCR with a certain response delay [9]. In practice, the non-negligible gate driver delay will also contribute to the dead time.

During the excess dead-time period (t_{dt}), current flows through the body diode of M_P , thus increasing the power loss due to the high voltage drop as highlighted in Fig. 2(b). The body-diode conduction loss can be approximated as:

$$\begin{aligned} P_{loss,dt} &= V_{diode} \cdot I_{diode} \cdot t_{dt} \cdot f_{sw} \\ &\approx 0.7V \cdot I_{L(max)} \cdot t_{dt} \cdot f_{sw} \end{aligned} \quad (2)$$

For the sake of simplicity, we assume that the body diode voltage drop V_{diode} is 0.7V in this paper. Parameters I_{diode} , $I_{L(max)}$ and f_{sw} represent the M_P body-diode current, the inductor peak current and the converter switching frequency respectively. Based on (2), the body-diode conduction loss is proportional to t_{dt} predefined in the controller circuit.

4) M_P is turned off *too late*: As mentioned earlier, for a synchronous DCM converter, a ZCD is normally required to turn off the synchronous switch when the inductor current drops to zero. However, due to the delay of the ZCD and the gate driver, a reverse current may be induced in the inductor at the time when M_P is turned off as illustrated in Fig. 2(c). The peak value of the reverse current increases with longer delay time, and thus results in more power losses. This current will pull V_X down to $2V_{IN} - V_{OUT} - V_{DIF}$ (trough), where V_{DIF} is the voltage difference from the trough in the ideal condition and is dependent on the peak value of the reverse current. The reverse current is conducted by the body diode of M_N after M_P is turned off. As shown in Fig. 2(c), we define this phenomenon as “ V_X -Undershoot”. Once this happens, V_X will ring between $2V_{IN} - V_{OUT} - V_{DIF}$ (trough) and $V_{OUT} + V_{DIF}$ (peak). The trough/peak value is clamped at 0.7V below ground/above V_{OUT} by the body diode of M_N/M_P .

5) M_P is turned off *too early*: To reduce the power loss due to the inductor reverse current mentioned previously, an input offset can be predefined in the comparator of a ZCD, to compensate for the delay of the ZCD and the gate driver. However, if over compensation occurs, “ V_X -Overshoot” will appear as shown in Fig. 2(d). After M_P is turned off, the remaining inductor current flows through M_P body diode, and thus induces extra power loss. For the remaining cycle after “ V_X -Overshoot”, voltage V_X will ring between $V_{OUT} + 0.7V$ (peak) and $2V_{IN} - V_{OUT} - 0.7V$ (trough), where the trough is clamped at $-0.7V$ by the M_N body diode.

For the sake of clarification, the term “ V_X -Undershoot”/“ V_X -Overshoot” in this paper only refers to the first body-diode conduction of M_N/M_P when M_P is turned off *too late/early* as in

Fig. 2(c)/ Fig. 2(d). The body-diode conduction of M_P when it is turned on too late (Fig. 2(b)) will be referred to as “excess dead time”.

B. Proposed Adaptive Gate Switching Control Technique by Utilizing the DCM Characteristics

As discussed previously, all the non-ideal switching operations result in extra power losses. To improve the efficiency, the adaptive gate switching control technique is proposed in this paper, whereby the switching operations will be adjusted continuously until the ideal switching is achieved. The adjustment is performed according to some of the DCM characteristics discussed previously, e.g., “excess dead time”, “ V_X -Undershoot”, and “ V_X -Overshoot”, which are used as indicators to determine whether the converter is undergoing non-ideal switching. The mechanism of the proposed adaptive control will be discussed in this section.

Fig. 3(a) shows the self-calibration algorithm for the ZCD used in the proposed AGSC. We assume that the ZCD employs a voltage comparator with tunable input offset. The circuit implementation of this comparator will be discussed in the next section. The positive and negative inputs of the comparator are connected to V_{OUT} and V_X respectively, as illustrated in Fig. 1(c).

The algorithm aims to find out an optimum input offset value, which compensates for the sum of all the delays encountered in the converter control loop exactly, thus achieving ideal turning off of the synchronous switch M_P . The switching node voltage V_X is monitored during the rising edge of signal V_P , where V_P is the gate control signal of M_P . If “ V_X -Undershoot”/“ V_X -Overshoot” is detected, the input offset will be reduced/increased in the subsequent cycle to turn off M_P earlier/later. The same process continues until the optimum input offset is finally achieved and maintained.

The above algorithm generates an input offset for the proposed ZCD to turn off M_P properly. Yet, to turn on M_P by the ZCD, a different input offset will be required. Therefore in this work,

the proposed AGSC adopts the architecture in Fig. 1(b), where an additional DTC is employed to generate M_P turning-on signal separately. This again shows that a ZCD designed with a fixed input offset as reported in the literature cannot achieve ideal operations.

The DTC self-calibration algorithm is illustrated in Fig. 3(b). Its control is slightly different from the ZCD because only one performance indicator, i.e. the “excess dead time” as illustrated in Fig. 2(b), is available. Therefore it adopts the perturbation and observation (P & O) method, where the dead time will keep perturbing around its optimum value.

III. CIRCUITS IMPLEMENTATION OF THE PROPOSED AGSC

By applying the self-calibration algorithm, the proposed AGSC is implemented in a boost converter as shown in Fig. 4(a). In this work, V_{IN} is in the range of 0.9 to 1.4V and V_{OUT} is 2.5V. Under proper M_P switching condition, V_X may have a minimum value of -0.7V when it rings between V_{OUT} (peak) and $2V_{IN} - V_{OUT}$ (trough) in DCM. This could be confused with a -0.7V “ V_X -Undershoot” when M_P is turned off too late. To distinguish these two conditions, a resistor R_N with small value is added between M_N body and substrate, which makes “ V_X -Undershoot” slightly lower than -0.7V, e.g. -0.8V. Thus the proposed controller can recognize the -0.7V ideal operation and will only be triggered when V_X drops to -0.8V. This extra R_N will not cause power loss at steady state, and it only requires small silicon area. The reason is that, under normal operations, M_N forward conduction current flows through the transistor channel during the on period and no reverse current occurs during the off period, thus current through R_N is always zero. Under non-ideal switching conditions (as shown in Fig. 2(c), with M_P turning off too late), M_N conducts reversely for a short while. This reverse current is small as compared to the forward conduction current; and furthermore, most of the reverse current will flow through the collector of the parasitic BJT (as compared to the base of the parasitic BJT), which is illustrated in Fig. 4(b). As the BJT base current is small, the on-chip R_N can have a minimal size without exceeding the current density limitation.

The block diagram of the proposed AGSC is shown in Fig. 4(c). The falling edge of the DTC output triggers signal V_P to turn on M_P while the rising edge of the ZCD output triggers signals V_P and V_{FW} to turn off M_P and turn on the freewheeling switch M_{FW} respectively.

A. Circuits Implementation of the proposed ZCD

The circuit implementation for the proposed ZCD is shown in Fig. 5. It has dual input pairs consisting of $M_{11} \sim M_{14}$, enabling the achievement of a very high gain. Transistors M_{11} and M_{12} have the same size, while M_{13} and M_{14} are unbalanced with $(W/L)_{13} < (W/L)_{14}$. The gates of M_{13} and M_{14} are connected through a transistor M_{15} operating in the triode region, which works as a variable resistor, realizing unbalanced V_{GS} voltages for M_{13} and M_{14} to compensate for their size mismatch and the time delay in the converter control loop during the turning off of M_P . M_{15} has a tunable on-resistance ($r_{on(M15)}$) controlled by its gate voltage V_{CTRL} , which is generated by the input-pair unbalance control circuit (IPUCC). The following equations can be derived from the size-unbalanced input pair.

$$\Delta V_{SG} = V_{SG(M13)} - V_{SG(M14)} \approx \sqrt{\frac{2(I_{B11} + I_{B12})}{\mu_p C_{ox}}} \cdot \frac{(W/L)_{M14}}{(W/L)_{M17}} \left(\frac{1}{\sqrt{(W/L)_{M13}}} - \frac{1}{\sqrt{(W/L)_{M14}}} \right) \quad (3)$$

$$V_{DS(M15)} = I_{B11} \cdot r_{on(M15)} \approx \frac{I_{B11}}{\mu_p C_{ox} (W/L)_{M15} (V_{G(M17)} - V_{CTRL} - V_{THP})} \quad (4)$$

$$V_{OS} = V_{DS(M15)} - \Delta V_{SG} \quad (5)$$

where ΔV_{SG} is the Source-Gate voltage mismatch of the input pair, $V_{DS(M15)}$ is the voltage drop across M_{15} , and V_{OS} is the equivalent input offset of the comparator. The transistor parameters μ_p , C_{ox} , V_{THP} , W and L are effective charge-carrier mobility, gate oxide capacitance (per unit area), threshold voltage, channel width and length respectively.

Under a certain V_{CTRL} value, designated as V_{CTRL-0} , the two voltages $V_{DS(M15)}$ and ΔV_{SG} in (5) will cancel each other exactly. Thus the overall input offset V_{OS} becomes zero. However, for system level consideration, a negative overall input offset is desired so as to compensate for the control loop delay, which should be corresponding to an IPUCC output value lower than V_{CTRL-0} .

As shown in Fig. 5(b), the IPUCC employs the overshoot-detector (OSD)/undershoot-detector (USD) to detect “ V_X -Overshoot”/“ V_X -Undershoot”, and then charges/discharges the capacitor C_{CTRL} to adjust the value of V_{CTRL} . In such a way, the ZCD input offset changes, realizing the self-calibration as described in Fig. 3(a). An increased/decreased V_{CTRL} results in a larger/smaller $r_{on(M15)}$, which will postpone/advance the ZCD triggering point in the subsequent cycle. The change of V_{CTRL} can be predicted by equations at different operating conditions, which will be derived as follows.

As illustrated in Fig. 6(a), when turning off M_p by the traditional ZCD, a delay period τ_{loop} is suffered by the converter. This is the overall loop delay, including delays of ZCD and gate driver, and so on. After applying the proposed ZCD, as shown in Fig. 6(b), the ZCD is calibrated to trigger when switching node voltage reduces to $V_{X(trg)}$ with instantaneous inductor current of $I_{L(trg)}$. After triggered, the ZCD needs certain time to generate its output, and this output will be passed to M_p gate driver, where extra time will be consumed to fully turn off M_p . The overall delay is τ_{loop} . The ZCD input offset at the triggering point is

$$V_{OS(trg)} = I_{L(trg)} r_{on(MP)} = \frac{V_{OUT} - V_{IN}}{L} \tau_{loop} r_{on(MP)}, \quad (6)$$

which will also satisfy the general offset equation in (5), thus leading to

$$V_{CTRL} = V_{G(M17)} - V_{THP} - \frac{I_{B11}}{\mu_p C_{ox} (W/L)_{M15} \left[(V_{OUT} - V_{IN} / L) \tau_{loop} r_{on(MP)} + \Delta V_{SG} \right]}, \quad (7)$$

where ΔV_{SG} has its expression in (3). Equation (7) is not recommended to be used in calculating V_{CTRL} , due to the involvement of some process parameters. However, it shows clearly the trend of V_{CTRL} change due to the variations of input/output voltages, inductor value, M_P size (affecting $r_{on(MP)}$), gate driver capability (affecting τ_{loop}) and process parameters.

In each non-ideal switching cycle, V_{CTRL} can either increase or decrease only once; in an ideal switching cycle, it remains unchanged. In each cycle, after ZCD detects the zero crossing point, the freewheeling switch M_{FW} will be turned on to suppress V_X from ringing and to avoid any unnecessary operations in the ZCD. As current flowing through M_{FW} is small, the transistor size of M_{FW} can be small as well. The functionality of the ZCD will not be affected if M_{FW} is removed, but the dynamic power consumption will increase due to the unnecessary comparisons of the ZCD when V_X keeps ringing.

As shown in Fig. 5(b), the ZCD calibration signal V_{CTRL} is generated by a charge pump, thus a capacitor ($C_{CTRL}=4.8\text{pF}$) is added to smooth its variation. This capacitor introduces a dominant pole to make the loop more stable, at the cost of a slower speed, i.e., longer calibration time. According to (7), if converter input/output voltage does not change (all other parameters like inductor value are fixed as well), V_{CTRL} will keep constant, thus speed limitation is not an issue. At such steady state, the proposed ZCD realizes near optimal operations, which is much better than the conventional designs where the inductor reverse current can be as high as several 10mA [3], [11]. But for applications with frequently changed input/output voltage, the advantage of the proposed design may not be so obvious due to its speed limitation.

The working principle of the OSD and USD as shown in Fig. 5(c)(d) can be explained as follows. The output V_{OS} of the OSD is pulled to ground by R_{OSD2} at normal conditions. Once “ V_X -Overshoot” happens, the voltage drop across the body diode of the converter’s synchronous switch will cause a voltage elevation at the source terminal of transistor M_{OSD} , where its gate

voltage is equal to V_{OUT} shifting down by about 0.2V through R_{OSD1} . Thus M_{OSD} will switch on and V_{OS} will rise as a pulse. In contrast, the output of the USD remains high at normal conditions. When “ V_X -Undershoot” occurs, the ringing of V_X has a trough lower than $2V_{IN}-V_{OUT}$. By biasing the gate at $V_{LEVEL}=2V_{IN}-V_{OUT}+V_{THN}$, M_{USD1} will be turned on and this will pull down the output V_{US} .

It is worth noting that the power consumption of the proposed ZCD is very small. In traditional designs, high speed ZCD is desired to reduce the inductor reverse current, where high speed is achieved by using a large DC biasing current. In this design, however, zero inductor reverse current is guaranteed by tuning the ZCD input offset. Therefore, speed is not a critical requirement in the proposed ZCD, and low biasing current is acceptable. In addition, the proposed ZCD provides better accuracy as well. Traditional designs monitor either the current conducting through or the voltage across the synchronous switch, to detect the zero crossing point. Both of the conducting current and the terminal voltage are very small when the inductor current reduces towards zero. However, when the inductor current is charged into or discharged from the small parasitic capacitor C_X after the synchronous switch is turned off, a large voltage ringing will be induced at V_X . By monitoring this large signal V_X , the proposed ZCD is therefore able to detect a much smaller inductor current as compared to traditional designs.

B. Circuits Implementation of the Proposed DTC

The circuit for the proposed DTC is shown in Fig. 7. It aims to achieve zero-voltage turning on for the synchronous switch, by generating an output V_{DTC} with a short delay after M_N control signal V_N . The delay is controlled by the supply voltage (V_{C_DTC}) of the inverter chain. As the inverters operate, V_{C_DTC} reduces and the delay increases. Therefore, the converter’s synchronous switch M_P will gradually turn on later until its body diode conducts during “excess dead time”, as illustrated in Fig. 2(b). The OSD will switch on transistor M_3 under this condition, and this will

charge V_{C_DTC} to a higher value to reduce the delay. Thus, the P & O algorithm as explained in Fig. 3(b) for the proposed DTC can be achieved.

IV. EXPERIMENTAL RESULTS

A boost DC-DC converter with the proposed AGSC has been implemented with Global Foundries 0.18 μ m CMOS technology with an area of 1.5mm². The micrograph of the chip is shown in Fig. 8. The 0.9~1.4V input and 2.5V output boost converter utilizes a 1 μ H off-chip inductor and a 10 μ F off-chip output filtering capacitor. A prototype of the converter controlled by the AGSC chip is also demonstrated in Fig. 9.

The performance evaluation is carried out through a comparison between: 1) the boost converter with the proposed AGSC, and 2) the boost converter with a GSC adopting the same control structure (Fig. 4(c)) as the proposed AGSC, but using the ZCD design as reported in [9]. According to (2), the efficiency improvement due to the proposed DTC directly depends on the dead-time period t_{dt} predefined in the comparison DTC circuit, thus the proposed DTC is applied in both cases for fair comparison. The tested on and off characteristics for the DCM boost converter with the proposed AGSC and comparison GSC are shown in Fig. 10. Due to response delay, the boost converter with the comparison GSC demonstrated a non-negligible inductor reverse current in Fig. 10(b), where the “ V_X -Undershoot” phenomenon was clear. In Fig. 10(a), the converter with AGSC indeed demonstrated better prevention against the inductor reverse current (after the synchronous switch M_P is turned off exactly at zero crossing point, the small inductor reverse current is due to the unequal inductor terminal voltages at the instance when M_P is just turned off), with the corresponding efficiency improved by up to 3.4% (Fig. 11). As a result, a maximum power efficiency of about 88% can be achieved when the boost converter is operating at 800kHz with 1.4V input voltage and 40mA load current as shown in Fig. 12, increasing the potential of utilizing this design in real portable devices for increased power efficiency.

The design specifications and performance comparison is summarized in Table I. It clearly shows the greatly improved accuracy on gate switching operations with the proposed AGSC technique. It is worth pointing out that, the sizes of M_P and M_N are actually optimized for high current CCM operation, which is not included in this paper. The relatively large switch size has caused more switching loss. If power MOSFET segmentation technique [23] was implemented in this work, the conversion efficiency can be further improved.

V. CONCLUSION

An adaptive gate switching control technique for DCM operating DC-DC converters was proposed. By monitoring the converter switching node voltage, the operating condition of the power switches can be estimated and adjusted. Thus, an AGSC, consisting of the self-calibrated DTC and ZCD, was designed. Besides accuracy improvement, self-calibration also reduced the speed requirement on ZCD design, and therefore reduced the power consumption.

A boost converter with the proposed AGSC and integrated power switches was taped out and tested experimentally. Owing to the AGSC, the converter features near-optimal gate switching. Therefore, the conversion efficiency is improved and the switching node voltage ringing is reduced. Because of the self-calibration capability, the proposed AGSC can provide effective and robust control in other applications with different tape-out processes, converter input/output voltages and load currents. It is also suitable for switching converters with different discrete gate drivers and power switches.

The proposed adaptive gate switching control technique can also be applied to buck and buck-boost DCM operating DC-DC converters. The DTC can be further applied in CCM operating converters as well, to determine the dead time on synchronous switch turning-on transitions.

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Fig. 1. Circuit illustrations of (a) a boost converter for investigating the characteristics under DCM operation, (b) a synchronous switch controlled by a ZCD and a DTC and (c) a synchronous switch controlled by only a ZCD.

Fig. 2. Waveform illustrations of different gate switching operations: (a) ideal (b) M_P is turned on too late (c) M_P is turned off too late and (d) M_P is turned off too early.

Fig. 3. Flow diagrams of the proposed adaptive control for (a) ZCD and (b) DTC.

Fig. 4. (a) Implementation of a boost converter with the proposed AGSC, (b) cross section view of the control switch, and (c) block diagram of the proposed AGSC.

Fig. 5. Circuits implementation of the proposed ZCD. (a) the main architecture, (b) the input-pair unbalance control circuit (IPUCC), (c) the overshoot detector (OSD) with its operating waveforms, and (d) the undershoot detector (USD) with its operating waveforms.

Fig. 6. Boost converter operating waveforms with (a) traditional ZCD and (b) proposed ZCD.

Fig. 7. Circuit implementation of the proposed DTC.

Fig. 8. Die photo of the boost converter with the proposed AGSC.

Fig. 9. Prototype of a boost converter with the proposed AGSC.

Fig. 10. Measurement results of the converter switching node voltage V_x and inductor current I_L (a) with the proposed AGSC and (b) with the comparison GSC.

Fig. 11. Efficiency improvement of the boost converter with the proposed AGSC over the boost converter with the comparison GSC ($V_{IN}=1.2V$).

Fig. 12. Power efficiency of the DCM boost converter with the proposed AGSC.

TABLE I
Design Summary and Comparison

Performance comparison:				
	JSSC 08 [9]	TPEL 11 [3]	This work	
Input voltage V_{IN}	0.9V~1.2V	2.7V~4.2V	0.9V~1.4V	
Output voltage V_{OUT}	2.5V	0.9V	2.5V	
Output current I_{OUT} (at peak efficiency)	100mA	55mA	40mA	
Peak efficiency under DCM	87%	~89%	88%	
External inductor L	1 μ H	2.2 μ H	1 μ H	
External capacitor C	4.7 μ F	4.7 μ F	10 μ F	
Frequency f_{sw}	~667kHz	~200kHz	800kHz	
Technology	0.35 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS	
Chip area	~3mm ²	1.4mm ²	~1.5mm ²	
Synchronous switch turn on timing error	~20ns	~0ns	<1ns	
Synchronous switch turn off timing error	~60ns	~100ns	~0ns	
Power MOSFETs implemented in this work:				
Size	M_N	$\frac{18720\mu m}{0.35\mu m}$	M_P	$\frac{44022\mu m}{0.3\mu m}$
Channel resistance	$r_{on(MN)}$	0.1 Ω	$r_{on(MP)}$	0.11 Ω
Bonding wire resistance	$r_{bonding(MN)}$	0.18 Ω	$r_{bonding(MP)}$	0.18 Ω
Total resistance * ¹	$r_{total(MN)}$	0.28 Ω	$r_{total(MP)}$	0.29 Ω
Gate capacitance * ²	$C_{G(MN)}$	407.4pF	$C_{G(MP)}$	715.2pF
* ¹ per bonding wire impedance is 1 Ω /cm and 10nH/cm				
* ² extracted from layout, including bond pads				