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Thermal Simulator of 3D-IC with Modeling of Anisotropic TSV Conductance and Microchannel Entrance Effects

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Abstract— This paper presents a fast and accurate steady state thermal simulator for heatsink and microfluid-cooled 3D-ICs. This model considers the thermal effect of TSVs at fine-granularity by calculating the anisotropic equivalent thermal conductances of a solid grid cell if TSVs are inserted. Entrance effect of microchannels is also investigated for accurate modeling of microfluidic cooling. The proposed thermal simulator is verified against commercial multiphysics solver COMSOL and compared with Hotspot and 3D-ICE. Simulation results shows that for heatsink cooling, the proposed simulator is as accurate as Hotspot but runs much faster at moderate granularity. For microfluidic cooling, our proposed simulator is much more accurate than 3D-ICE in its estimation of steady state temperature and thermal distribution.

I. INTRODUCTION

Leveraging on the existing economies of scale semiconductor processes, 3D Integrated Circuit (3D-IC) has attracted tremendous research interest as being a commercially viable technological innovation to keep up with the pace of growth in the demand for computing power [1]. By expanding the design space into the third dimension, 3D-IC significantly reduces average wire length, wire delay, power consumption and footprint [2–4]. However, stacking of multiple circuit layers makes effective cooling more challenging due to higher power density and larger junction-to-ambient thermal resistance.

Proper thermal management is mandatory to avoid thermal-induced aging, performance degradation and even malfunctioning. Various solutions have been proposed, including the relocation and redistribution of heat sources and heat paths through thermal-aware floorplanning and scheduling [5, 6], exploitation of novel active and passive cooling methods such as microfluidic cooling [7] and thermal through silicon vias (TSVs) [8, 9]. For any of these approaches, an accurate and computationally efficient thermal model is almost always needed to adapt and control the circuit temperature under a given power profile and cooling requirements.

Numerical multiphysics simulators such as ANSYS [10] and COMSOL [11] are general and accurate but their long simulation cycle makes design phase and runtime thermal management inefficient. As a trade-off, analytical models were proposed to provide rough estimations to speed up the simulation. Early tools such as the well-accepted Hotspot [12] simulates both transient and steady state temperature of heatsink-cooled 2D/3D circuits. Results from Hotspot were shown to be accurate for 2D circuits. However, its modeling of 3D architecture was too simplistic. As microfluidic cooling was pro-

posed as a scalable cooling solution with better cooling effect than heatsink cooling for high performance 3D systems, various thermal models [13–16] were subsequently proposed for liquid-cooled structure, among which the latest released model is 3D-ICE [15, 16]. As 3D-ICE ignores the entrance effect [16, 17] and adopts the conventional parameter correlation for macro-scale pipes [18], it tends to under-estimate the liquid-cooling-induced thermal gradient. Owing to its irregularity and profiling difficulty, thermal effects of TSVs in 3D-IC has not been properly investigated in previous thermal models. In practical implementation, TSVs are likely to concentrate in small regions [19] as I/O interfaces. A detailed analysis on the thermal influence of TSV's location and size is thus necessary for an accurate plot of the thermal map of 3D systems.

In this paper, a fast and accurate steady state thermal simulator for TSV-based 3D-IC will be presented. The proposed simulator models both heatsink and microchannel-based cooling as the two major cooling methods found in literature. The anisotropic TSV thermal effects and entrance effect of microchannels are both investigated and incorporated to address the deficiencies of Hotspot and 3D-ICE. Section II describes typical architectures of 3D-IC with either heatsink or microfluidic cooling. In Section III, our proposed thermal model is introduced, with emphasis on the thermal effect of TSV and entrance effect of microchannels. The simulation results are compared and verified in Section IV and the paper is concluded in Section V.

II. TARGET ARCHITECTURE OF 3D-IC

In 3D-IC, multiple layers of circuit are stacked with fast interlayer connections. A circuit layer typically comprises of Back End of Line (BEOL), device and thinned bulk sublayers. Depending on the cooling demand, different cooling methods are applied. The schematics in Fig. 1 show the cross-sectional views of 3D-ICs with heatsink cooling for low power circuits and microfluidic cooling for high performance 3D stacks. For heatsink-cooled 3D circuits, thermal interface material (TIM) is smeared in between circuit layers for better thermal connectivities. The generated heat is then dissipated into ambient through the spreader and heatsink probably with the aid of a fan. For microfluidic-cooled 3D stacks, microchannels are etched at the back of dies before bonding. Those microchannels are assumed to be uniformly distributed with identical channel width and height. The channel walls are thus of the same width except possibly for the walls at the boundaries. Liquid coolant flows through the microchannels and carries away the generated heat. Without loss of generality, it is as-

Fig. 1. Schematic of 3D integrated circuit with Heatsink and microfluidic cooling

sumed that the coolant reservoir is large enough so that the inlet coolant is always at the ambient temperature, keeping in mind that the ambient temperature setting can always be modified to simulate for non-ideal cases where a higher inlet temperature is observed.

III. COMPACT THERMAL MODEL OF 3D-IC

To achieve a balance between accuracy and speed on estimating the steady state temperature of 3D-ICs, finite element approximation is adopted, where the 3D stack under study is divided into regular grid cells according to the user-defined row-column resolution. Thermal conductances between adjacent cells are then calculated by considering the effect of TSVs. At steady state, the thermal balance equation holds for every grid cell as follows.

$$\sum (T_i - T_{i,adj}) * g_{i,adj} = P_i \quad (1)$$

where T_i and $T_{i,adj}$ denote the temperatures of the i^{th} grid cell and its adjacent grid cell, respectively. $g_{i,adj}$ represents the thermal conductance between the two cells, and P_i is the heat generated by the i^{th} grid cell. The matrix equation of thermal equilibrium can be solved by the sparse solver KLU [23] with the provided power consumption.

A. Thermal Conductance between Solid Cells with Anisotropic TSV Effects

In a 3D circuit, thousands of TSVs may co-exist to deliver the power and signal. These TSVs are normally filled with metal which has a higher thermal conductivity than silicon. Previous works on thermal-TSVs [8, 9] suggest that they can have a significant influence on the steady state temperature of 3D-ICs. Such influence is due to the change of thermal conductivity in the heat transfer path when a TSV is inserted and is highly dependent on the TSV's size and position. In this work, all TSVs are assumed to be squarish cross-sectionally to ease the modeling process, with the understanding that round TSVs can always be projected to squarish ones of proper sizes.

For two grid cells without TSV, the thermal conductance between them is formulated as

$$g_{ij} = kA/t \quad (2)$$

where k denotes thermal conductivity, A is the cross-sectional area through which the heat flux passes and t is the length of

the heat transfer path. When a TSV is inserted as shown in Fig. 2(a), the equivalent x , y , and z direction thermal conductances of the grid cell can be computed as:

$$g_x = (1 + \frac{wh(\beta - 1)}{WH(1 + (1 - w/W)(\beta - 1))})g_{x0} \quad (3)$$

$$g_y = (1 + \frac{wh(\beta - 1)}{WH(1 + (1 - h/H)(\beta - 1))})g_{y0} \quad (4)$$

$$g_z = (1 + \frac{wh(\beta - 1)}{WH})g_{z0} \quad (5)$$

where $g_{x0} = \frac{K_{cell}HL}{W}$, $g_{y0} = \frac{K_{cell}WL}{H}$ and $g_{z0} = \frac{K_{cell}WH}{L}$ are the thermal conductances of the grid cell without TSV and L is the depth of the grid cell. $\beta = K_{TSV}/K_{cell}$ is the ratio of the thermal conductivities between TSV and grid cell. Rectangular TSV is considered in general since a TSV may fall on the boundaries of grid cells so that only a part of it is inside the grid cell. This set of equation reveals that thermal conduction improvement due to TSV insertion is anisotropic which is more significant vertically and mitigated laterally. Note that superposition principle is applicable if multiple TSVs are inserted into the same grid cell.

Fig. 2. Geometry of grid cell with TSV

In real implementation, TSVs are normally surrounded by a thin layer of less thermally conductive dielectrical liner for insulation purpose, as shown in Fig. 2(b). To count for the thermal isolation of dielectrics, the equivalent thermal conductivity of TSV with liner is defined as follows.

$$K_{TSV,xy} = (1 + \frac{d_m^2(\gamma - 1)}{(d_m + 2d_l)(d_m + 2d_l\gamma)})K_{liner} \quad (6)$$

$$K_{TSV,z} = (1 + \frac{d_m^2(\gamma - 1)}{(d_m + 2d_l)^2})K_{liner} \quad (7)$$

where d_m is the side length of the metal core, d_l is the liner thickness and $\gamma = K_{metal}/K_{liner}$ is the ratio of the thermal conductivity between metal and liner.

To calculate the thermal conductances between all the solid grid cells with TSV effects, thermal conductances without TSV are first obtained according to (2). The sizes and positions of TSVs are then imported to determine their overlaps with all grid cells. Based on the equivalent thermal conductivity of every TSV, their contributions to thermal conductance are then added up to the overlapped solid grid cells according to (3)-(5). The thermal conductance between two adjacent solid grid cells can then be obtained as half the sum of their thermal conductances.

B. Convective Heat Transfer and Entrance Effect of Microchannels

Convective heat transfer between solid and fluid cells can be characterized by the convective conductance, defined as follows:

$$g_{Conv} = h * A_{conv} \quad (8)$$

where h is the heat transfer coefficient and A_{conv} is the area of interface where convection takes places. In our thermal model, the convective conductances of heatsinks are considered as one of the configuration inputs in accordance to Hotspot [12]. Tabulated values of convective resistances for heatsink can be found from the manufacturer datasheet.

For microfluidic cooling through microchannels, h is calculated as:

$$h = \frac{k_f Nu}{D_H} \quad (9)$$

where k_f is the coolant's thermal conductivity. D_H represents the hydraulic diameter and is given by (10) for rectangular channels.

$$D_H = \frac{4 \cdot A_{Ch}}{P_{Ch}} \quad (10)$$

where A_{Ch} and P_{Ch} denote the channel cross-sectional area and channel perimeter, respectively. The Nusselt number Nu is usually obtained by empirical correlations to Reynolds number Re , Prandtl number Pr and channel dimension in the literature. In our thermal model, the following correlation for microchannels [22] is used.

$$Nu_{PP} = 0.1165 \left(\frac{D_H}{Pitch} \right)^{0.81} \left(\frac{H_{Ch}}{W_{Ch}} \right)^{-0.79} Re^{0.62} Pr^{1/3} \quad (11)$$

where $Pitch$ refers to the center-to-center distance of adjacent microchannels. H_{Ch} and W_{Ch} denotes the height and width of microchannels, respectively.

In addition, it was noted that the heat transfer rate is significantly higher near the inlet of microchannels due to the thin developing thermal boundary layer [16, 17], which was ignored by most of the previous works. To model the influence of such entrance effect, we make the following modification to the conventional macro-scale formulation [17].

$$Nu_{ST} = Nu_0 (Re * Pr)^{1/3} \left(\frac{D_H}{l} \right)^\eta \quad (12)$$

where l denotes the distance from the channel inlet. The original values 1.86 and $1/3$ of the coefficients Nu_0 and η have been revised to 30 and 1.67, respectively by model-fitting against COMSOL [11] for application on microfluids. The aggregated Nusselt number can thus be calculated as

$$Nu = Nu_{PP} + Nu_{ST} \quad (13)$$

C. Steady State Thermal Analysis

At steady state, all the grid cells are under thermal equilibrium and (1) holds. For microfluidic cooling, the channel temperature is also held constant where the heat is transferred from upstream to downstream in the form of massive flow. Thus the

following equation is satisfied by the liquid channel cells under thermal equilibrium.

$$\sum_{j \in \{walls\}} g_{ch,i,j} (T_{ch,i} - T_j) = (T_{ch,i} - T_{ch,i-1}) Q C_V \quad (14)$$

where $T_{ch,i}$ and $T_{ch,i-1}$ indicate the temperatures of the i^{th} channel cell and its upstream cell. Q and C_V are the coolant's flowrate and volumic specific heat, respectively. Based on (1) and (14), a matrix equation can be set up as follows irrespective of the cooling technique.

$$GT = P \quad (15)$$

where T is a column array for the unknown steady state temperature of each grid cell and P is the heat generation column array. G is an $N \times N$ coefficient matrix where N denotes the total number of grid cells. Note that the thermal conductance is zero for two cells that are not in contact physically. Thus G is a sparse matrix with the number of non-zero elements linearly proportional to N . This sparse matrix equation can be efficiently solved by existing sparse solvers such as KLU [23] to obtain the steady state temperatures of every grid cell.

D. Software Implementation

The proposed thermal model has been implemented in C program. The basic program flow is shown in Fig. 3. The thermal

Fig. 3. Program flow chart

model accepts a layer configuration file to set up the physical description of the 3D-IC, including detailed sizing, cooling method, TSV setting, and power consumption, etc. After that, the model calculates the thermal conductances by considering the TSV effects. The G matrix is then built by completing the column pointer array, row index array and numerical value array required by KLU. Finally, the P array is created and the steady state temperature is obtained by solving (15). In our program, the time spent on thermal conductance calculation is linearly dependent on the number of TSVs, which is an integer constant of limited value for a given circuit. The construction of G and P both have a time complexity of $O(m)$, where m denotes the number of non-zero entries of the matrix. The KLU algorithm has a time complexity of $O(N + m)$, where N is the total number of grid cells. Since m is linearly proportional

to N , our proposed thermal model has a time complexity of $O(N)$, which scales linearly with the total number of grid cells. Our proposed thermal model are available for downloading via [24].

IV. VERIFICATION, COMPARISON AND DISCUSSION OF EXPERIMENT RESULTS

In this section, we verify the accuracy of the proposed thermal simulator and compare our results with existing works. For both cooling methods, a two-layer 3D stack is used for the test. The chip is set to a size of $1.8 \times 1.8 \text{ mm}^2$ with $12 \mu\text{m}$ BEOL layers and $2 \mu\text{m}$ device layers. The thickness of bulk layer is $48 \mu\text{m}$ for the top tier and $148 \mu\text{m}$ for the bottom tier. Ambient temperature is assumed to be 300 K . The details of cooling package setup is listed in Table I. In the absence of physical

TABLE I
EXPERIMENT SETTINGS

Heatsink Cooling Setting	
TIM thickness	$20 \mu\text{m}$
TIM thermal conductivity	$4 \text{ W}/(\text{mK})$
Spreader Size (mm)	$30 \times 30 \times 1$
Spreader thermal conductivity	$400 \text{ W}/(\text{mK})$
Heatsink Size (mm)	$60 \times 60 \times 6.9$
Heatsink thermal conductivity	$400 \text{ W}/(\text{mK})$
Heatsink Convective conductivity	$10 \text{ W}/\text{K}$
Microfluidic Cooling Setting	
Microchannel Size (μm)	100×100
Channel Wall Width	$100 \mu\text{m}$
Default Flowrate	$9 \text{ ml}/\text{min}$
Coolant Type	Deionized Water

prototypes, our thermal simulator is validated against the accurate commercial multiphysics solver COMSOL [11]. A simple 3×3 mosaic floorplan is adopted for the two circuit layers with customizable power densities. All the experiments are performed on a Linux server with Intel Xeon 3.47 GHz processor and 50 GB of memory.

A. Heatsink-Cooled 3D-IC

For heatsink-cooled 3D-IC, we compare our results with COMSOL and Hotspot 5.0. A set of uniform power density (PD) at typical magnitude is assigned to the device layers of 3D-IC. The maximum and minimum steady state temperatures from the three simulators are reported in Table II, where power density is measured in W/cm^2 .

In this experiment, a 16×16 grid division on each layer is used for Hotspot and our simulator. The mesh in COMSOL is set at the finest granularity to produce the most accurate result. Both our model and Hotspot adopted the same equation (2) to calculate the thermal conductances between solid cells, which results in the same thermal circuit for heatsink-cooled 3D-ICs. Thus, it is not surprising that our thermal simulator and Hotspot produce almost identical results although different solvers are adopted. Compared with COMSOL, the deviation of our thermal simulator is in the range of $0.2 - 1.2\%$ due to

TABLE II
STEADY STATE TEMPERATURE (K) COMPARISON AMONG COMSOL, HOTSPOT AND PROPOSED SIMULATOR

PD		COMSOL	Hotspot	Ours	Error
50	Max	313.72	312.83	312.83	0.3%
	Min	308.16	307.41	307.40	0.2%
100	Max	327.45	325.66	325.66	0.5%
	Min	316.33	314.81	314.81	0.5%
150	Max	341.17	338.49	338.49	0.8%
	Min	324.49	322.22	322.22	0.7%
200	Max	354.90	351.32	351.32	1.0%
	Min	332.66	329.62	329.62	0.9%
250	Max	368.62	364.15	364.15	1.2%
	Min	340.82	337.03	337.02	1.1%

TABLE III
RUNTIME COMPARISON AMONG COMSOL, HOTSPOT AND PROPOSED SIMULATOR

Model\PD	50	100	150	200	250
COMSOL	42	42	42	42	42
Hotspot	0.763	1.019	1.187	1.31	1.41
Ours	0.068	0.068	0.059	0.061	0.066
Speedup	11x	15x	20x	21x	21x

coarser vertical granularity which was set as the total number of sublayers. Finer vertical granularity is possible by further dividing the sublayers. However, the tradeoff between accuracy and runtime shall be considered to determine a suitable grid resolution. The deviation of temperature results increases monotonically with the increase of heat flux, because increasing the heat flux amplifies the differences in thermal circuits.

Table III lists the runtime of the three simulators in *seconds* for this experiment set. Only the speedup against Hotspot is reported in this table because it is unfair to compare the speedup against COMSOL, which has a larger problem size due to much finer granularity. Up to $21\times$ speedup is achieved for this test case. As the recursive multigrid approach by Hotspot scales logarithmically with the problem size, it will have a shorter runtime when the grid dimension is large. Fig. 4 depicts the runtime scaling of both simulators at a moderate power density of $150 \text{ W}/\text{cm}^2$. The five problem sizes correspond to 8×8 , 16×16 , 32×32 , 64×64 and 128×128 lateral grid dimensions respectively, with vertical grid resolution equal to the total number of sublayers which is 16. It can be seen that hotspot performs better after the forth point. However, the grid dimension in Hotspot is restricted to powers of two to compromise for the convenience of its recursive solving method, while our model has no restriction on the grid dimension which is important for modeling microfluid-cooled 3D-ICs.

We then examine the accuracy of TSV modeling by inserting three different patterns (Fig. 5) of TSVs into the circuit. For convenience, all TSVs in COMSOL are assumed to have identical size, and punch through the substrate of the top tier to the device layer of the bottom tier. Si_3N_4 is assumed to be the liner material and copper is used as the filling metal. Ta-

Fig. 4. Runtime Scaling of Our Thermal Simulator and Hotspot

Fig. 5. The three TSV test patterns

ble IV lists the reduction of maximum temperatures compared with the baseline without TSVs. It shows the estimation error varies with different TSV patterns, where the largest deviation appears on Pattern A. Consider the base temperature of 300K, our TSV thermal model is accurate with the largest deviation of only 0.57K.

B. 3D-ICs with Microfluidic Cooling by Microchannels

To verify the accuracy of the proposed thermal model on microfluidic cooling, we compare the simulation results with COMSOL and 3D-ICE 2.1. The same 2-layer 3D circuit is used except that it is cooled by the microfluidic channels between two circuit layers instead of heatsink. The same set of typical power densities is applied to the device layers. The maximum and minimum temperatures for the top device layer is reported

TABLE IV
REDUCTION OF MAXIMUM TEMPERATURE DUE TO TSV INSERTION

Pattern\PD		50	100	150	200	250
A	COMSOL	0.20	0.40	0.60	0.80	1.00
	Ours	0.31	0.63	0.94	1.26	1.57
	Error	0.11	0.23	0.34	0.46	0.57
B	COMSOL	0.14	0.29	0.44	0.59	0.73
	Ours	0.18	0.36	0.53	0.71	0.89
	Error	0.04	0.07	0.09	0.12	0.16
C	COMSOL	0.12	0.24	0.36	0.48	0.60
	Ours	0.16	0.31	0.47	0.63	0.78
	Error	0.04	0.07	0.11	0.15	0.18

in Table V with their corresponding percentage errors enclosed in brackets. It shows that our proposed thermal model is very accurate with a percentage error of less than 1.1% for this test case. In contrast, 3D-ICE exhibits large errors especially for the minimum temperatures due to the ignorance of entrance effect, which causes the thermal gradient to be severely underestimated. Fig. 6 shows the temperature maps of the top device layer at a power density of $150W/cm^2$ plotted based on the results of three simulators. It can be seen that the temperature distribution of our thermal model agrees very well with COMSOL while that of 3D-ICE deviates significantly.

TABLE V
STEADY STATE TEMPERATURE (K) COMPARISON AMONG COMSOL, 3D-ICE AND PROPOSED SIMULATOR

PD		COMSOL	3D-ICE	Ours
50	Max	314.3	317.4(1.0%)	314.0(0.1%)
	Min	301.7	314.2(4.1%)	302.4(0.2%)
100	Max	328.6	334.8(1.9%)	328.0(0.2%)
	Min	303.4	328.4(8.2%)	304.8(0.5%)
150	Max	342.9	352.2(2.7%)	341.9(0.3%)
	Min	305.2	342.6(12.3%)	307.2(0.7%)
200	Max	357.2	369.6(3.5%)	355.8(0.4%)
	Min	306.9	356.8(16.3%)	309.6(0.9%)
250	Max	371.5	387.0(4.3%)	369.8(0.5%)
	Min	308.6	371.0(20.2%)	312.0(1.1%)

Fig. 6. Comparison of estimated thermal distribution of top device layer

Due to the predominant heat extraction through microchannels, the thermal effect of TSV is less pronounced compared with that in heatsink-cooled 3D-ICs. For example, a reduction in maximum temperature of merely 0.28K is reported by our thermal model for the test bench at a power density of $250W/cm^2$ with TSV pattern C.

V. CONCLUSION

In this paper, an accurate steady state thermal simulator has been presented for both heatsink-cooled and microfluidic-cooled 3D-ICs. This model is capable of estimating the thermal effect of TSVs in fine-granularity and computationally efficient. It also considers entrance effect of microchannels based on the most appropriate thermodynamics for microfluidic cooling. The simulation results of the test cases from the proposed model are in good concordance with those obtained from commercial software COMSOL, with a maximum error of 1.2% for heatsink cooling and a maximum error of 1.1% for microfluidic

cooling. Comparing with Hotspot for heatsink cooling at moderate grid dimension, our thermal model generated identically accurate results in a much shorter runtime. Comparing with 3D-ICE for microfluidic cooling, our thermal model is more accurate in the estimations of temperature and temperature distributions. The results obtained from our thermal model also conclude that the thermal effect due to TSV has been marginalized under microfluidic cooling.

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