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High Frequency Drain Current Noise Modeling in MOSFETs under Sub-Threshold Condition

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Abstract— A new high frequency drain current noise model was developed for MOSFETs under sub-threshold condition. A simple parameter extraction technique is proposed, which utilizes Y-parameter analysis on the RF small-signal equivalent circuit. Good agreement has been obtained between the predicted and measured results up to 20 GHz.

Index Terms—De-embedding, High frequency noise, MOSFET, Noise modeling, RFCMOS noise, RF MOS transistor noise, Sub-threshold noise, Weak inversion noise

I. INTRODUCTION

In new and upcoming wireless applications, such as distributed micro-sensors or medical applications, minimizing power consumption is the primary concern and has motivated investigation of the optimum design for minimizing energy dissipation for a given performance constraint. Sub-threshold circuits are ideal for this class of applications. To make the sub-threshold circuits a realistic solution, accurate models predicting the HF noise characteristics of the short-channel CMOS in sub-threshold region are of paramount importance.

In the strong inversion regime, flicker noise is dominant at low frequency. Flicker noise occurs in MOS devices due to interface traps. The chief characteristic of flicker noise is its $1/f$ spectrum. Hence at RF frequencies, the MOSFET flicker noise becomes negligible and thermal noise is the dominant source of noise. Thermal noise is caused by the random thermal motion of the current carriers in the device. In MOSFET, thermal noise is generated at channel region and its parasitic resistances. The mentioned noise contributes to the drain current noise. At high frequency, the channel thermal noise is coupled to the gate causing induced gate noise. The channel thermal noise in short-channel MOSFET has been studied in detail experimentally and theoretically [1,2].

In the weak inversion regime, the channel thermal noise is derived to correspond to shot noise of drain current [1, 3, 4].

The shot noise is generated when the current flows across the p-n junction potential barrier in the source-bulk junction. The conventional shot noise is defined by

$$S_{i_d} = 2qI_D \quad (1)$$

where I_D is the DC drain current.

However, in a few publications [5, 6], the drain current noise behavior has been reported to deviate from classical shot noise model at RF frequencies. The high frequency drain current noise is found to be independent of gate bias and dependent of frequency in the sub-threshold region. In [6], the van der Ziel's high frequency shot noise model in p-n+ diode [1] has been extended to model the high frequency shot noise generated in the source-bulk junction [6]. However, the AC conductance model used in [6] is not valid.

In this paper, a model that is capable of predicting the drain current noise of short channel MOSFETs in sub-threshold region is presented. Such model is explained in detail in Section III. The measurement setup and the extraction for drain current noise intensity are discussed in Section II. In Section IV, the model parameter extraction methodology is presented. The model is verified in Section V.

II. MEASUREMENT

The device under test (DUT) is NMOS transistors with channel width per finger $W' = 5\mu\text{m}$, channel length $L = 0.13\mu\text{m}, 0.25\mu\text{m}, 0.5\mu\text{m}$ and $1\mu\text{m}$, and the number of fingers $N_F = 4$. They were fabricated using Chartered Semiconductor Manufacturing Ltd's $0.13\mu\text{m}$ RFCMOS technology process. HP8510 network analyzer and ATN NP5B Microwave Noise Parameter System were used to measure the on-wafer scattering and noise parameters for a frequency range of 5GHz to 20GHz. The noise parameters measured include the minimum noise figure, NF_{min} , equivalent noise resistance, R_n and optimum reflection coefficient, Γ_{opt} . System calibration was performed using LRRM method before the RF transistor and its de-embedding “open” structures were measured.

After measuring the scattering and noise parameters of the transistors, the measurement data were de-embedded to minimize the error due to the pad and interconnect parasitic effect. The power spectral density of the channel thermal noise S_{i_d} was extracted from the de-embedded noise parameters.

A. Y-parameter De-embedding

First, a two-step de-embedding procedure [7] is performed to remove the parallel elements introduced by the pads that are

determined from the additional “open” structures.

$$[Y_{DUT-OPEN}] = [Y_{DUT}] - [Y_{OPEN}] \quad (2)$$

Y_{DUT} are the Y-parameters of the measured DUT and Y_{OPEN} are the Y-parameters of the “open” structures.

The intrinsic transistor is still embedded by the series resistors such as R_g , R_d , and R_s due to the interconnection lines. The series parasitic parameters can be determined through cold modeling of the device. The device is measured at different gate voltages above threshold voltage, zero drain voltage and at high frequency. The gate resistance R_g can be obtained by using a linear regression method to find the y-intercept of $\Re(Z_{11} - Z_{12})$ against $1/(V_G - V_T)$ at an infinite gate voltage V_G . Similarly, the source resistance R_s can be extracted from the y-intercept of $\Re(Z_{12})$ against $1/(V_G - V_T)$. The same extraction method was used to obtain the drain resistance R_d from the y-intercept of $\Re(Z_{22} - Z_{12})$ against $1/(V_G - V_T)$. The series inductances are negligible compared to the extrinsic capacitive effect of the device in weak inversion.

The de-embedding matrix for the series elements is formulated as follows:

$$[Z_s] = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \quad (3)$$

The intrinsic Y-parameters can be obtained as follows:

$$[Y_i] = [[Y_{DUT-OPEN}]]^{-1} - [Z_s]^{-1} \quad (4)$$

Y_i represent the intrinsic Y-parameters of the device.

B. Noise De-embedding

Based on the same DUT and de-embedding structure used in Y-parameter de-embedding, the Chen’s noise de-embedding method is performed to remove the parallel coupling parasitic noise [7].

$$[C_Y^{DUT-OPEN}] = [C_Y^{DUT}] - [C_Y^{OPEN}] \quad (5)$$

C_Y^{DUT} is the admittance correlation matrix of the DUT and C_Y^{OPEN} is the admittance correlation matrix of the “open” structures. $C_Y^{DUT-OPEN}$ is the noise correlation matrix de-embedded from the parallel coupling effect. $C_Y^{DUT-OPEN}$ is then transformed to its $C_Z^{DUT-OPEN}$ correlation matrix such that the series de-embedding can be performed to remove the series parasitic noise.

$$[C_Z^S] = [C_Z^{DUT-OPEN}] - [C_Z^S] \quad (6)$$

where C_Z^S is the correlation matrix of the series parasitic.

$$[C_Z^S] = 2kT\Re([Z_S]) \quad (7)$$

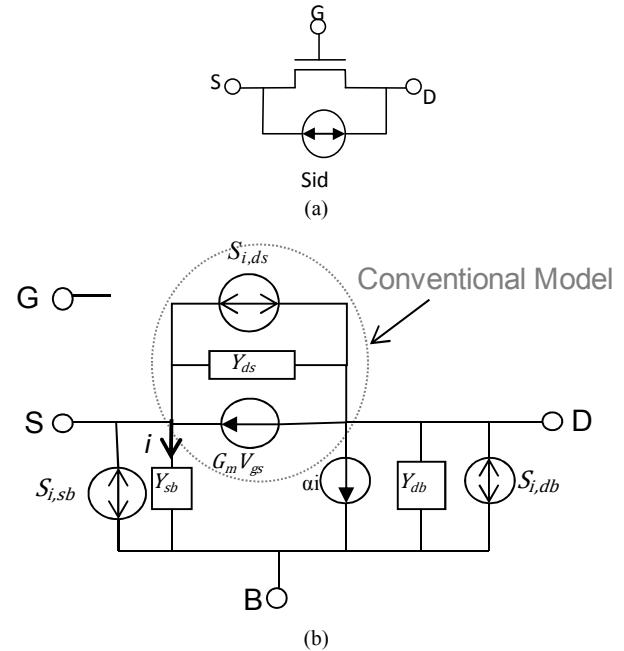


Figure 1. (a) Drain current noise in MOSFET is modeled as an equivalent single noise source connected from source to drain. (b) The equivalent drain current noise in MOSFET in weak inversion region is modeled by adding the source-bulk junction noise source and the drain-bulk junction noise source to the conventional shot noise model.

C_Z^I is the intrinsic noise correlation matrix that can be converted to its C_Y to obtain the de-embedded noise parameter such as NF_{min} , R_n , and Γ_{opt} [10]. The power spectral density of the drain current noise S_{id} can be extracted with

$$S_{id} = 2C_{22Y}. \quad (8)$$

III. DRAIN CURRENT NOISE MODEL IN MOSFET

In MOSFETs, the source-bulk junction and the drain-bulk junction can be viewed as a p-n⁺ junction. When the current carriers, which are electrons, cross the junction potential barrier, shot noise is generated. The high frequency shot noise spectral density is expressed as [1]

$$S_i(f) = 2q(I + 2I_o) + 4kT[g(f) - g_0], \quad (9)$$

where I is the DC current flow into the junction, I_o is the saturation current, $g(f)$ is the junction AC conductance and g_0 is the junction DC conductance.

A new drain current noise model in MOSFET under sub-threshold bias condition is proposed to include the noise generated in the source-bulk junction and drain-bulk junction, as shown in Figure 1(b). The overall drain current noise is modeled with an equivalent single noise source, shown in Figure 1(a), with the noise equation derived from Figure 1(b) as follows:

$$S_{id} = S_{i,ds} + \alpha^2 S_{i,sb} + S_{i,db} \quad (10)$$

where $S_{i,ds}$ is the conventional drain current noise spectral density given by

$$S_{i,ds} = 2qI'_{DS}(1 + e^{-V_{DS}/\phi_t}), \quad (11)$$

with I'_{DS} is the saturation drain current in MOSFET and ϕ_t is the thermal voltage kT/q . For $V_{DS} > 5\phi_t$, $S_{i,ds}$ can be approximated to

$$S_{i,ds} \approx 2qI'_{DS}. \quad (12)$$

$S_{i,sb}$ and $S_{i,db}$ represent the noise generated in the source-bulk junction and the drain-bulk junction, given by equation (13) and (14).

$$S_{i,sb} = 4kTg_{sb} = 4kT\Re(Y_{sb}) \quad (13)$$

$$S_{i,db} = 4kTg_{db} = 4kT\Re(Y_{db}) \quad (14)$$

α is the small signal current gain for common-base NPN transistor, which can be derived as follows:

$$\alpha^2 = \frac{|Y_{mb} - Y_{bs}|^2}{|Y_{sb}|^2} \quad (15)$$

$$\alpha^2 = \frac{(g_{mb} + g_{j,bs})^2 + \omega^2(C_{db} - C_{bd} + C_{bs})^2}{(g_{mb} + g_{j,bs})^2 + \omega^2C_{sb}^2} \quad (16)$$

In sub-threshold region, intrinsic capacitances are small compared to the extrinsic capacitances. Therefore, if the transistor is built with symmetry structures for source and drain, $C_{bd} \approx C_{bs}$ and $C_{db} \approx C_{sb}$, the small signal current gain α will be close to unity. Thus, the drain current noise in the transistor operated in sub-threshold condition is expressed as

$$S_{i_d}(f) \approx 2qI_D + 8kTg_{db}(f). \quad (17)$$

IV. EXTRACTION OF MODEL PARAMETER

The drain-bulk junction can be approximated as a resistor R_{db} in series with a capacitor C_{db} , and thus the drain-bulk junction conductance is given by

$$g_{db} = \frac{\omega^2 C_{db}^2 R_{db}}{1 + \omega^2 C_{db}^2 R_{db}^2}. \quad (18)$$

By performing Y-parameter analysis on the circuit in Figure 2, the drain-bulk junction admittance is obtained as follows:

$$\Re(Y_{22} + Y_{12}) = g_{ds} + g_{db} \quad (19)$$

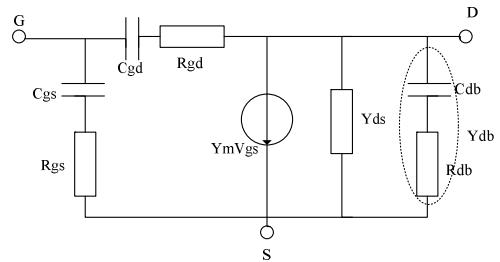


Figure 2 Small-signal equivalent circuit represents the intrinsic device. Drain-bulk junction is modeled as a resistor in series with a capacitor.

In weak inversion region, $g_{ds} \ll g_{db}$. Hence, by plotting $\omega^2/\Re(Y_{22} + Y_{12})$ against ω^2 , the resistance R_{db} can be extracted from the slope of the plot by using the linear regression method. The capacitance C_{db} can then be obtained as follows:

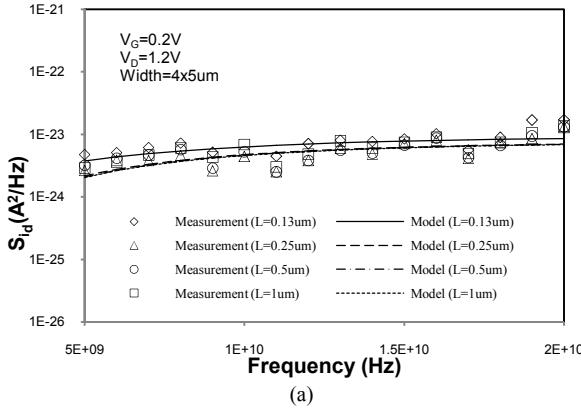
$$C_{db} = \left(\frac{\omega^2 R_{db}}{\Re(Y_{22} + Y_{12})} - \omega^2 R_{db}^2 \right)^{-1/2} \quad (20)$$

V. RESULTS AND DISCUSSIONS

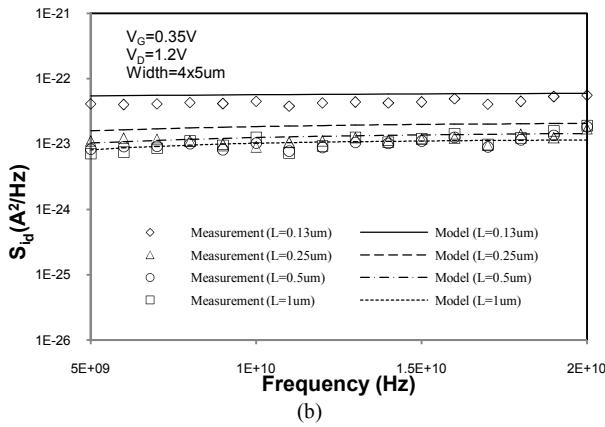
The drain current noise in n-MOSFETs in the sub-threshold regime can be predicted from the drain current noise model presented in section III. Figures 3 and 4 show the comparison between the calculated drain current noise spectral density and the extracted drain current noise from the noise measurement data for drain voltage of 1.2V and varying channel length of $L = 0.13, 0.25, 0.5$ and $1.0\mu\text{m}$, and their threshold voltages are around 0.30V. The predicted noise spectral density in the n-MOSFET show good agreement with the noise measurement data.

The drain current noise in the moderate inversion region is almost constant with frequency, as shown in Figure 3(b). The conventional noise model in (1) predicts that the drain current noise depends only on DC current driving the transistor and thus the noise is independent of frequency. This conventional noise model is able to predict the noise in moderate inversion region. However, at RF frequencies, the drain current noise in the sub-threshold shows decent frequency dependency in Figure 3(a). In the sub-threshold region, the additional noise generated in the source-bulk and drain-bulk junction is frequency dependent, and thus can be enhanced by increasing the frequency.

Figure 4 indicates that the drain current noise in the sub-threshold region is independent of gate bias and channel length. At high frequency, the noise generated by the AC conductance of source-bulk and drain-bulk region dominates the drain current noise and the contribution of channel noise becomes negligible. Therefore, the drain current noise is independent of channel conditions such as channel length, gate bias so as the carrier density. Instead, the amplitude of RF drain current noise in sub-threshold region is determined by the conditions of the source-bulk junction and drain-bulk junction.



(a)



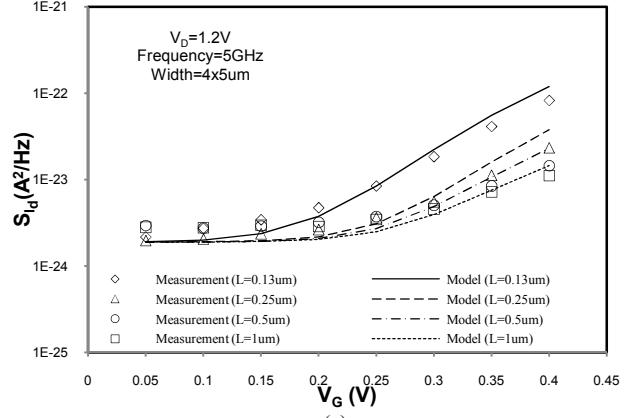
(b)

Figure 3 Comparison between sub-threshold drain current noise model with measured data against frequency for different L at $V_D=1.2V$. In (a) the transistors are biased at $V_G=0.2V$ in weak inversion region. In (b), the transistors are biased at $V_G=0.35V$ in moderate inversion region.

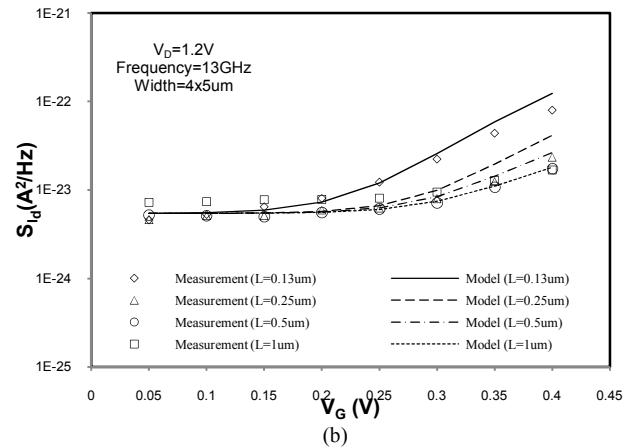
VI. CONCLUSION

The RF drain current noise model in sub-threshold region is presented. The predicted noise shows good agreement with noise measurement data. The drain current noise spectrum in MOSFET was estimated by using the DC drain current model and the AC drain-bulk conductance model with the model parameters extracted from the Y-parameters measurement.

In sub-threshold region, noise is generated when the current carriers cross over the potential barrier of source-bulk junction and drain-bulk junction. At high frequency, the drain current noise is much larger than the classical shot noise. While the classical shot noise model expect that with the decrease of gate voltage, the noise will reduce exponentially, the high frequency drain current noise stays unchanged once the gate voltage goes below the threshold voltage. In fact, at the RF frequencies, the drain current noise in the sub-threshold region is dominated by the thermal noise due to the ac conductance of the source-bulk junction and drain-bulk junction. Hence, the intensity of the drain current noise is determined only by the conditions of source-bulk junction and drain-bulk junction and will be almost independent of the channel conditions such as channel length and gate bias conditions.



(a)



(b)

Figure 4 Comparison between sub-threshold drain current noise model with measured data against gate bias for different L at frequency of 5GHz in (a) and 13GHz in (b). Both are biased at $V_D=1.2V$. The same trend can be observed in both frequencies.

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