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High Accuracy Time-Mode Duty-Cycle-Modulation-Based Temperature Sensor for Energy Efficient System Applications

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Abstract This paper presents a new time-mode duty-cycle-modulation-based high accuracy temperature sensor. Different from the well-known $\Sigma\Delta$ ADC based read-out structure, this temperature sensor utilizes a temperature-dependent oscillator to convert the temperature information into temperature related time-mode parameter values. The useful output information of the oscillator is the duty-cycle, not the absolute frequency. In this way, this time-mode duty-cycle-modulation-based temperature sensor has superior performance over the conventional inverter-chain based time domain types. With a linear formula, the duty cycle output streams can be converted into temperature values. The design is verified in 65nm standard digital CMOS process. The verification results show that the worst temperature inaccuracy is kept within 1°C with a one-point calibration from -55°C to 125°C . At room temperature, the average current consumption is only $0.8\mu\text{A}$ ($1.1\mu\text{A}$ in one phase and $0.5\mu\text{A}$ in the other) with 1.2V supply voltage and the total energy consumption for a complete measurement is only 0.384nJ .

Keywords temperature sensor · time-mode · duty-cycle modulation · energy efficiency

1 Introduction

Together with the development of VLSI, the integration of SOC's become larger and more complicated. In order to realize smart control of the systems, on-chip temperature sensors are integrated into the SOC's to provide accurate temperature informa-

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tion. Currently, the on-chip temperature sensors are widely used for enhancing system reliability and performance. Applications include dynamic thermal management of processors, random access memory refresh-rate control, and wireless sensor networks. The temperature sensors measure heat to ensure that a process stays within a certain range, providing safe use of an application, or meeting a mandatory condition when dealing with extreme heat, hazards, or inaccessible measuring points.

In the temperature sensors with $\Sigma\Delta$ ADCs [11,4], the whole power consumption is limited by the temperature information read-out circuits realized by ADCs. Due to the existence of conventional Opamps based integrators and oversampling mechanism, the power consumption is usually more than tens of μW . From the aspect of energy efficiency, the power hungry $\Sigma\Delta$ ADCs are not suitable. In [11], the authors recommend decreasing the required oversampling ratios (OSRs) by implementing a special ADC structure named zooming ADC. This ADC is based on a second-order $\Sigma\Delta$ ADC. With the same SNDR, it can reduce the required OSR to a quarter of that of the normal second-order $\Sigma\Delta$ ADCs. However, control logic of the zooming ADC is complicated, and the high gain Opamp within the ADC is still power-hungry.

As a result, new time-mode temperature sensor architectures were reported to avoid the utilization of ADCs. In [12], large temperature coefficient resistors were used for the frontend of the temperature sensor. Unfortunately, these resistors are not always available in standard digital CMOS process. In [2], MOSFET delay lines were used to generate temperature dependent information. The temperature accuracy was based on the temperature coefficient of the threshold voltages and electron carrier mobilities. In comparison to the conventional bipolar transistor frontend approach, the accuracy is unpredictable.

A recently published work [5] proposed an interesting approach which utilized the duty-cycle to process the temperature information. The duty-cycle based temperature sensors are superior than the frequency output ones as the ratio values are more linear than the absolute frequency values. However, a drawback of the design in [5] was the existence of two Opamps which consume $27\mu\text{A}$ to achieve high accuracy requirement (90dB gain and 70dB gain respectively) implemented in $0.7\mu\text{m}$ CMOS process. To further reduce the power consumption and maintain a high accuracy of the temperature sensor, a low power temperature-dependent oscillator is presented in the proposed design. As opposed to the structure that used two comparators in [9], a structure similar with [1] is utilized in the proposed design. As a result, only one comparator remains in the proposed design for further energy saving.

The output of the proposed design is the duty-cycle of a certain clock signal. In one phase when the reference is V_{BE} , the total current consumption is only $0.5\mu\text{A}$. In the other phase when the reference voltage becomes $n\Delta V_{BE}$, the total current consumption is $1.1\mu\text{A}$ in order to save die area. The settling time of the proposed temperature sensor is only 1 or 2 cycles (OSRs of the $\Sigma\Delta$ ADCs are usually larger than 100). In this manner, the total energy consumption for a complete measurement is only $0.384nJ$ when the output frequency at room temperature is around $5kHz$.

This paper is organized as follows: section 2 briefly introduces the system level algorithm and architecture. Section 3 provides the detailed circuit level analysis. The simulation results with one-point post-calibration are depicted in section 4. Finally, section 5 concludes the paper.

Fig. 1 Temperature Dependence of μ , $n\Delta V_{BE}$, V_{BE} , V_{BG}

2 System Algorithm and Architecture

2.1 Basic Algorithm Analysis

As widely known, the conventional approach to generate the temperature related information is the ratio between the PTAT (Proportional to Absolute Temperature) base-emitter voltage difference ΔV_{BE} of two bipolar transistors and the temperature independent bandgap voltage V_{BG} , which is

$$\mu = \frac{n \cdot \Delta V_{BE}}{V_{BG}} = \frac{n \cdot \Delta V_{BE}}{V_{BE} + n \cdot \Delta V_{BE}} \quad (1)$$

The numerator part $n\Delta V_{BE}$ of μ in equation (1) is PTAT and the denominator V_{BG} is temperature independent with careful selection of a fixed parameter n . Therefore, the temperature coefficient of μ is also PTAT. The temperature dependence of $n\Delta V_{BE}$, V_{BE} and V_{BG} are shown in Fig.1.

The horizontal axis in Fig.1 represents the temperature. The shaded range denotes the military temperature range from -55°C to 125°C . The PTAT ΔV_{BE} increases with temperature and the complementary to absolute temperature (CTAT) V_{BE} decreases with temperature. As the slope of V_{BE} is much greater than ΔV_{BE} , the parameter n is adopted to compensate the slope difference between them. The sum of $n\Delta V_{BE}$ and V_{BE} is the bandgap voltage V_{BG} which is temperature independent. From absolute zero to around 600K, the value of μ increases from zero to one, corresponding to the variation of $n\Delta V_{BE}$ and V_{BE} .

With a fixed conversion formula, the value of μ can be transferred into Celsius temperature value directly:

$$T = A \cdot \mu + B \quad (2)$$

In equation (2), A and B are constants, where A is around 600, and B is about -273K .

In order to avoid the implementation of ADCs, capacitors can be used to convert the temperature dependent voltages into time variables. With the simple formulae of capacitor charging,

$$\begin{aligned} t &= (V \cdot C)/I \\ V &= (I \cdot t)/C \end{aligned} \quad (3)$$

Equation (1) can be rewritten as

$$\mu = \frac{n \cdot \Delta V_{BE}}{V_{BG}} = \frac{\frac{I_1 \cdot t_1}{C_1}}{\frac{I_2 \cdot t_2}{C_2}} \quad (4)$$

In equation (4), t_1 represents the required time for the capacitor C_1 charging from ground to $n\Delta V_{BE}$, t_2 is the charging time from zero voltage to V_{BG} for capacitor C_2 . C_1 and C_2 are the charging capacitors for $n\Delta V_{BE}$ and V_{BG} respectively.

With the scaling of sub-micron processes, the supply voltages are usually equal to or even lower than 1.2V, which are less than the 1.25V bandgap voltage. In this manner, the important value V_{BG} is not available in advanced processes. If the combination of V_{BE} and $n\Delta V_{BE}$ is shifted into the digital domain, the limitation caused by process scaling will be relaxed.

As a result, another time parameter t_3 is introduced into equation (4). In this design, t_3 represents the charging time of capacitor C_3 from ground to V_{BE} .

Therefore, equation (4) can be rewritten as

$$\mu = \frac{n \cdot \Delta V_{BE}}{V_{BE} + n \cdot \Delta V_{BE}} = \frac{\frac{I_1 \cdot t_1}{C_1}}{\frac{I_3 \cdot t_3}{C_3} + \frac{I_1 \cdot t_1}{C_1}} = \frac{t_1}{t_3 + t_1} \quad (5)$$

As a result, only $n\Delta V_{BE}$ and V_{BE} are required in frontend of the sensor. As shown in equation (5), the value μ is converted into the ratio between two charging times if charging currents and capacitor values are equal.

Supposing t_1 corresponds to the phase of high voltage level (supply voltage 1.2V in this design) and t_3 is for the phase of low voltage level (ground), the value μ can be treated as the duty cycle of an oscillator output.

2.2 System Level Description

The block diagram of the system level is shown in Fig.2. The proposed temperature sensor contains two sub-blocks: the PTAT current generator front-end and the oscillator-based read-out part.

The PTAT current generator front-end is similar to the conventional structure: a PTAT current is generated by the gate-source voltage (V_{GS}) difference of two transistors in sub-threshold region across the resistor R_{BG} . Only currents in the two branches are consumed in this block. The current value for each branch is 38nA.

As mentioned previously, the summation of V_{BG} and $n\Delta V_{BE}$ is moved to the read-out part. Therefore, no additional V_{BG} branch is required. As a result, the power consumption is further reduced.

Fig. 2 System Level Block Diagram

Working mechanism of the oscillator is as follows: in phase ϕ_1 (ϕ_1 is high), the positive input node of the comparator (V_P) is connected to the reference voltage $n\Delta V_{BE}$. The negative input node of the comparator (V_N) is shorted to the top plate of the left capacitor C_1 . The charging current for C_1 is I_{PTAT} . When the rising edge of phase ϕ_1 arrives, capacitor C_1 is charged by I_{PTAT} . As long as the voltage V_N reaches $n\Delta V_{BE}$, the comparator generates a falling edge.

With the complementary phase clock generator, in phase ϕ_2 (ϕ_2 is high), C_3 is charged by I_{PTAT} , the left capacitor C_1 is discharged by a bypass switch. Meanwhile, V_{BE} is connected to the negative input node of the comparator as the reference voltage. When V_P approaches V_{BE} , a rising edge appears at the output of the comparator.

In this manner, the right block in Fig.2 behaves like an oscillator.

The proposed approach avoids the requirement of two comparators in different phases[5]. Unlike the general oscillators, the output period t_P is not constant, which is equal to

$$t_P = t_1 + t_3 = \frac{n \cdot \Delta V_{BE} \cdot C_1}{I_1} + \frac{V_{BE} \cdot C_3}{I_3} = \frac{V_{BG} \cdot C}{I} \quad (6)$$

If the current and capacitor values are equal, the period t_P is reciprocal to the PTAT current which is not linear with temperature as PTAT current is in the denominator. Fortunately, the absolute value of output frequency is not critical. The only important value is the ratio of t_1 and t_1+t_3 , which is the duty-cycle in the proposed design (μ in equation (5)). Consequently, the design requirement of the oscillator is relaxed as compared to the conventional oscillator.

Fig. 3 Complete Circuits for the Proposed Temperature Sensor

3 CIRCUIT REALIZATION

3.1 Description of the Oscillator

The detailed circuit diagram is depicted in Fig. 3. All the switches and current sources are shown with actual transistors. Apparently, comparing with the conventional ADC-based temperature sensors, the proposed design is much simpler. Therefore, the circuit complexity and power consumption are reduced.

Unlike in Fig. 2, the reference values $n\Delta V_{BE}$ and V_{BE} are shown in actual configuration. The resistor R_P has the same value as the R_{BG} in PTAT current generator. The biasing current for R_P in phase ϕ_1 is n times greater than that for R_{BG} to generate the reference voltage $n\Delta V_{BE}$.

The reason for using more current instead of larger size resistor is based on the consideration of area. Given that the value of R_{BG} is approximately $1M\Omega$ (the biasing current I_{PTAT} is $38nA$ in the proposed design). In order to generate enough $n\Delta V_{BE}$, the value of R_P will be almost $14M\Omega$. A resistor with such a large value in CMOS process occupies a significant area which results in a significant increase in cost. In cost comparison, the increase in biasing current in a half phase is more reasonable.

To increase the accuracy of current mirrors, cascode transistors are adopted. The nodes V_N and V_P correspond to the descriptions in Fig. 2. In order to make the reference voltages on V_P and V_N stable in the corresponding half cycle, two small parallel capacitors C_{1p} and C_{3p} are added to the resistor R_P and the bipolar transistor Q_1 respectively.

Moreover, Dynamic Element Matching (DEM) is employed for the current mirrors to reduce the influence of the mismatches among them [10]. The clock of DEM is ϕ_H which is equal to the frequency of the following TDC (or counter).

Fig. 4 Timing Diagram of the Oscillator

Fig.4 shows the simulation results of the voltages at the input and output nodes of the comparator. The upper clock signal is the same as ϕ_2 in Fig 3. When CK (ϕ_2) is high, V_N is equal to V_{BE} , V_P increases because C_1 is charged by the biasing current I_{PTAT} . As long as the value of V_P reaches V_N , the combination is alternated. $n\Delta V_{BE}$ appears on V_P and V_N increases until the output of the comparator changes. The waveforms of V_P and V_N are consistent to the analysis in the previous section.

The spikes appearing in Fig.4 are due to the settling of the two parallel capacitors (C_{1p} and C_{3p}). As the capacitors settle after a certain time interval, spikes can be observed. As long as the parallel capacitors settle within one quarter of the cycle, the spikes will not influence the final duty-cycle values.

To further improve the accuracy, chopping technique is utilized for removing offsets of comparators. In the proposed design, the chopping switches in the comparator are driven by a much lower frequency than the TDC which is ϕ_L in Fig.3. The frequency ratio of ϕ_H and ϕ_L is 16 in the proposed design. Besides the offsets, another source of inaccuracy for the comparators is the system delay t_{delay} . The parameter t_{delay} due to the delay of comparator and clock buffers.

In this design, the bias PTAT current is 38nA, R_P is chosen to be $1M\Omega$, C_1 and C_2 are both 8pF, and the clock frequency is around 5kHz at room temperature. As the t_{delay} is much smaller than $0.1\mu s$, the inaccuracy caused by t_{delay} can be ignored.

3.2 PTAT Current Generator

In order to maintain high accuracy and further simplify the design, a modified P-TAT current generator is chosen in this design. As mentioned, some publications [4, 12] used large temperature coefficient resistors to sense the temperature variation. However, these resistors are not available in many standard digital CMOS processes. Hence, to make the design suitable for general digital CMOS processes, the NMOS

Fig. 5 Circuits of PTAT Current Generator Front-end

transistors working in sub-threshold region are chosen as front-end of the proposed sensor.

According to [13], the gate to source voltage value of a NMOS transistor working in sub-threshold region can be depicted by the following equation:

$$V_{GS} = n \frac{KT}{q} \ln \frac{I_D}{(W/L)I_{D0}} \quad (7)$$

Therefore, the voltage drop on the resistor R_{BG} can be written as

$$V_{R_{BG}} = \Delta V_{GS} = V_{GS2} - V_{GS1} = n \frac{KT}{q} \ln \frac{(W/L)_1 I_2}{(W/L)_2 I_1} \quad (8)$$

where $n = 1 + C_d/C_{OX}$, C_d is the surface depletion capacitance, C_{OX} is the gate oxide capacitance. If I_1 is chosen to be equal to I_2 with PMOS current mirrors, the current through R_{BG} can be written as

$$I_{R_{BG}} = \frac{V_{R_{BG}}}{R_{BG}} = \frac{n}{R_{BG}} \frac{KT}{q} \ln \frac{(W/L)_1}{(W/L)_2} \quad (9)$$

In this manner, a PTAT current is generated with NMOS transistors working in sub-threshold region.

Fig. 5 shows the structure of the proposed PTAT current generator. As previously mentioned, it is not required to generate the bandgap voltage V_{BG} . Moreover, the only

necessary parameter is the PTAT current. Therefore, besides summation of branches of $n\Delta V_{BE}$ and V_{BE} , the two other branches which exist in [11,2] are also saved. As a result, the PTAT current generator in this design is much simpler than the other publications with bipolar transistors as the frontend of the temperature sensors.

R_{BG} in PTAT current generator is composed of two different resistor types. The $n+$ diffusion resistor has a PTAT temperature coefficient. The poly silicon resistor shows CTAT temperature behaviour. The combination of the two types of resistor ($1M\Omega$) has a temperature variation of less than 0.1% in the temperature range from -55°C to 125°C which corresponds to less than 0.01°C temperature error. In the proposed application, 0.01°C is within small fluctuation.

To maintain large output impedance of the current sources, cascode structures are adopted. The two transistors M_3 and M_4 are working in linear region as large resistors. As the current value is small, utilizing transistors instead of large resistors can further save the entire area. The size of M_1 is $(10\mu\text{m} \times 12)/200\text{nm}$. The size of M_2 is $(10\mu\text{m} \times 4)/200\text{nm}$.

Considering the mismatches between different current sources, DEM technique is also utilized for the current sources to further improve the accuracy of the PTAT current generator. In the proposed design, the DEM switches in the frontend is driven by ϕ_L in Fig.5. The bias currents for M_1 and M_2 are equal.

The start-up portion is composed of two transistors: M_9 and M_{10} .

The threshold voltage of a PMOS transistor is around 500mV in the adopted process. In the start-up period, when the voltage difference V_1 between V_{PS} and V_{NS} (V_2 between V_{PC} and V_{NS}) is greater than 0.5V, the start-up circuit is turned on. As a result, the voltage value of V_{PS} will decrease and V_{NS} will increase consequently.

When the PTAT current generator is working properly, the upper PMOS current source transistors $M_5 \sim M_8$ are working in saturation region. The voltage difference V_1 (or V_2) is around 200mV which is low enough to turn off the start-up paths.

4 CIRCUIT VERIFICATION

This design is verified with standard 65nm CMOS process. The layout area is $90\mu\text{m} \times 100\mu\text{m}$. The supply voltage is 1.2V. The total power consumption is 1.32 (or 0.6) μW . The total energy consumption for a completed measurement is only 0.384nJ when the output frequency in room temperature is around 5kHz . The accuracy FOM is $0.12\text{nJ}\%^2/\text{conversion}$ [11].

The 20 runs of post-layout Monte-Carlo simulations (variable process corners and mismatches) are performed. The post-layout simulation results are shown in Fig. 6.

In Fig. 6(a), the horizontal axis represents the temperature scale, ranging from -55°C to 125°C , which corresponds to the military range; the vertical axis corresponds to the duty-cycle values.

In order to suppress the influence of jitter at output of the oscillator, results of 2 cycles are averaged to generate the final duty cycle value. The sweeping step is 10°C within the temperature range. From -55°C to 125°C , the output duty cycle of the oscillator increases from around 35% to 72%.

Fig. 6 Post-layout Monte-Carlo Simulation Results for the proposed temperature sensor

In order to further analyze the accuracy of the proposed temperature sensor, one-point calibration is processed in MATLAB in room temperature. As the two-point calibration increases the cost significantly, some publications with two-point calibration [12, 8] are not suitable for mass production. Therefore, one point calibration is preferred for temperature sensor designs[11].

Fig.6(b) shows the temperature inaccuracy after one-point calibration in MATLAB at 25°C. Similarly, the horizontal axis corresponds to the temperature, and the vertical axis to temperature inaccuracy error after calibration. As shown in the Fig.6(b), the remaining temperature inaccuracy is less than 1°C. This error is mainly

Table 1 Performances Summary and Comparison

	[7]	[3]	[6]	[8]	Present Work
Type	FDC*	TDC**	TDC	Oscillator	Oscillator
Process (nm)	65	350	65	90	65
Power(μ A)	333	11.1	500	2.343	0.5/1.1
V_{DD} (V)	1.2	3.3	1	0.35	1~1.2
Temp. range($^{\circ}$ C)	-40~110	0~90	0~110	0~100	-55~125
Acc. 3σ ($^{\circ}$ C)	-2.9/2.7	-0.4/0.6	± 1.5	± 0.68	1
Calibr.($^{\circ}$ C)	@90	@ 10,70	@40	@ 15, 85	@25
Conv.time	3μ s	500ms	2.13μ s	0.1ms	0.4ms
Area(mm^2)	0.0066	0.6	0.008	0.003	0.009

* Frequency to Digital Converter

** Time to Digital Converter

due to the nonlinearity of I_{PTAT} in the PTAT current generator and the curvature of V_{BE} in the oscillator, which cannot be calibrated by one-point calibration.

The outputs of the proposed sensor can be processed by a simple counter based TDC which is driven by the internal timers. Due to the low frequency output, the TDC could achieve very high accuracy with common timers.

The performance of this design is compared with the state-of-the-art sensors as shown in Table I. After taking into account of the estimated power and performance losses due to manufacturing, wire bonding, package leads, PCB traces and other undesirable parasitic effects, the proposed design can still achieve excellent performance.

5 CONCLUSION

A simple and accurate time-mode duty-cycle-modulation-based temperature sensor is presented. For the purpose of simplification and process scaling, the temperature related information is converted from voltage-domain into time-domain. With the adoption of duty-cycle generated by the oscillator, the read-out circuits avoid the utilization of power hungry $\Sigma\Delta$ ADCs. According to the post-layout Monte-Carlo simulation results, the inaccuracy of the proposed temperature sensor with the utilization of one-point calibration is less than 1° C, which is enough for most energy efficient system applications.

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Appendix A: Proof of Choosing NMOS Transistors for PTAT Current Generator

Although bipolar transistors have better linearity than MOS transistors in sub-threshold region, there are two reasons for the utilizing of MOS transistors in this design.

The first consideration is the proper operation of the PMOS current source transistors. As the supply voltage is only 1.2V and the threshold voltages of the transistors are approximated to 0.5V, the value of V_{NS} is around 0.5V in room temperature. If bipolar transistors are adopted, V_{NS} becomes greater than 0.6V in room temperature which will drive the current source transistors into triode region. The accuracy of current mirroring will be affected.

On the other hand, the performance of parasitic bipolar transistors (PNPs) is not excellent in deep submicron processes. Based on simulations of the PNPs, the current gain β (current ratio of I_C over I_B) is even less than 1 which means the base current becomes comparable to the collector current.

As in most calculations, the base current is ignored based on large β value, the emitter current is supposed to be equal to the collector current. However, due to small β values, the errors of V_{BE} caused by β s cannot be neglected in the design.

$$V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{S1}}\right) = \frac{kT}{q} \ln\left(\frac{I_{PTAT}}{I_{S1}} \frac{\beta_1}{\beta_1 + 1}\right) \quad (10)$$

$$V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{S2}}\right) = \frac{kT}{q} \ln\left(\frac{I_{PTAT}}{I_{S2}} \frac{\beta_2}{\beta_2 + 1}\right) \quad (11)$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_{S1}}{I_{S2}} \frac{\beta_1}{\beta_1 + 1} \frac{\beta_2 + 1}{\beta_2}\right) \quad (12)$$

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_b} = \frac{(V_{BE1} - V_{BE2})}{R_b} = \frac{kT}{q \cdot R_b} \ln\left(\frac{I_{S1}}{I_{S2}} \frac{\beta_1}{\beta_1 + 1} \frac{\beta_2 + 1}{\beta_2}\right) \quad (13)$$

In the equations.(10-14), two bipolar transistors Q_1 and Q_2 are biased equally by I_{PTAT} . Each one has a saturation current I_S and current gain β accordingly. The bias current is generated by ΔV_{BE} crossing resistor R_b . As shown in equation.(13), the final PTAT current includes the parameter β . Unfortunately, β_1 and β_2 are not equal. Therefore, significant error appears with difference of β s.

Additionally, the value of β s is not flat when the emitter currents are swept. It is better to bias the PNPs with at least 1 μ A currents for operation in the flat region. Such large biasing current is not reasonable in the proposed application. Therefore, NMOS transistors instead of PNPs are chosen in the design.

Appendix B: Evaluation of the Influence of Mismatches

(1) Mismatch of Capacitors

For a 10 μ m x 10 μ m MIM capacitor, $\Delta C/C$ is approximated to 0.01% according to the tech files provided by the foundry. In the proposed design, 6pF for C1 and C2 are chosen (reasons will be calculated in the following answer), the capacitor's mismatch is $100/2500 \times 0.01\% = 4 \times 10^{-6}$.

Employing equation (5):

$$\mu = \frac{n \cdot \Delta V_{BE}}{V_{BE} + n \cdot \Delta V_{BE}} = \frac{\frac{I_1 \cdot t_1}{C_1}}{\frac{I_3 \cdot t_3}{C_3} + \frac{I_1 \cdot t_1}{C_1}} = \frac{t_1}{t_3 + t_1} \quad (14)$$

Considering the mismatch between C_1 and C_3 , assume $C_3 = (1 + \Delta C/C)C_1$, the above equation becomes:

$$\begin{aligned} \mu &= \frac{\frac{I_1 \cdot t_1}{C_1}}{\frac{I_3 \cdot t_3}{C_3} + \frac{I_1 \cdot t_1}{C_1}} = \frac{t_1}{t_1 + t_3 \frac{1}{1 + \Delta C/C}} \approx \frac{t_1}{t_1 + t_3 (1 - \frac{\Delta C}{C})} = \frac{t_1}{t_1 + t_3 - t_3 \frac{\Delta C}{C}} \\ &= \frac{t_1}{(t_1 + t_3)(1 - \frac{t_3}{t_1 + t_3} \frac{\Delta C}{C})} = \frac{t_1}{t_1 + t_3} (1 + \frac{t_3}{t_1 + t_3} \frac{\Delta C}{C}) \end{aligned} \quad (15)$$

As the values of duty-cycle are within 0.4 to 0.7 in the proposed design, the same range can be applied to $t_1/(t_1 + t_3)$. Therefore, the mismatch caused μ error (duty-cycle error) is less than $0.7 \times 4 \times 10^{-6}$. When the duty-cycle error is converted into actual temperature error, it is less than $2.8 \times 10^{-6} \times 600 = 1.68 \text{m}^\circ\text{C}$, which can be ignored in the proposed application.

(2) Mismatch of Currents

Using the same analysis for the mismatch of capacitors, assume $I_3 = (1 + \Delta I/I_1)I_1$, equation (5) becomes:

$$\begin{aligned} \mu &= \frac{\frac{I_1 \cdot t_1}{C_1}}{\frac{I_3 \cdot t_3}{C_3} + \frac{I_1 \cdot t_1}{C_1}} = \frac{t_1}{t_1 + t_3 (1 + \frac{\Delta I}{I})} = \frac{t_1}{t_1 + t_3 + t_3 \frac{\Delta I}{I}} \\ &= \frac{t_1}{(t_1 + t_3)(1 + \frac{t_3}{t_1 + t_3} \frac{\Delta I}{I})} = \frac{t_1}{t_1 + t_3} (1 + \frac{t_3}{t_1 + t_3} \frac{\Delta I}{I}) \end{aligned} \quad (16)$$

With the adopted DEM technique (just 3 more pairs of switches, negligible area), the residue mismatch reduces from $t_3/(t_1 + t_3)\Delta I/I$ to $t_3/(t_1 + t_3)(\Delta I/I)^2$. With a usual current mirror inaccuracy of 1%, the residue is less than $0.7 \times (1\%)^2 = 7 \times 10^{-5}$.

Related calculation can be found in page 60 of [10].

When it is converted into temperature error, it will be $7 \times 10^{-5} \times 600 = 0.04^\circ\text{C}$, which can be ignored in the proposed application.

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