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Effect of Direct Current Stressing to Cu-Cu Bond Interface Imperfection for Three Dimensional Integrated Circuits

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Abstract

The ability to be used as both a glue layer and the interconnection line has put Cu metal interconnection as the ultimate goal for 3D-IC. However, the inherent properties of Cu-Cu bond interface that are not always perfect have raised some concerns. This work investigates the evolution of the Cu-Cu bond interface that had been subjected to prolonged electrical current stress. Interface evolutions were characterized by a combination of electrical current stressing and bond interface cross-sectional analysis. While interface improvement was observed in terms of interface void reduction after current stressing, early failures to the interconnection line adjacent to the bond interface were observed. Electromigration had driven void migration from the large bond interface area to the much smaller adjoining interconnect line. This potentially has a significant impact on the future of 3D-IC technology that utilizes Cu-Cu bonding. However, this problem can be mitigated by inserting a barrier layer in between the bond interface and the interconnect line to prevent the migration of the voids into the interconnect line.

Keywords: 3DIC, Cu-Cu Bonding, Electromigration

1. Introduction

The prospect of utilizing Cu-Cu thermocompression bonding for fine-pitch bonding that provides mechanical adhesion as well as inter-layer electrical interconnection has drawn significant interest on the application of Cu-Cu bonding for three dimensional integrated circuits (3DIC) [1]. While there have been numerous demonstrations of Cu-Cu bonding [2], the observed bond interfaces were not always perfect [3]. The interface defects could come from pre-bonding surface imperfections such as surface's micro-roughness, dishing induced by chemical-mechanical-polishing (CMP) or contamination, leading to interface micro-voids. Furthermore, oxide precipitates are readily present at the bond interface even though care had been taken to minimize Cu oxide by surface pre-cleaning [4]. As a result, *true* contact area of the bond interface is only a fraction of the bonding pad's nominal area [4]. Interface imperfection potentially poses serious mechanical and electrical reliability concerns, particularly in future fine-pitch Cu-Cu bonds that handle high current densities.

From the point of view of electrical reliability, concern arises as an imperfect bond interface in the form of micro-voids can act as a vacancy source. In terms of electromigration, vacancies or even the whole void could migrate to someplace else driven by the flow of electrical current [5,6]. On the one hand, vacancy migration out of the bonding interface can be a positive phenomenon. They may indirectly improve the bond properties by reducing the interface voids. Or from another point of view, the true contact area can be increased with the electromigration induced void reduction. Electromigration-induced bond interface improvement had been reported in [7,8], as well as analytically modeled in [9], whereby the phenomenon has been indicated by a contact resistance reduction under direct current stressing.

On the other hand, problem of interconnection line weakening could arise when the bonded interface is adjoined by interconnection lines (e.g. structure shown in Fig.1). Vacancies that were in the bonding interface, driven by electromigration, could migrate and accumulate somewhere at any adjoining interconnection line. Significant accumulation of vacancies would lead to formation of voids, which have an adverse effect on the interconnection reliability. Voids on the interconnection line can lead to current crowding, localized heating, subsequently melting and failures. If this is true, the coupling of a bond interface with an interconnection line will have serious consequences, as it reduces the overall interconnection reliability.

In this paper, a study on the effect of direct current stressing to the bond interface that is adjoined to an interconnection line is presented. Experiments were focused on the observation of the Cu-Cu bond interface voids evolution under prolonged current stress. The experiments utilized a combination of electrical current stressing and bond interface cross-sectional analysis. In particular, we found that coupling of any bond interface with an interconnection line without a barrier layer would lead to serious reliability concern.

2. Experiments

The coupling effect between a bond interface and interconnect lines were evaluated by comparing the results from two types of constant current stressing. The two types of stressing at room temperature on cross-bar contact test structures [8], i.e. type 1 and type 2, are illustrated in Fig. 1 (a) and (b), respectively. In the first arrangement (type 1), the current source and ground terminal were placed in such a way that the stressing current flowed through the bond interface as shown in Fig. 1(a). A constant current was pumped from the source to the ground terminal as indicated by I^+ and I , respectively. At the same time, the voltage drop across the interface was monitored between V^+ and V terminals. In the second arrangement (type 2), the I^+ and I probes

were placed in such a way that the current did not flow through the bond interface, as shown in Fig. 1(b). Similar stressing was also conducted on daisy chain structures as shown in Fig. 1(c).

The structures were fabricated by bonding two 200 mm patterned Cu wafers face-to-face, followed by backside wafer thinning to access the probing pads for electrical characterization. The cross bar structures consist of only a single metallization layer and has three different metal line patterns with 6 μm , 8 μm and 10 μm width, to form two sizes of bonding interface, i.e. $8 \times 6 \mu\text{m}^2$ and $10 \times 8 \mu\text{m}^2$, respectively.

The daisy chain structures consist of two Cu metallization levels, namely M1 (interconnection) and M2 (bonding pad), respectively. They are separated by a Ta barrier layer. The bond interface was formed through the mating of the two M2 metallization from the two sides of the wafers.

Scanning Electron Microscopy (SEM) – Focus Ion Beam (FIB) cross-sectioning was used to obtain cross-sections of the bond interface for interface defects imaging. GIMP and ImageJ software were utilized to isolate and quantify the interface voids, respectively.

3. Results and Discussion

Table I. Samples' stress condition and failure time.

Sample No	Bond Size (μm)	Initial Contact Resistance ($\text{m}\Omega$)	Stress Current (A)	Type	Max Current Density		Stress Time/Failure Time (s)
					line (MA/cm^2)	interface (MA/cm^2)	
1	8×6	$2.86 \pm 4.03 \times 10^{-3}$	0.12	1	2	0.25	10000*
2	8×6	$3.03 \pm 4.00 \times 10^{-3}$	0.12	1	2	0.25	10000*
3	8×6	$2.96 \pm 4.41 \times 10^{-3}$	0.12	2	2	NA	10000*
4	8×6	$2.97 \pm 5.31 \times 10^{-3}$	0.18	1	3	0.375	160
5	8×6	$2.81 \pm 3.96 \times 10^{-3}$	0.18	2	3	NA	4600
6	10×8	$2.76 \pm 2.45 \times 10^{-2}$	0.3	2	3.75	NA	32400
7	10×8	$2.76 \pm 2.56 \times 10^{-2}$	0.3	2	3.75	NA	940
8	10×8	$2.80 \pm 2.65 \times 10^{-2}$	0.3	1	3.75	0.375	20
9	10×8	$2.76 \pm 4.28 \times 10^{-2}$	0.3	1	3.75	0.375	2

* No Failure

Table I summarizes the test structures' initial contact resistance as well as their stress condition. It should be noted that the current density in the line is much higher than the current density through the bond interface. Under current stressing, all structures were observed to have a linear relationship between current and voltage (i.e. ohmic behaviour), with the $8 \times 6 \mu\text{m}^2$ and $10 \times 8 \mu\text{m}^2$ bonded area having an average initial contact resistance of $2.93 \pm 4.34 \times 10^{-3} \text{ m}\Omega$ and $2.77 \pm 2.98 \times 10^{-2} \text{ m}\Omega$, respectively.

Apart from samples 1 to 3 that had not failed, it was observed from samples 4 to 9, that stressing of type 1 (i.e. stress current passed through the bond interface) failed much faster as compared to type 2 (i.e. stress current did not pass through the interface). Open-circuit failures were observed from the abrupt change in the monitored resistance. Failure

on type 1 stressing is signified by a sudden drop in the monitored voltage between V^+ and V^- as well as monitored current at I terminal.

Fig. 2(a) shows the positions of multiple FIB cuts on a single cross bar structure. It can be observed that the voids are distributed across the entire bonding interface as shown in Fig. 2(b); with the center of the bond having the highest quantity of voids as shown in Fig. 2(c). These results suggest that the observable quantity of voids can be subjective. The main reason for this is that different quantity of voids depends on the position of FIB cuts with respect to the geometry of the cross-bar structure. When taken parallel to either of cross bar's arm, the void area appears larger as compared to a FIB cut that is done closer to the center of the bonding. However, it was relatively difficult to maintain consistent cutting location of multiple cuts on a single test structure. Thus, to maintain consistent cutting location, FIB cuts were taken diagonally with respect to the geometry of the bonding pad as shown in Fig. 3 (a), with the corners of the cross-bar structure used as markers. On the same figure, it also shows the typical failure site for type 1 stress condition, i.e. at adjacent Cu line away from the bond interface as shown in Fig. 3(a).

Fig. 3 (b) shows side to side comparison of the SEM cross sections from type 1 and type 2 with respect to a control sample (unstressed sample). To maintain consistency, the cross sectional SEM images were taken diagonally with respect to the cross-bar structure as indicated by the "FIB cutting line" in Fig. 2 (a), where the corners of the cross-bar structure act as a natural marker for the cutting line. It can be clearly observed that there is a distinct difference in the quantity of interface voids for different stress conditions. Voids were quantified by first isolating the void image from SEM by GIMP software and followed by void area calculation by means of pixel counting using ImageJ software. As shown in Fig. 3(c), it reveals that the structures that had

current stressing through the interface have less voids as compared to type 2 stressing, as well as those samples that were not subjected to current stressing.

SEM-FIB on the stressed daisy chain also shows a similar trend in terms of the interface voids as shown in Fig. 3. Daisy chain that had gone through 1 hr stressing with 50 mA shows less voids at the bond interface as compared to non-stressed daisy chain structures. These observations have been confirmed by void quantity analysis, as shown in Fig. 4(a) and (b) for non-stressed and stressed daisy chain, respectively.

Another interesting observation is that, after current stressing, more voids were observed to accumulate at the barrier-Cu M1 interface, as pointed out by solid arrows in Fig. 3. The presence of Ta between M1 and M2 acts as a diffusion barrier and effectively blocks any materials transfer. Hence, the voids between the two metallization layers can only originate from other source, that is the interconnection lines instead of the bond interface.

Based on the current results, we can deduce that the voids from the bond interface could be driven somewhere else into the interconnect system by the electric current. This mechanism could improve the bonding properties as indicated by a reduction of interface's voids. This observation is in agreement with earlier experimental results in [5, 6], and later modeled in [9], that is direct current stressing on the bond interface may improve the bond properties. However, the voids at the interface could, and have been observed to accumulate in the interconnection lines under current stressing. With significant number of vacancies accumulation, voids could form, which in turn weakens the interconnection line and accelerates the interconnection line failure. The entire mechanism is as illustrated in Fig. 5(a).

Usage of a barrier layer between the adjoining interconnection line and the bond interface could thus help to prevent the interconnection-bond interface coupling effect, whereby the barrier

layer could effectively prevent vacancy migration from the bond interface to the interconnection line and ultimately reduce possible void formation due to vacancy accumulation. However, it is undesirable as this barrier layer between the Cu bonding pad and interconnection line increases the total interconnection resistance, as illustrated in Fig. 6(b).

4. Summary and Conclusions

The effects of direct current stressing on Cu-Cu bond interface have been evaluated. While there is an improvement in the bond property in terms of a reduction in interface void volume, there is a possibility of new reliability issues due to the coupling of an interconnection line directly with the bond interface, which causes a shorter failure time. The weakening of the interconnection line is caused by the accumulation of vacancies/voids from the much larger bond interface area into the narrower interconnection line, driven by an applied electrical current. This reduction in the interconnect line reliability may be prevented by blocking materials flow with a diffusion barrier layer incorporated between the bond interface and the adjoining interconnects line.

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Figure Captions

Fig. 1. Test structure designs and stressing methodology. (a) Type 1 stressing, the stress current passes through the interconnect lines as well as the bond interface, (b) Type 2 stressing, stress current only passes through the interconnection line, (c) current stressing on daisy chain structure.

Fig. 2. Multiple cuts on a single cross bar structure show that the voids are distributed across the entire bonding interface. (a) Top view SEM image showing cutting location with respect to cross bar structure, (b) cross sectional SEM images at three different cutting locations, (c) interface voids quantification by void isolation and pixel counting.

Fig. 3. Void characterization through diagonal FIB cutting, (a) Failure site is typically observed on the adjacent Cu line away from the bond interface, closer to the source ($I+$) terminal, (b) SEM-FIB cross section comparisons between structures that had gone through different stressing, i.e. Type 1 stressing, type 2 stressing and control sample and (c) interface voids quantification by void isolation and pixel counting.

Fig. 4. SEM-FIB cross section comparison between daisy chain structures that were subjected to current stressing. Solid and dashed arrow points to voids found between barrier and M1-Cu interface, voids found on the bounding interface and current direction, respectively. (a) No current stressing, (b) 50 mA for 1 hour.

Fig. 5. Voids quantification and comparison of stresses and non-stresses daisy chain structure from SEM-FIB cross section images by ImageJ. Stressed structure has lower average void quantity at bond interface. (a) Non-stressed daisy chains. (b) stressed daisy chain 50 mA current for 1 h.

Fig. 6. Illustration of interface voids evolution, (a) electric current drives voids from the bond interface to interconnection line, which in turn weakens the interconnection line and accelerates the interconnection line failure. (b) Usage of barrier layer between the interconnection line and the bond interface could help to prevent the interconnection-bond interface coupling effect by blocking the void movement from bonding interface to interconnection line, which also increases the total interconnection resistance.

Fig. 1.

(a)

(b)

(c)

Fig. 2.

(a)

(b)

Type 1 void isolation: 0.009 μ m ²
Type 1 void isolation: 0.012 μ m ²
Type 2 void isolation: 0.032 μ m ²
Control void isolation: 0.118 μ m ²

(c)

Fig. 3.

Fig. 4.

Fig. 5.

Fig. 6.