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A DC to 14GHz Fully Differential Amplifier for Wideband low power applications

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Abstract—This paper presents a high performance wideband amplifier and justifies the performance with the aid of measurement results. The amplifier consumes very low power about 6.8mW from a supply voltage of 1.8V. The amplifier is designed using a cross coupled cascode topology to improve the Gain and Bandwidth. The design is implemented in a 0.18 μ m SiGe BiCMOS process (ft = 200GHz) with 9.3dB small signal differential Gain and a flat 3dB Bandwidth from DC to 14GHz. The design size of the core amplifier is 230 μ m x 80 μ m.

Keywords—Wideband Amplifier, Differential amplifier, SiGe BiCMOS process, low power, millimeter-wave

I. INTRODUCTION

With the ever increasing demand of present generation for quick access to huge amount of information from internet and other sources, there is need for data transmission media that supports higher data access speeds. This calls for Wired or Wireless Transceivers operating at higher data rates. The recently introduced 60GHz ISM band supports larger bandwidth of about 7GHz which is continuous [6]. So that the standards governing the Data transmission at this frequency band like IEEE 802.15.3c, 802.11ad, etc can have the flexibility to determine the number of channels and the channel bandwidth within the 7GHz window.

Such 60GHz Transceivers require building blocks operating at higher frequency with larger bandwidth [7]. Mainly the power output to meet Link budget requirement needs Wideband Amplifiers at intermediate stages of the Transmitter chain to boost the Power Gain without saturation. At this higher frequency of 60GHz there is large amount of Noise interference affecting the Receiver chain. Hence to improve the Signal to Noise ratio we again need Wideband Amplifiers at the various stages to reduce the overall Noise figure of the Receiver chain.

The paper is organized as sections with Section II briefing on the Wideband amplifier design consideration and providing an analytical description on the design of the proposed amplifier. Section III, covers the Measurement results obtained from on-wafer testing of the design and Section IV concludes the paper with revisit to important aspects and performance of the design proposed.

II. DESIGN ANALYSIS OF PROPOSED WIDEBAND AMPLIFIER

There are few properties that are required from these Wideband Amplifiers which makes them suitable to be utilized at both transmitter and receiver sections of the Transceiver [7]. The Wideband amplifiers, as the name suggests, must support wide bandwidth, operate at higher frequencies, provide higher Gain, consume very less power, occupy very small footprint in the Transceiver chip area and support power shutdown option using a digital input pin. The Power shutdown option is necessary for saving power in the Time multiplexing scheme between Transmitter and Receiver sections. All these features enable the Wideband Amplifiers to be integrated in the Transceivers for portable mobile applications. This paper proposes one such Wideband amplifiers with measurement results to verify its performance.

The proposed Wideband amplifier has a fully differential architecture which has both input and output with differential signaling as shown in Fig 1. This architecture ensures to eliminate the even order harmonics and improves the circuit linearity.

Fig.1. Circuit Schematic of Proposed Wideband Amplifier

One of the important concerns of the differential amplifiers is that it is very difficult to fabricate a perfect symmetrical circuit even on the same wafer or die. This process related asymmetry causes the common mode signals to be seen along with the differential output. This common mode Gain of the differential amplifier is undesirable for certain biomedical

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applications and for precision devices. A small common mode signal can induce distortion in the final output. The ability of the differential amplifier to suppress the common mode signals as compared to the differential signal input is the Common Mode Rejection ratio. In addition the asymmetry or device mismatch causes DC offset to be seen at the final output. Since the proposed amplifier is capable of amplifying the signals from DC, the DC offsets affect the output response. With the cross-coupled structure in the proposed design, the current distribution between the two arms of the differential amplifier is evenly distributed to avoid any offsets due to mismatch between the differential pairs. The mismatch is equally shared between both the Differential ends [4].

Fig.2 (a) Current distribution (b) Differential amplifier equivalent

This is illustrated in the Fig 2(a). The current entering each of the differential pair arms is “ I_Q ” through the Load resistors, R_L . Then for a small signal input $v_{in} = -\delta v$ and $v_{ip} = +\delta v$, the corresponding increase seen in the Collector current of Q1 and Q2 is $\delta I/2$, and decrease of collector current of Q3 and Q4 is also by same amount $\delta I/2$.

The Fig 2 suggests that a change in collector current of $\delta I/2$ corresponds to a small signal voltage δv based on the Transistor characteristic equation,

$$I_c = I_s \cdot e^{\frac{-v_{be}}{\eta V_T}} \quad (1)$$

Differentiating I_c with respect to v_{be} we get,

$$\delta I_c = -\frac{I_s}{\eta V_T} \cdot e^{\frac{-v_{be}}{\eta V_T}} \cdot \delta v_{be} = -g_m \cdot \delta v_{be} \quad (2)$$

where,

$$g_m = \frac{I_s}{\eta V_T} \cdot e^{\frac{-v_{be}}{\eta V_T}} = \frac{I_c}{\eta V_T} \quad (3)$$

g_m is dependant on I_c and Temperature. From Fig 2,

$$\frac{\delta I}{2} = -g_m \cdot \delta v \quad (4)$$

The circuit is basically equivalent to two differential pairs connected in parallel with configurations as in Fig 2(b). The currents entering and leaving the two arms of the differential pair is consistent with the circuit operation and also the errors get cancelled including the leakage currents as illustrated in the

Fig 2. All the 4 transistors are designed to be of same size. The topology simplifies the layout implementation making the process variations to have very little influence on the performance of the amplifier as shown in Fig 3 below.

Fig.3. Layout of the cross-coupled Quad transistors

Current sources provide advantages of setting the fixed bias current and also can be easily employed for power down control using transistor switches. The switches can be placed at the first current mirror and the power shut off is propagated through the current sources. This sets the current in the whole amplifier approach to 0A.

This amplifier can be integrated in the transceiver ICs as Intermediate Amplifier to set the Gain for required Link budget. When the Transceiver is operated with Time-Domain multiplexing mode, the circuits in the Transmitter or Receiver chain, which is not functional, can shut off their DC power consumption. This can be achieved with the proposed amplifier using the power down digital pin. This pin can be accessed externally and when it is set to 1.8V, the amplifier is shut off and consumes a negligible amount of current in the range of nanoamperes (nA). For normal circuit operation, the pin must be set to 0V.

The capacitive feed-through is overcome by the cascode stage stacked above the cross coupled pair. This introduces isolation between the input and the inverting output. Otherwise it introduces the Miller capacitive effect as shown in Fig 7.

The circuit requirement suggests providing fixed gain from DC to 14GHz. Hence the DC is not blocked along the signal path and is equally amplified. The 1.5dB Gain flatness achieves a bandwidth of up to 10GHz. The design avoids Inductors, capacitors which are frequency dependant components and hence the Layout becomes very compact – 230 μ m x 80 μ m. The more compact the design, its cost in the SOC integration is also reduced.

III. EXPERIMENTAL RESULTS

The proposed IFA design was fabricated using 0.18 μ m SiGe BiCMOS technology from Tower-Jazz Semiconductor. The Fig 4 shows the microphotograph of the design implemented. The core area of the Amplifier occupies only 0.2mm x 0.08mm excluding the IO pads. For aiding in on-wafer measurement the differential RF inputs and outputs are extended to GSSG RF pads along with VDD supply and Power down digital input using Digital Pads. The amplifier was measured using Vector Network Analyzer (VNA).

TABLE I. SUMMARY OF PERFORMANCE OF WIDEBAND AMPLIFIERS

Parameters	Units	[1]	[2]	[3]	[5]	This work
Technology	-	0.8 μ m SiGe HBT	0.13 μ m CMOS	0.25 μ m SiGe BiCMOS	0.35 μ m SiGe BiCMOS	0.18μm SiGe BiCMOS
Bandwidth	GHz	3.1 to 10.6	DC to 11.5	DC to 7.8	1.2 to 17	DC to 14.3
Gain (S21)	dB	19.9	13.2	10.6	8.5	9.3
Topology	-	DE - Emitter coupled pair	SE - splitting-load inductive peaking	SE - CB-CC cascade	SE – multiple f/b inductive peaking	DE - Cross coupled Cascode
Power consumption	mW	77	9.1	6.5	21	6.8
Core Area	mm ²	0.14 (IO Pad)	0.08	0.26 x 0.52	0.775 x 0.71	0.22 x 0.08
Noise Figure	dB	2.9	5.6	4.4	5.7	6.9*

SE – Single Ended and DE – Differential Ended

* - Post simulation result for Noise Figure

Fig.4. Microphotograph of the Amplifier with the Test probes – GSSG for differential I/O, 3 DC probes

For normal amplifier operation, the VDD voltage is set to 1.8V and the Power Down pin is set to 0V. The differential I/O GSSG probes are connected to the Input and output of the amplifier to measure the small signal S-parameters.

From the 1.8V voltage source, the amplifier consumes 3.8mA of current at 27deg C room temperature. The measured small signal differential gain S_{dd21} in the flat band as shown in the Fig 5 is on average equal to 9.3dB and measured 3dB bandwidth is 14.3GHz. This design incorporated the considerations for wider bandwidth and is evident from the measurement plot. The bandwidth with 1.5dB gain flatness is 10.1-GHz. Fig 6 suggests output matching is less than -15.5dB over the entire amplifier range.

Since the measurement setup had a limitation for measuring circuit Noise Figure, we have summarized the post-simulation Noise Figure value in the Summary table. The Noise figure obtained from simulation plot of 6.8dB suggests a flat noise figure value till 10.1GHz and gradually increases as the Gain drops with increase in measurement frequency.

Fig.5. Measurement plot of the Amplifier Small signal Gain (|S21|) against frequency

Fig.6. Measurement plot of Output Return Loss (|S22|) against frequency

Fig.7. Common Emitter stage against the Cascode stage for enhancement of Bandwidth

The measurement results of the proposed work and a comparison of the results with the previous work are summarized in the Table 1. The proposed design achieves best gain-bandwidth product figure of merit with economical use of DC Power consumption of only 6.8mW and active chip area of $0.22 \times 0.08 \text{ mm}^2$.

The amplifier stability factors namely K_f and $B1f$ (Δ) are measured against frequency and plots are shown in Fig 8 and Fig 9. The plot suggests that the amplifier is unconditionally stable over entire operating frequency range.

Fig.8. Measurement plot of Stability factor, ($K_f \geq 1$)

IV. CONCLUSION

A wideband SiGe BiCMOS amplifier with very low power consumption and suitable design convenient for Layout implementation has been presented. The proposed amplifier incorporates features like cross-coupled cascode topology to meet the target of wide bandwidth and high Gain. The power down functionality renders the circuit to be inactive when not operational with negligible current consumption in range of tens of nanoamperes. The design architecture is very less susceptible to process variation providing a small signal Gain of +9.3dB over a 3dB bandwidth of 14.3GHz. Furthermore the amplifier consumes a total current of 3.8mA using a supply voltage of 1.8V and occupies a core area without IO pads of $0.22 \times 0.08 \text{ mm}^2$.

Fig.9. Measurement plot of Stability factor, ($B1f \geq 0$)

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