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# SI and EMI Performance of Signaling Scheme through UTP cable

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**Abstract**— Signal integrity (SI) and electromagnetic interference (EMI) performances of single-ended and differential-pair schemes through an unshielded twisted pair (UTP) cable have been studied systematically through experiment. The EMI performance is evaluated with measurement of common-mode (CM) noise current on the UTP cable. The SI performance is assessed by measurement of digital waveforms with and without the UTP cable connected.

**Index Terms**—Common-mode current, electromagnetic compatibility, signal integrity, low voltage differential signalling

## I. INTRODUCTION

Data transmissions between electronic modules are usually achieved with either single-ended (SE) or differential-pair (DP) configuration. Analyses have been carried out to study the impact of characteristic impedance for different signaling schemes on EMI and voltage stability [1]. When high-speed digital signals propagate through a cable, SI problem may arise together with radiated emissions from the cable. Significant level of common-mode (CM) current on the cable can be an EMI concern [2]. It has been shown that SE signaling generates higher CM noise in the presence of a split ground plane on the PCB [3]. There is no comprehensive study on the SI and EMI performances of different signal schemes through cable, such as the unshielded twisted pair (UTP). This paper aims to carry out such a study for more conclusive results. To facilitate a systematic study, two logic families, low-voltage transistor-transistor logic (LVTTTL) and low-voltage differential signaling (LVDS) are selected for SE and DP signaling schemes implementations, respectively [4]. For fair comparison, all these logic gates are sourced from the same manufacturer. To know the impact of data rates on the SI and EMI performances, digital signals at 25, 50, 75, and 100 MHz are selected for the study [5].

To evaluate the SI performance, digital signal waveforms will be measured with and without UTP cable. Also, the CM current will be measured at the mid-point of the UTP cable to access the EMI performance. The UTP cable is chosen for the study as it is commonly used for typical local area network (LAN) connections. The characteristic impedance of such cable is  $100\Omega \pm 15\Omega$  operating in the band of 1 MHz to 200 MHz [6].

## II. DESIGN OF TEST CASE

Three printed circuit boards (PCBs) are designed and fabricated for this study [7]. Fig. 1 shows the schematic of the clock driver circuit for the LVTTTL digital signal.

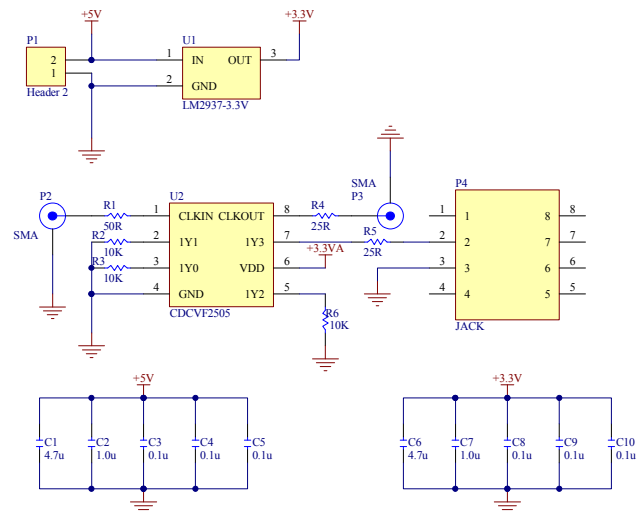


Figure 1. Schematic of LVTTTL clock driver circuit

The circuit is fabricated on a two layer PCB. The clock buffer has the flexibility to generate clock frequency from 24 MHz to 200 MHz [8]. The second PCB contains a digital clock circuit that consists of a SE to differential driver [9]. It converts the SE serial input signals from the clock buffer to LVDS signals. The LVTTTL – LVDS driver could handle a maximum data rate of 400 Mbps. Typical LVDS logic has an output differential voltage of 350 mV when terminated with a 100 $\Omega$  resistor. According to the specifications, the minimum differential voltage terminated by a 100 $\Omega$  resistor is found to be 247 mV. The traces for the output signals were kept short and symmetrical so as to minimize the differential-mode (DM) to CM conversion due imbalance [10]. For both the driver cards, they are able to make use of signals generated from an external source through a SMA connector interface. The provision allows the study to be carried out at different data transmission rates. The clock buffer provides well-defined logic signals of the same edge rate from the functional generator at varying clock frequencies of 25 MHz, 50 MHz, 75 MHz, and 100 MHz.

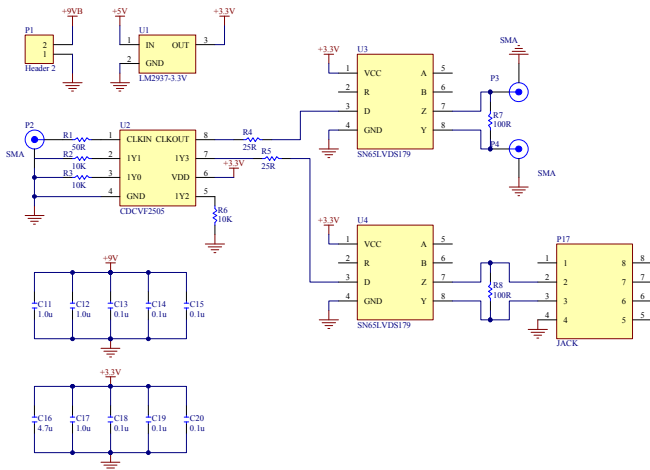


Figure 2. Schematic of circuit to generate LVDS signal

Fig. 3 shows the block diagram of the PCB designed to facilitate the measurement of the output signal waveform from the other two PCBs mentioned earlier. It provides the necessary RJ45 and SMA connections. The SMA connectors will be used to interface with external measurement instrument.

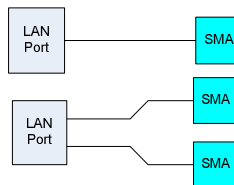


Figure 3. Block diagram of waveform monitor board for SE and DP signals measurement

### III. EXPERIMENTAL SETUP

Fig. 4 shows the experimental setup for performing the SI and the CM current measurements. To measure the digital waveforms, a high-speed digital phosphorous oscilloscope (500 MHz / 5 GS/s) is used. For the CM current measurement, a wideband current probe (1 MHz – 1.2 GHz) is employed. The current probe is clamped onto the middle of the UTP LAN cable of 2.7 m in length. A 25 dB pre-amplifier (1 MHz – 1.2 GHz) is connected between the current probe and the spectrum analyzer (9 kHz - 6.5 GHz) to improve the measurement sensitivity, as the CM current is usually quite small.

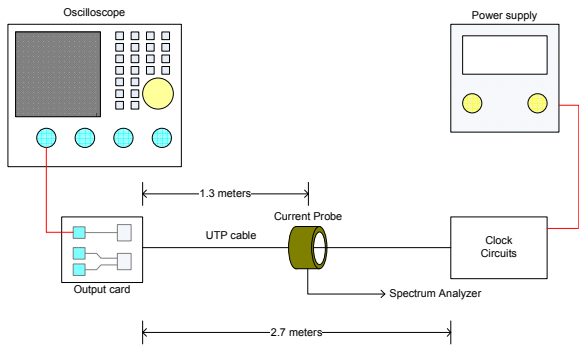


Figure 4. Experimental setup for measuring SI and CM current

### A. Signal integrity measurement results

Fig. 5 shows the measurement points to be probed for the SE signaling scheme.

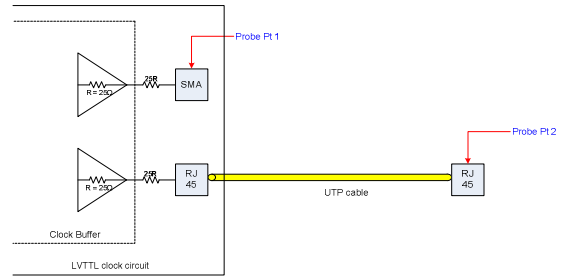


Figure 5. Probing points for LVTTL SE signaling

For the measurement, the digital signal without any cable interface is obtained at probe point 1. Probe point 2, which is at the far-end of the cable, will be measured once the cable is connected to the LVTTL clock driver circuit. Using the measured waveform at probe point 1 as a reference, the waveform at probe point 2 will be compared with the reference waveform to access the SI performance of the transmitted signal through the cable. Figs. 6 to 9 show source and received waveforms of the LVTTL signals at different data rates. The results show that for LVTTL signal, the performance of the received signal degrades with increasing data rate. Very obvious signal distortion is observed. The amplitude of the received logic level can be nearly 50% of the transmit logic level.

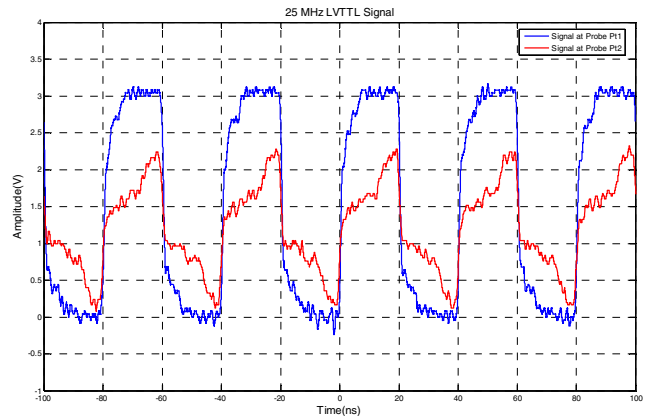


Figure 6. 25MHz LVTTL signal measured at probe points 1 and 2

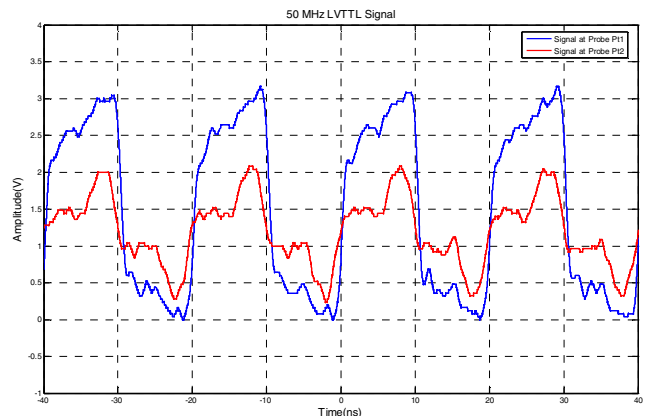


Figure 7. 50MHz LVTTTL signal measured at probe points 1 and 2

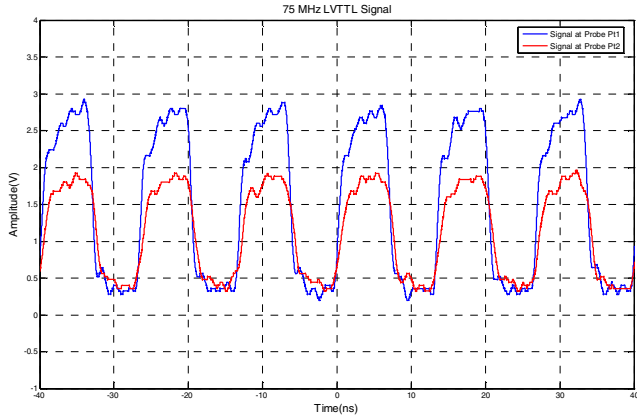


Figure 8. 75MHz LVTTTL signal measured at probe points 1 and 2

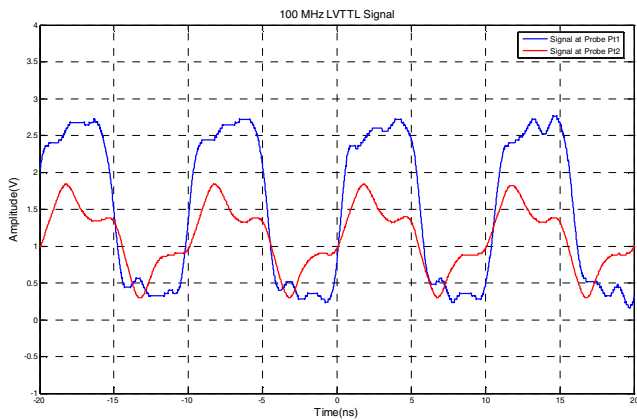


Figure 9. 100MHz LVTTTL signal measured at probe points 1 and 2

Fig 10 shows the terminations and probe points for the measurement of LVDS signaling. Similarly, probe point 1 measures the LVDS signal when the driver is terminated with  $100 \Omega$  directly without cable connection. Probe point 2 measures the LVDS signal after the signal propagating down the UTP cable.

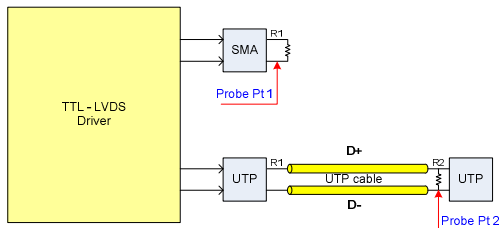


Figure 10. Terminations and probe points for LVDS circuit

Fig. 11 shows the attenuation versus frequency plot per 100 m for a UTP Cat 5 cable [11]. Even at 100 MHz, the attenuation for a 2.7 m UTP cable is only slightly more than 0.5 dB.

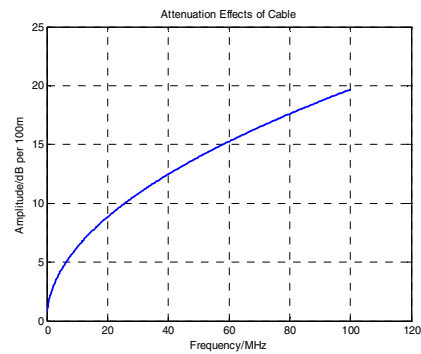


Figure 11. Attenuation of Cat 5 UTP cable versus frequency

Figs. 12 to 15 show the waveforms for the LVDS signal measured at probe points 1 and 2 for 25 MHz, 50 MHz, 75 MHz and 100 MHz data rates, respectively.

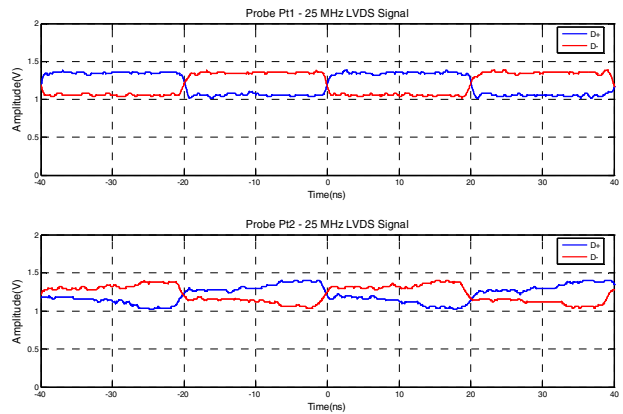


Figure 12. 25 MHz LVDS signal measured at probe points 1 and 2

The measured results show that though the received signal suffered some distortion but the logic levels have little attenuation, even up to 100 MHz clock speed.

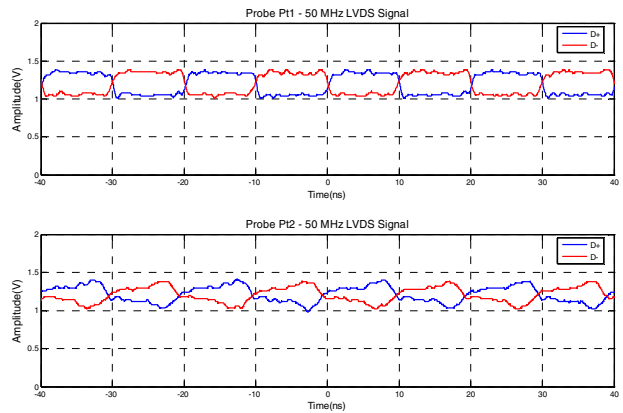


Figure 13. 50 MHz LVDS signal measured at probe points 1 and 2

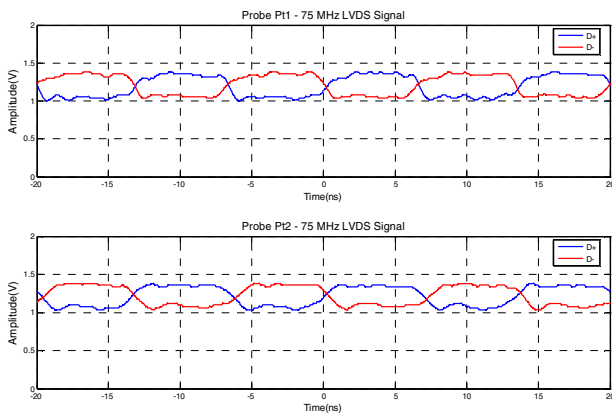


Figure 14. 75 MHz LVDS signal measured at probe points 1 and 2

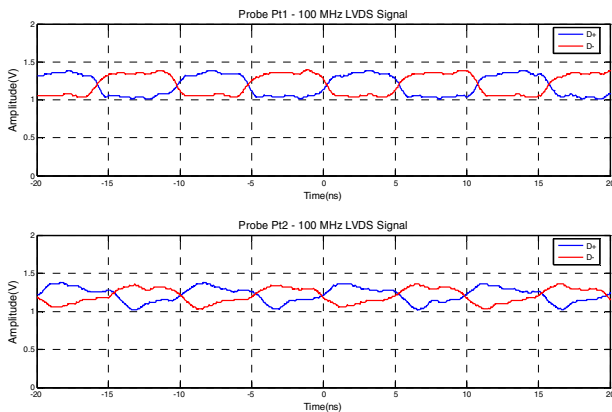


Figure 15. 100 MHz LVDS signal measured at probe points 1 and 2

#### IV. COMMON MODE CURRENT MEASUREMENT

Fig. 16 shows the measured CM noise current up to 1 GHz when LVTTTL signals of the four clock frequencies are sent through the UTP cable. The fundamental and the associated harmonics of the clock frequency are clearly observed in the CM current spectrum. For all the four cases, significant levels of CM current spectrum have been measured. Such levels of CM currents will cause the 2.7 m UTP cable to radiate efficiently as a wire antenna up to 1 GHz.

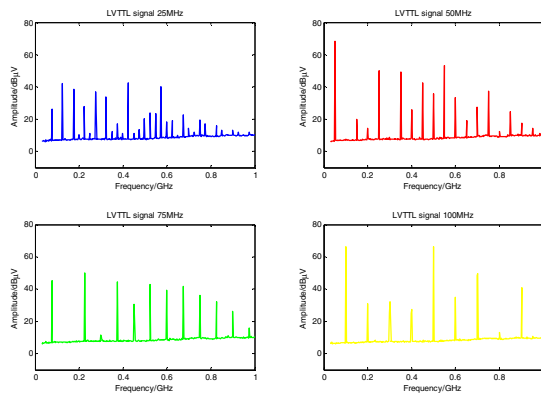


Figure 16. CM current for SE signaling scheme at 25, 50, 75 and 100 MHz

Fig. 17 shows the CM noise current measured when LVDS signal of the four clock frequencies are sent through the UTP cable. It shows that CM current levels are 20 to 30 dB lower than those of the SE signaling. At 100 MHz, noticeable levels of CM currents begin to show up but are still much lower than those of the SE signaling operated at the same frequency.

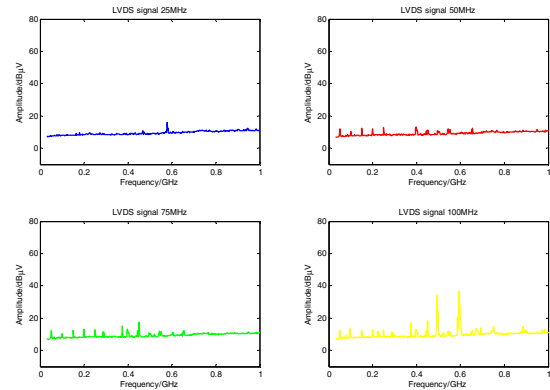


Figure 17. CM current for DP signaling scheme at 25, 50, 75 and 100 MHz

#### V. CONCLUSIONS

A systematic study of the SE and DP signaling schemes through an UTP cable has been carried out experimentally. It shows that even at relatively low data rate of 25 MHz, the LVDS signal (SE scheme) has already suffered from significant signal distortion and attenuation. Also, significant amount of CM noise current with harmonics up to 1 GHz is also observed, which indicates a high EMI potential to other communication users. As for the LVTTTL signal (DP scheme), reasonably good SI is observed and CM noise current begins to surface when the data rate exceeds 75 MHz.

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