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An 8mW Ultra Low Power 60GHz Direct-conversion Receiver with 55dB Gain and 4.9dB Noise Figure in 65nm CMOS

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Abstract — An ultra low power direct-conversion receiver is demonstrated for V-band 60GHz applications in 65nm CMOS process. The power consumption is significantly reduced by the design of low-power low noise amplifier (LNA), transconductance mixer and variable gain amplifier (VGA). A compact quadrature-hybrid coupler is developed for transconductance mixer for the reduction of both power and area. The proposed receiver (0.34mm² chip area) is measured with 8mW power, the minimum single-side-band (SSB) noise figure (NF) of 4.9dB, and the maximum power conversion gain of 55dB.

Index Terms — CMOS 65nm, ultra low power, 60GHz receiver.

I. INTRODUCTION

Thanks to the rapid scaling of CMOS process, it has become possible to implement 60GHz high data-rate wireless system by low-cost CMOS integrated circuits (ICs). In 60GHz transceiver design, receiver front-end is a critical block that amplifies small RF signal from antenna and down converts it to baseband under specified signal-to-noise ratio. In order to achieve high-order modulation with efficient bandwidth utilization and also desired communication range, the receiver must satisfy high gain, high linearity and low noise figure (NF) requirements. However, the high gain, high linearity and low noise performance specifications introduce the expense of power overhead for portable applications. As such, ultra low power receiver design is desirable but also challenging for 60GHz CMOS receiver design. Recently, several excellent 60GHz CMOS direct-conversion receivers front-end have been reported [1], [2]. However, all these 60GHz direct-conversion receivers have high power consumption from 50.2mW to 34mW. As such, it is of great interest to design the low NF and high gain direct-conversion receiver with ultra low power consumption.

In order to address the aforementioned issues, an ultra low power, yet low noise and high gain direct-conversion receiver is demonstrated in this paper at 60GHz. One transconductance mixer is designed with a compact quadrature-hybrid to achieve the high gain and ultra low power consumption. The UMC standard 65nm

CMOS process is deployed for the chip tapeout with 0.34mm^2 chip area. The measurement of the fabricated 60GHz CMOS direct-conversion receiver shows 8mW power consumption, the minimum single-side-band (SSB) noise figure (NF) of 4.9dB, and the maximum power conversion gain of 55dB.

II. ULTRA-LOW POWER DESIGN OF 60GHz CMOS DIRECT-CONVERSION RECEIVER

The building blocks of one typical direct-conversion receiver include LNA, mixer and VGA. In the following, we illustrate the ultra low power 60GHz CMOS direct-conversion receiver design from each building block starting from the LNA.

Fig. 1: Circuit schematic of low-power LNA design with high-Q dual-layer inductor for matching

A. 3-Stage LNA with High- Q Dual-layer Inductor

LNA determines the overall NF of receiver. To achieve low NF and high gain further with low power, one needs to minimize transistor size and also to realize high-Q passive for low-loss matching. The schematic of the single-ended 3-stage LNA is shown in Fig.1a. Common-source(CS) with inductive-degeneration topology is used for M1 to have a lower NF in the first stage, and CS without

degeneration is used for M2 and M3 to have higher gain. The current consumption of LNA can be reduced by the transistor size reduction [3]. Note that in 60GHz low power LNA design, large inductance value is required in the matching network, which cannot be achieved with T-line based structure. Thus high-Q inductor design is need at 60GHz to reduce the loss of matching network. In order to further improve the Q-factor of matching network, dual-layer inductor is deployed in this paper. As shown in Fig.1b, the aluminum-layer (AL) is stacked on the top most copper layer (M6) in the inductor design. As verified by the EM simulation (ADS Momentum) results in Fig.1c, the Q of dual-layer inductor (15.5) is almost 50% higher than the one (10.5) of the single-layer inductor on M6 at 60GHz when using the UMC standard 65nm CMOS process. The post-layout simulation (Cadence Spectre) shows that the proposed LNA has 12dB gain and 4.2dB NF, and the measured power consumption is 5.4mW.

B. Transconductance Mixer with Compact Quadrature Hybrid Coupler

As the second key building block of receiver, the design of down-conversion mixer affects the receiver performance such as conversion gain, NF and power consumption. Conventionally, gilbert cell mixer is widely used for its compact size. As all transistors operate in the saturation region, each gilbert cell mixer consumes relatively large power at around 18mW at 60GHz [4]. Moreover, a large LO voltage swing is required for the Gilbert mixer to enable an effective mixing, which further results in excessive power dissipation in LO driver stages. On the contrary, transconductance mixer [5] has much smaller power consumption, as transistors are biased in the sub-threshold region. As such, transconductance mixer is more suitable for low power design. However, one disadvantage of transconductance mixer is the requirement of quadrature hybrid coupler which may consume large chip area [6]. In this paper, a double balanced transconductance mixer that incorporates RF and LO signal on-chip combining is presented (Fig.2) for 60GHz application.

Particularly, a compact $160 \times 200 \mu\text{m}^2$ quadrature hybrid coupler is proposed to reduce the chip area with 9 times reduction than the meander-line coupler in [6]. The EM simulation results (ADS Momentum) of the proposed quadrature hybrid coupler are given in Fig.3a. It is shown that all ports of coupler are matched to 50Ω impedance, and the RF/LO isolation is more than 20dB from 20GHz to 100GHz. As Fig.3b shows, the magnitude and phase mismatch between Port 2 and Port 3 are less than 0.5dB and 0.5Deg in the frequency range of interest (58~67GHz), respectively. After applying the transconductance mixer with the proposed compact quadrature-hybrid coupler, both the chip area and power of mixer are largely reduced. The post-layout simulation (Cadence Spectre) shows that the proposed mixer offers 6dB conversion gain and 10dB

Fig. 2: Circuit schematic of low-power transconductance mixer design with compact quadrature hybrid coupler

Fig. 3: (a) S-parameter of quadrature hybrid coupler; and (b) Magnitude and phase mismatch between Port 2 and Port3 of quadrature hybrid coupler

SSB NF, and the measured power consumption is 0.5mW.

C. VGA with Modified Cherry-Hooper Amplifier

A modified Cherry-Hooper amplifier is applied to in the design of main amplifier stage with source-follower feedback and an additional feedback resistor for gain enhancement. Firstly, it has improved power efficiency because high gain-bandwidth product can be provided without the extra supply voltage. Secondly, there is no additional chip area needed for inductively peaked gain stages with active or passive inductors. [7] As such, both power and chip-area efficiency can be achieved for the receiver. The post-layout simulation (Cadence Spectre) shows that the proposed VGA offers 38dB gain and 50dB tuning range, while 40dB gain tuning range is achieved via adjusting VC and 2mW power is consumed in the measurement.

III. MEASUREMENT RESULTS

The 60GHz direct-conversion receiver occupies 0.34mm^2 chip area, of which the die photo is shown in Fig.4a. The receiver chip is wire-bonded to an open cavity package for the testing purpose. As shown in the

Fig. 4: (a) Die photo of proposed receiver; and (b) Measurement Setup

measurement setup in Fig.4b, all the power and control pins are connected to the PCB and the RF, LO and IF ports are connected through the CASCADE Microtech Elite-300 probe station. Agilent PNA-X Network Analyzer N5247A is used for the conversion gain, NF and S-parameter measurement. Note that cold-source method is utilized in the NF analysis.

The receiver operates with 1V power supply with merely 8mW power consumption excluding testing buffer. LNA, mixer and VGA consume 5.5mW, 0.5mW and 2mW power according to the measurement, respectively. The measured conversion gain, NF and input S11 are shown in Fig.5. The maximum input S11 of -8dB implies good power matching at the receiver input.

Fig. 5: Measured results: conversion gain, NF and input S11 of the designed receiver

As a summary, the proposed 60GHz CMOS receiver is compared to the state-of-the-art direct-conversion receivers in CMOS processes at 60GHz. Note that LO signals are mainly from external sources except [8] from internal. For an effective and fair comparison, only the maximum gain and the minimum NF are listed, and the receiver power is shown excluding the signal generation circuit (LO) and output buffer. Table I shows the power consumption of receiver building blocks among which LNA, Mixer and VGA consumes 5.4mW, 0.5mW and 2mW, respectively. The overall 8mW power of the proposed receiver is 3~6 times lower than all the rest receiver designs at 60GHz. Moreover, compared to the previous works in [1], [2], [8], the proposed receiver shows the highest conversion gain, best NF and smallest chip area.

TABLE I: STATE-OF-THE-ART 60GHz CMOS RECEIVER PERFORMANCE COMPARISON

Parameters	This work				[2]	[8]	[1]
	LNA	Mixer	VGA	Overall			
Gain(dB)	12*	6*	38*	55	60	30	18
NF(dB)	4.2*	10*	-	4.9	3.9	7.1	9
Power(mW)	5.4	0.5	2	8	20	38.8	50
Supply(V)	1				1	1.2	1.8
LO	-	-	-	Ext	Ext	Int	Ext
CMOS Process	65nm				65nm	90nm	130nm
Chip Area(mm ²)	0.1	0.18	0.02	0.34	0.2	1.4	1.2
* indicates post-layout simulation results, and all other are measured results.							

IV. CONCLUSION

An ultra low power direct-conversion receiver is designed and fabricated in 65nm CMOS process for V-band 60GHz applications. The power consumption of proposed receiver is significantly reduced to 8mW from low-power designs of each component such as LNA, mixer and VGA. The proposed 60GHz direct-conversion receiver is fabricated in the UMC standard 65nm CMOS process with 0.34 mm² chip area. The measured results show 8mW power, the minimum SSB NF of 4.9dB and the maximum power conversion gain of 55dB.

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