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## Design, Modeling and Simulation of an Anchorless Nano-Electro-Mechanical Nonvolatile Memory

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**Abstract.** Non Volatile Memories (NVMs) based on a storage layer, like FLASH, suffer from poor retention at high temperature, high voltage writing, and wear out while cycling. This paper presents the structure, operation and modeling details of a new NVM based on nano-electromechanical memory (NEM) cell having two stable mechanical positions and actuated by electrostatic forces. Permanent retention is obtained by adhesion forces only, eliminating the leakage observed in all types of storage layers. First part of the work focus on the introduction of single cell of NEM based NVM structure and operation. The second part of the work focus on NEM based NVM modeling and behavior implementation with *Verilog-A* compact modeling and testing in *Cadence* environment. The results verify the correct functionality and scalability of the new NEM cell. With the anchorless shuttle, the design is highly eased and scalable, compared to standard anchor based NEM structures.

**Keywords:** Non Volatile memories (NVMs), Nano-electromechanical (NEMs), *Verilog-A* modeling.

### 1. Introduction

With CMOS scaling, the MOSFET threshold voltage has not been reduced as aggressively as the gate length due to the increase in subthreshold leakage. As a result, scaling of the power supply voltage has also slowed down in the most recent CMOS nodes for maintaining high performance. Thus, power density has emerged as a major challenge for continued MOSFET scaling [1]. Therefore, alternative transistor designs that can achieve steeper switching behavior than a MOSFET have been proposed to alleviate this issue [2]–[3]. However, any CMOS or CMOS like technology will have a lower limit in energy per operation due to off-current ( $I_{OFF}$ ). To overcome this limit, nano electromechanical (NEM) switches have been investigated for digital logic applications [4]–[7] because they ideally offer zero  $I_{OFF}$  and perfectly abrupt switching behaviour. In principle, the operating voltage of a NEM switch (and therefore  $V_{dd}$ ) can be reduced down to the supply voltages of CMOS circuits providing very low active power consumption. In addition to low-power digital logic applications, nano electromechanical field-effect transistors (NEMFETs) have also been proposed for analog-circuit applications such as resonators and sensors [8]. The motion of the mechanical gate (or body) changes the equivalent gate-oxide thickness and, hence, the transistor current so that a mechanical signal can be effectively converted into an electrical signal with high transduction efficiency. As the channel length of MOS transistors approaches the nano-dimensions, the control of short channel effects becomes a great challenge. As a result, the scaling of traditional memory cells such as the 6T SRAM, DRAM, or flash is made difficult because of their tight requirements on static leakage, and immunity to process variations and noise. NEMS-based memories have been suggested as promising candidates for high density NVM exceeding 1Tb/in<sup>2</sup> [9].

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Low density NEMS non-volatile memories with low power consumption have already been reported, where the electrostatic actuation of metal-metal switches is used with CMOS-compatible voltages [10]-[12]. The current mainstream of NVM is based on FLASH technology [13]-[14]. However, memories based on a storage layer, like FLASH, suffer from poor retention at high temperature, high voltage writing, and wear out while cycling. To explore novel NEMS based NVMs, the demand for accurate modeling of memory cells behaviour with *Verilog-A* has increased. *Verilog-A* is a popular language for compact model development. *MATLAB* is also frequently used for compact model development, due to its ease of use and powerful data manipulation and plotting routines. However, *MATLAB* models are not compatible to circuit simulators. *Verilog-A* is almost as easy to use as *MATLAB*, and it can be used directly in circuit simulators – as well as in parameter extraction software, which provides methods for handling measured data. *Verilog-A* is supported in a number of commercial simulators and parameter extraction tools, as well as in proprietary simulators of several semiconductor companies.

This paper presents behavioural descriptions and a *Verilog-A* model of a new anchorless NEM memory cell [18] having two stable mechanical positions actuated by electrostatic forces. The rest of this paper is organized as follows. Section 2 presents the new memory cell structure and operational details. Analytical modeling of the electromechanical behaviour describing the cell behaviour and a *Verilog-A* description of the new NEM memory cell are explained in section 3. Simulation results supporting the device behaviours are presented in section 4. Finally, conclusions are offered in section 5.

## 2. The Anchorless Shuttle Memory

Figure 1 presents the structure of a new nano-electromechanical memory cell, having two stable mechanical positions and actuated by electrostatic forces. Permanent retention is obtained by adhesion forces only, eliminating so leakage observed in all types of storage layers. The core of the memory cell is an anchorless metal shuttle, which is placed inside a cavity and vertically switches from one fixed electrode to another pair of fixed electrode. A double air-gap geometry ensures that the shuttle electrode is actively switched. Memory detection is ohmic, with an ideally large ratio between ON and OFF levels. Metals used are TiN or TaN, both of them having ideal electro-mechanical contact properties: hardness, low wear, no native oxide, and excellent thermal stability. Gravity is found to be negligible at this scale; and a free flying electrode is a very robust, compact and scalable design, targeting low-cost, high-density and high-temperature non-volatile memory applications.

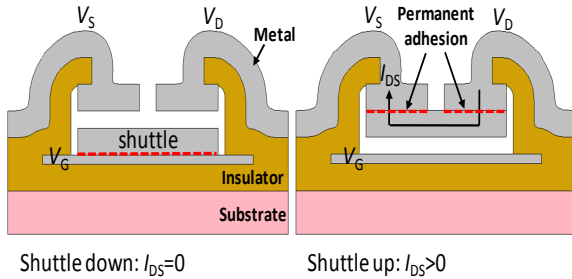


Fig. 1: Two bistable states of the NEM non-volatile memory with a double air gap and a free flying shuttle. (When the shuttle is down (left), no current can flow from drain to source. In the up state (right), the shuttle will short drain and source electrodes. Switching occurs when the electrostatic actuation overcomes adhesion forces.)

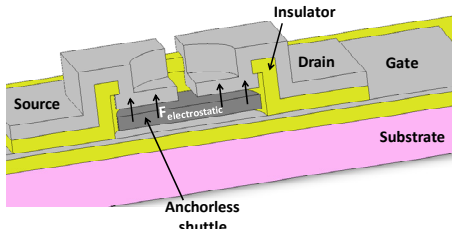


Fig. 3: 3D sketch of the anchorless non-volatile memory cell.

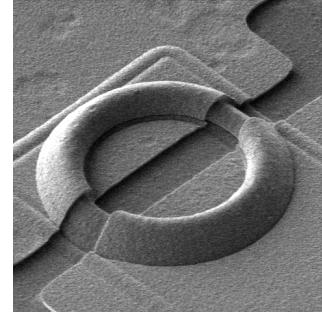


Fig. 2: Experimental circular test structure. Two metal electrodes (source and drain) are visible. A circular guiding pod is defined all around the circular shuttle to provide lateral guiding of the free shuttle.

TABLE I. Operating principle of the shuttle NVM device

Operation	Conditions	Remark
Switching down	$V_D = V_S = 0$ $V_G = V_P$	$V_P$ : Pull-out voltage, $F_{\text{electrostatic}} > F_{\text{adhesion}}$
Switching up	$V_D = V_S = V_P$ $V_G = 0$	Switching to both drain and source. Symmetric switching up/down (hysteresis)
Read	$V_D = V_R$ , $V_S = 0$ $V_G = 0$	$V_R$ : Read voltage ( $V_R \ll V_P$ ), Dow-state: $I_{DS} = 0$ , Up-state: $I_{DS} > 0$ , $I_{DS} \approx V_{DS} / 2 \cdot R_C$
Hold	$V_D = V_S = V_G = 0$	Non-volatility: adhesion increases with temperature

The shuttle memory cell is based on the commuting of a free standing (flying) electrode between a bottom fixed electrode (Gate) and two anchored electrodes (Drain and Source). Forces acting on the shuttle are (i) the electrostatic force, (ii) adhesion forces between the shuttle and fixed electrodes, (iii) damping forces during transients, and (iv) the gravity. No elastic anchors are used, as the gravity force is found to be negligible compared to adhesion forces (at least 4 decades, for typical designs). An anchorless design is very advantageous, as it makes the NEMs memory extremely scalable and it eliminates many causes of failure or operation drifts (such as beam fatigue, residual stress, device to device mismatch etc.) and facilitates cell design and modeling. Switching occurs when the electrostatic force applied to the shuttle overcomes adhesion force. A DC voltage ( $V_{DC}$ ) applied to the gate electrode will move the shuttle down (assuming  $V_D=V_S=0$ ), while a DC voltage applied to both drain and source ( $V_D=V_S=V_{DC}$ ) will move the shuttle up (assuming  $V_G=0$ ). Memory reading is done by passing a small current between drain and source (OPEN or SHORT). Reading is bidirectional to ease circuit design. Figure 2 shows the test structure image of the proposed NEM NVM device and Fig. 3 shows the NEM cell in 3D sketch. The NEM cell switching behaviour is summarized in Table I.

### 3. Electro-mechanical modelling of the Shuttle NVM device

#### 3.1. Mechanical modeling

The model presented in this study describes a transition from the UP-state (the shuttle being stucked to both drain and source) to the DOWN-state (the shuttle being stucked to the gate). The separation slit between drain and source electrodes is considered to be negligible, compared to the shuttle area. Similarly, fringing fields are neglected in a first approach. Therefore, the electrostatic force applied to the shuttle (UP-state) towards the gate is expressed as:

$$F_{elec}(x=0) = \frac{1}{2} \cdot \frac{\epsilon_0 \cdot A \cdot (V_G - V_{D/S})^2}{(2d_{gap})^2} = \frac{1}{8} \cdot \frac{\epsilon_0 \cdot A \cdot V_G^2}{d_{gap}^2} \quad (1)$$

The parameter A represents the shuttle planar area,  $2d_{gap}$  the vacuum gap (double-air gap structure, see Fig. 1),  $\epsilon_0$  the permittivity of vacuum and  $x=0$  the initial position of the shuttle. As the shuttle is stucked to drain and source, then  $V_{shuttle}=V_D=V_S=0$ . Adhesion forces between the shuttle and fixed electrodes in Eqn (2) are given in terms of adhesion energy  $\Gamma$  and distance  $x$  between the two surfaces, where  $F_{adh}=0$  if  $x>d_{vdw}$  and  $d_{vdw}$  is approximated to 5nm. Model parameter  $\alpha$  represents the ratio between real to apparent contact area. This approximation is only valid for smooth surfaces. The exact *Force–Energy* adhesion plot is highly experimental and usually extracted from atomic force microscopy (AFM) *Force–Stiction* plots.

$$F_{adh}(0 < x < d_{vdw}) = \frac{2\Gamma \cdot A \cdot \alpha}{d_{vdw}} \cdot \frac{d_{vdw} - x}{d_{vdw}} \quad (2)$$

To confirm this value, AFM scan of a smooth physical vapor deposition (PVD) of tantalum nitride (TaN) layer was conducted. It was found (see Fig. 4) that the surface is very smooth and ideal for electro-mechanical contacts. Furthermore, PVD TaN depicts ideal properties in terms of low residual stress and stability at high temperature. Adhesion energy of 33mJ/m<sup>2</sup> is extracted, which correspond to an adhesion force of  $F_{adh}(x=0, \alpha=1)=13\text{kN/m}^2$ , in good accordance with other published reports. The switching voltage ( $V_p$ ) is the gate voltage at which the electrostatic force equals the adhesive fore. Thus, from (1) & (2),  $V_p$  can be expressed by

$$V_p = 4d_{gap} \cdot \sqrt{\frac{\Gamma \cdot \alpha}{d_{vdw} \cdot \epsilon_0}} \quad (3)$$

#### 3.2. Electrical modeling

Although mechanical motion tends to dominate the switching delay of a single cell, the overall circuit switching delay is affected by the electrical delay as well. Predicting the amount of time required for a channel in the *on*-state to discharge a load capacitance requires accurate modeling of both the *on*-state resistance and the capacitances of the device. The *on*-state resistance is comprised of the resistance of the channel ( $R_{ch}$ ), the resistance of the contacts between the channel and the source/drain ( $2R_{con} = R_{CS} + R_{CD}$ ) and source/drain resistances ( $2R_{sd}$ ). Following [7], the resistance of the contact at each side of the channel depends on the conditions under which the contact is made and the properties of the material as,

$$R_{con} = \frac{4\rho\lambda}{3A_r} \quad (4)$$

where,  $\rho$  is the resistivity of the contacting material,  $\lambda$  is the mean free path of electrons in the contact material, and  $A_r$  is the effective contact area as given by,

$$A_r \approx \frac{F_{elec}}{\xi H} \quad (5)$$

where,  $H$  is the hardness of the material and  $\xi$  is the deformation coefficient. The electrode resistances can be simply approximated as

$$R_{sd} = \frac{\rho L_{sd}}{H W_{sd}} \quad (6)$$

where, the symbols  $\rho$ ,  $L$ ,  $H$ , and  $W$  represent the sheet resistance, length, thickness, and width of the electrode. The values of these electrode resistances are obviously highly material dependent. The electrical delay is also determined by the load capacitance seen by the device. In our intended VLSI applications the load capacitance is dominated by wire parasitics and the load presented by other devices. The load presented by the devices consists of many parasitic capacitors, but the largest of these are the capacitors formed by the air gap between the gate and the shuttle across which the device is actuated ( $C_{Gsh}$ ), and the overlap capacitance between the gate and the source/drain electrodes ( $C_{GS}$ ) and ( $C_{fr}$ ).  $C_{Gsh}$  and  $C_{GS}$  can be modeled as standard parallel plate capacitors,

$$C_{Gsh} = \frac{\epsilon_0 A_{ov}}{(2d_{gap} - x)}, C_{GS} = \frac{\epsilon_0 A_s}{(2d_{gap} - x)} \quad (7)$$

and fringe capacitance  $C_{fr}$  can be modeled as

$$C_{fr} = \frac{2\epsilon_0 W}{\pi} \ln \left( 1 + \frac{t_{gate}}{2d_{gap}} \right), \quad (8)$$

where,  $t_{gate}$  is the thickness of the gate electrode. Figure 4 and Fig.5 present the NEM NVM model implemented in *Verilog-A*, capturing the device's electro-mechanical behaviour as well as its parasitic resistors and capacitors. Listing 1 describes the sample *Verilog-A* model of the NEM NVM cell behaviour.

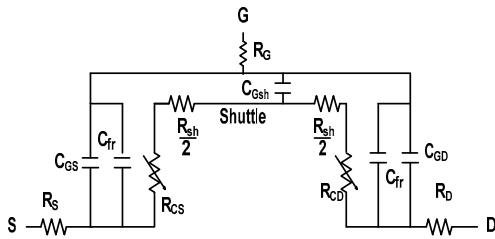


Fig. 4: Electrical equivalent in up-state.

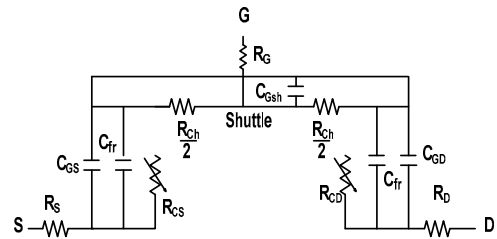


Fig. 5: Electrical equivalent in down-state.

**Listing 1.** Sample *Verilog-A* description of the NEM memory cell.

```
//Device definition
module NEMcell3T(S,D,G) ;
  inout S, D, G;
  electrical S, D, G, n1,n2, n3, n4, n5, n6 ;
  branch (S, n2) res1;

//Shuttle dimension definition
parameter real L = 2u from [0 : inf] ;
parameter real W = 2u from [0 : inf] ;
real Fel, Ar, RG, Rsh, Rcon_on, Rcon, Rcon_off;

// Initial resistance values calculation
Rsh= shuttle_resistivity * L / (tsh * W);
Rcon_on= 4.0 * cont_resistivity * lambda / (3*Ar);
Rsd= source_resistivity * Ls/(tsource*W);
Vp = sqrt ((8*dgap*dgap* Fa)/(e0));

analog begin
  V(res1) <+ Rsd * I(res1) ; // represents R_S in Fig 4,5
  I(cap1) <+ ddt(CG_S * V(cap1)); // represents C_GS in Fig 4,5
end
if ((0 <= V(G) < Vp) && (V(S) == 0) && (V(D) == 0) ) begin
  Rcon= Rcon_on;
end
else if ((V(G) >= Vp) && (V(S) == 0) && (V(D)
== 0) ) begin
  Rcon= Rcon_off;
end
endmodule
```

## 4. Results and Discussion

The device default parameters used for simulations are as follows:  $L=2\mu\text{m}$ ,  $W=2\mu\text{m}$ ,  $t_{\text{sh}}=0.3\mu\text{m}$ ,  $d_{\text{gap}}=0.1\mu\text{m}$ , TaN metal electrodes and shuttle, shuttle resistivity= $131\text{nm}$ ,  $F_a=13\text{k}$ . The developed model is implemented in *Verilog-A* and tested in *Cadence* environment. The minimum switching voltage  $V_P$  needed to pull the shuttle out of adhesion is extracted. Simulation results are plotted in Fig. 6 for various  $\alpha$ -parameters ratio. The following observations are important. First, gravity is at least 4 to 5 decades smaller than the adhesion force needed to initiate switching, demonstrating the robustness of the anchorless design. Second, adhesion force will very quickly decrease after pull-out, while electrostatic force will increase. That means the electrostatic force must be the highest to lift-off the shuttle. Last, all 3 forces (electrostatic, adhesion, and gravity) have similarly a linear dependence to the shuttle surface  $A$ . That means  $V_P$  doesn't depend from the actuation area  $A$ . This is an unusual result for most electrostatic MEMS devices, but of great interest for device scaling. Variation of drain current with gate voltage for different adhesive forces between the electrodes and shuttle is presented in Fig. 7. As the adhesive force reduces, the gate voltage required for switching the shuttle will reduce and no effect on the  $I_{\text{ON}}/I_{\text{OFF}}$  ratio. Variation of ON state resistance with gate voltage for different gap thickness is presented in Fig. 8. This is due to the change in the contact area, which is the dominating component in the total ON resistance. Figure 9 shows the variation of drain current with shuttle length for different  $V_G$ . With the increase in both shuttle length and gate switching voltage, drain current can be enhanced.

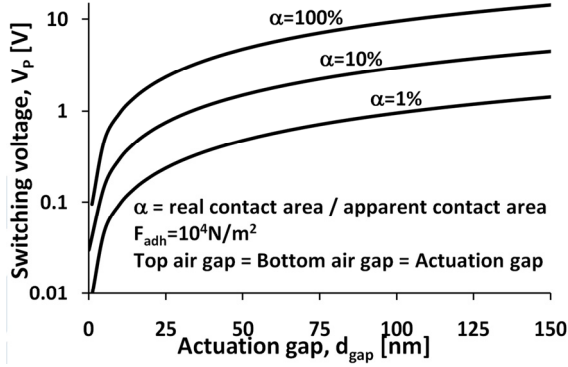


Fig. 6: Switching pull-out voltage  $V_P$  (log-scale) vs. actuation gap  $d_{\text{gap}}$  for various values of the real to apparent contact area ratio ( $\alpha$ -parameter). Sub-25nm actuation gaps are typically needed for low-voltage actuation. Switching voltage does not depend on shuttle area  $A$ .

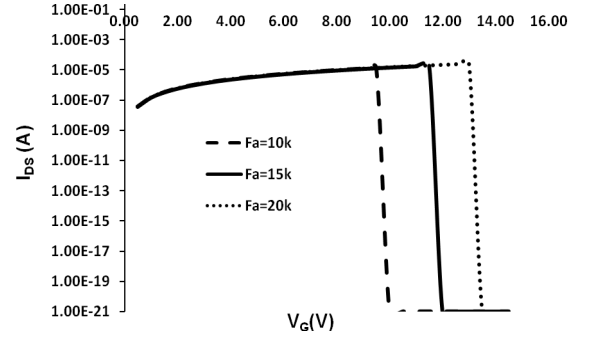


Fig. 7: Plot of  $I_{\text{DS}} - V_G$  of the shuttle based NEM NVM cell for different Adhesive forces ( $V_{\text{DS}}=0.2\text{V}$ ).

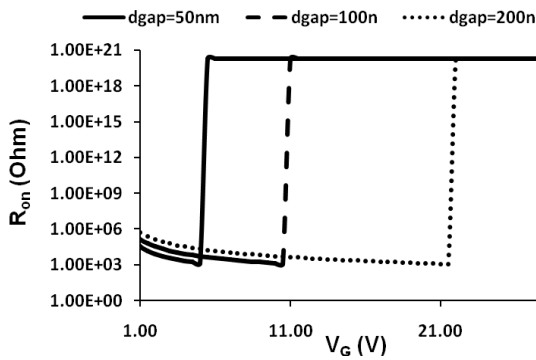


Fig. 8: Plot of  $R_{\text{on}} - V_G$  of the shuttle based NEM cell for different actuation gap thickness ( $V_{\text{DS}}=0.2\text{V}$ ).

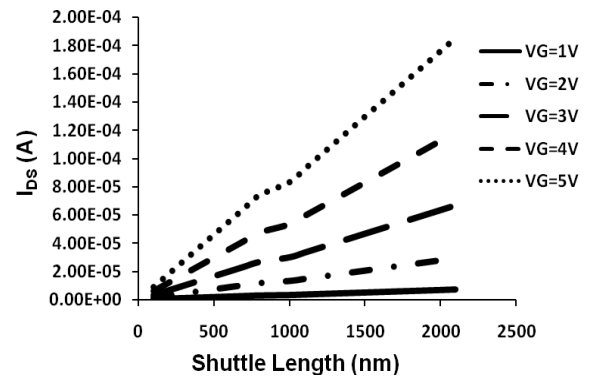


Fig. 9: Plot of  $I_{\text{DS}}$  vs shuttle length cell for different  $V_G$ .

## 5. Conclusion

In this paper, a new anchorless, shuttle based NEM memory cell is presented. The cell electro-mechanical behavior has been implemented with *Verilog-A* and verified in *Cadence* environment. The effect of drain and gate potentials on drain current is examined in combination with scaling down in shuttle dimensions. With the anchorless shuttle, the design is highly eased and scalable, compared to standard

anchor based NEM structures. With scaling down in the actuating gap thickness, the minimum gate voltage required for switching the shuttle gets reduced with an increase in  $I_{ON}/I_{OFF}$  ratio. Further improvements can be combining the shuttle memory with a NEMs based logic.

## 6. References

- [1] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE J. Solid- State Circuits*, vol. 40, no. 9, pp. 1778–1786, Sep. 2005.
- [2] A. M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M. J. Declercq, P. Renaud, C. Hibert, P. Fluckiger, and G. A. Racine, "Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal over-gate architecture," *Proc. Int. Symp. on Quality Electronic Design*, pp. 496–501, Mar.2002
- [3] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than  $kT/q$ ," *IEEE International Electron Devices Meeting Tech. Dig.*, pp. 289–292, Dec.2002.
- [4] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, and H.-S. P. Wong, "Design considerations for complementary nano electromechanical logic gates," *IEEE International Electron Devices Meeting Tech. Dig.*, pp. 299–302, Dec.2007
- [5] H. Kam, T.J K.Liu, V. Stojanovic, D. Markovic, and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Trans. Electron Devices*, vol. 58, no. 1,pp. 236-250, Jan. 2011.
- [6] H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon, and T.-J. K. Liu, "Design and reliability of a MEM relay technology for zero-standby-power digital logic applications," *IEEE International Electron Devices Meeting Tech. Dig.*, pp. 809–812, Dec.2009
- [7] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T. J. K. Liu, D. Markovic, E. Alon, and V. Stojanovic, "Demonstration of Integrated Micro-Electro- Mechanical Relay Circuits for VLSI Applications," *IEEE J. Solid- State Circuits*, vol. 46, no. 1, pp. 308-320, Jan. 2011.
- [8] D. Grogg, D. Tsamados, N.-D. Badila, and A. M. Ionescu, "Integration of MOSFET transistors in MEMS resonators for improved output detection," *Proc. 18th Int. Solid-State Sens. Actuators Conf. Tech. Dig.*, pp. 1709–1712, June 2007
- [9] M. Despont, U. Drechsler, R. R. Yu, B. H. Pogge, and P. Vettiger, "Wafer-Scale Micro device Transfer/Interconnect: From a New Integration Method to its Application in an AFM-Based Data-Storage System ," *IEEE Journal of MEMS*, vol.13, Issue 6,pp. 895-901, 2004.
- [10] M. A. Beunder, R. V. Kampen, D. Lacey, M. Renault, C. G. Smith, "A new embedded NVM technology for low-power, high temperature, rad-hard applications," *IEEE Non-Volatile Memory Techn. Symp.*, pp. 65-68, Nov.2005.
- [11] J.-M. Sallese and D. Bouvet, "Principles of space-charge based bi-stable MEMS: The junction-MEMS," *Sensors and Actuators A: Physical*, vol. 133, no. 1, pp. 173–179, Jan. 2007.
- [12] N. Abele, A. Villaret, A. Gangadharaiah, C. Gabioud, P. Ancey, and A. M. Ionescu, "1T MEMS memory based on suspended gate MOSFET," *IEEE International Electron Devices Meeting*, pp. 509–512, Dec.2006.
- [13] G. Forni, C. Ong, C. Rice, K. McKee, and R. J. Bauer, "Flash memory applications," *Nonvolatile Memory Technologies With Emphasis on Flash*, pp. 19–62, Wiley, IEEE Press,2008.
- [14] J. J. Chen, N. R. Mielke, and C. C. Hu, "Flash memory reliability," *Nonvolatile Memory Technologies With Emphasis on Flash*, pp. 445–590, Wiley, IEEE Press,2008.
- [15] M. Mierzwinski, P. O'Halloran, B. Troyanovsky, R. Dutton, "Changing the paradigm for compact model integration in circuit simulators using Verilog-A," *Proc. of the Nanotechnology Conference and Trade Show*, vol. 2, pp. 376–379, Feb. 2003.
- [16] G. J. Coram, "How to (and how not to) write a compact model in Verilog-A," *Proc. IEEE International Behavioral Modeling and Simulation Conference*, pp.97-106, Oct.2004.
- [17] Verilog-AMS Language Reference Manual, version 2.2, Accellera, 2004.
- [18] V. Pott, G. L. Chua, V. Ramesh, J. T. M. Lin, and T. T. Kim, "The shuttle nano-electro-mechanical non-volatile memory," *IEEE Trans. Electron Devices*, 2012 (*In press*).