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Miniaturized 3-bit Phase Shifter for 60-GHz Phased-Array in 65-nm CMOS Technology

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***Abstract*—The paper presents a compact 3-bit 90 °phase shifter for phased-array applications at the 60-GHz ISM band (IEEE 802.11ad standard). The designed phase shifter is based on reflective-type topology using the proposed reflective loads with binary-weighted digitally-controlled varactor arrays and the transformer-type directional coupler. The measured eight output states of the implemented phase shifter in 65-nm CMOS technology, exhibit phase-resolution of 11.25 °with an RMS phase error of 5.2 °. The insertion loss is 5.69 ±1.22 dB at 60-GHz and the return loss is better than 12 dB over 54-66 GHz. The chip demonstrates a compact size of only 0.034 mm^2.**

***Index Terms*—Digital control, reflective-type phase shifter (RTPS), millimeter-wave.**

I. Introduction

PHASED-ARRAYS [1]-[4] for the 60-GHz ISM band applications require the variable phase shifters to have a good tradeoff between the low insertion loss and the fine phase-resolution. Two types of phase shifters, including reflective-type phase shifter (RTPS) [1], [5], and switched-type phase shifter (STPS) [3], [6], are widely employed in 60-GHz phased-arrays to provide fine phase-resolution of 22.5 ° and even 11.25 ° with insertion loss of around 12-15 dB for 360 ° phase shifting range.

The RTPS is capable to output continuous phase shift according to analog tuning voltages, which are usually provided by digital-to-analog converters (DACs) for the digital control purpose. Since the phase shift of RTPS is not linear with respect to the tuning voltages [1], [5], [7], the resulted phase-resolution relies heavily on the resolution and accuracy of these DACs. In [1], a 6-bit DAC was co-designed on-chip to tune the 180 ° phase shifter and achieved 4-bit (11.25 °) phase-resolution. On the other hand, the STPS has the intrinsic advantages of digital control due to its topology of cascaded switching networks [3], [6]. However, the STPS with finer phase-resolution needs more cascaded stages that lead to higher insertion loss as well as larger circuit size. Recently in [6], a 60-GHz 5-bit STPS was reported and achieved an average insertion loss of 14.6 dB with core circuit size of 0.34 mm^2. But insertion loss of ~7.3 dB and size of ~0.17 mm^2 of the STPS in [6] are contributed by the 3-bit 90 °phase shifter.

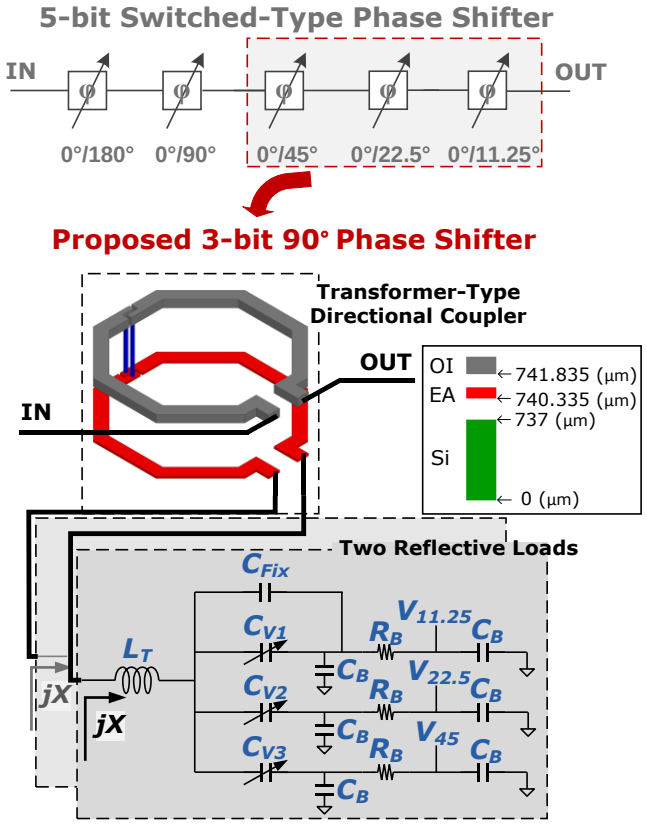

Fig. 1: Conventional 5-bit STPS and the proposed 3-bit 90 phase shifter.

In this paper, a concept of switch-less digital reflective loads by using binary-weighted digitally-controlled varactor arrays is proposed for phase shifter as shown in Fig. 1. A 60-GHz 3-bit 90 °phase shifter based on the proposed concept is developed. In contrast to the conventional analog RTPS in [1], [5] and [7], the implemented phase shifter is directly controlled by digital bits instead of analog tuning voltages. Comparing to the STPS, the proposed phase shifter achieves insertion loss and size reductions.

II. Circuit Design

A. Topology

The proposed phase shifter comprises of a 3-dB transformer-type directional coupler and two identical

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reflective loads as shown in Fig. 1. Since it is of RTPS topology, the phase shift is varying according to the phase angle of the reflection coefficient [7]:

$$\Gamma_{Load} = \frac{jX - Z_0}{jX + Z_0}, \tag{1}$$

where X is the reactance of the reflective loads with the minimum and maximum values denoted as $X_{\min}$ and $X_{\max}$, respectively. The characteristic impedance of the coupler is Z_0. Thus, the phase shift and the total phase-shift range are

$$\varphi_{out} = -\pi - 2\arctan\left(\frac{X}{Z_0}\right), \tag{2}$$

$$\varphi_{total} = 2\left|\arctan\left(\frac{X_{\max}}{Z_0}\right) - \arctan\left(\frac{X_{\min}}{Z_0}\right)\right|. \tag{3}$$

B. *Transformer-Type Directional Coupler*

The transformer-type directional coupler is adopted for its compactness. The size reduction is over 50% comparing to the broadside coupler in [5]. As shown in Fig. 1, the coupler uses two metal layers, colored in grey (OI) with 3.3 μm thickness and red (EA) with 0.9 μm thickness respectively. The blue traces are the metal via with length extended for better illustration. The coupler has its primary and secondary coils inter-crossed where the primary coil is firstly constructed on OI layer for half-turn, and then is routed down to EA layer for another half-turn to complete the winding trace. Meanwhile, the secondary coil is formed on EA layer first, and then crosses to complete the full-turn on OI layer. Thus, the structure is symmetrical so that the impedance looking into the four ports are expected to be the same. The optimized outer diameter is found as 69 μm with trace width of 5 μm to minimize the coupler loss while maintaining the return loss and isolation better than 15 dB. In Fig. 2, the full-wave simulation using *ANSYS HFSS V.14* shows that the transformer-based coupler achieves the total insertion loss less than 0.9 dB and the return loss and isolation better than 17 dB over 50-70 GHz. The phase balance is kept close to 90 °.

C. *Reflective Loads with the Binary-Weighted Digitally-Controlled Varactor Arrays*

As shown in the bottom of Fig. 1, the proposed reflective load comprises of three varactors C_{V1} to C_{V3} and one fixed-value capacitor C_{Fix} in shunt-connection. The L_T is a series inductor that forms a resonator together with the collective capacitances to increase the load reactance X varying range and the phase-shifting range according to (3). The C_B and R_B are biasing components with values of 1 pF and 10 kΩ respectively. The digital control function is realized by biasing the three control bits, $V_{11.25}$, $V_{22.5}$ and V_{45} to either 0 V or 1.2 V. Since each varactor has two capacitance values under alternative digital biasing, the proposed reflective load is capable of achieving eight different reactance values as well as eight phase shifts for the phase shifter according to (2). The C_{Fix} is added to compensate the overall phase error with the tradeoff of a reduced phase-shifting range. The varactor sizes are binary-weighted and the optimized design parameters are summarized in Table I.

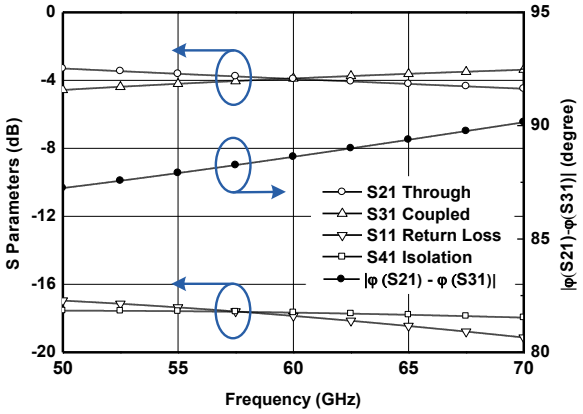


Fig. 2. Simulated performance of the transformer-type directional coupler.

TABLE I
DESIGN PARAMETERS

	Fixed Components	Variable Components		
		Size (Fingers×W/L)	Min. (fF)	Max. (fF)
C_{Fix}	17.8 fF	-	-	-
$C_{V1\text{-}min}$	-	1×1.6 μm/0.47 μm	2.47	7.4
$C_{V2\text{-}min}$	-	2×1.6 μm/0.47 μm	4.92	14.6
$C_{V3\text{-}min}$	-	4×1.6 μm/0.47 μm	9.78	28.7
L_T	110 pH	-	-	-

III. EXPERIMENTAL RESULTS

The measurement is performed on-chip using Agilent N5247A PNA-X network analyzer and Cascade Elite 300 probe station.

In Fig. 3, the die micrograph of the fabricated phase shifter is shown, where the circuit size excluding testing pads is only 0.034 mm^2.

Fig. 4 depicts the measured results of eight states over frequency range of 54-66 GHz that fully covers the 60-GHz

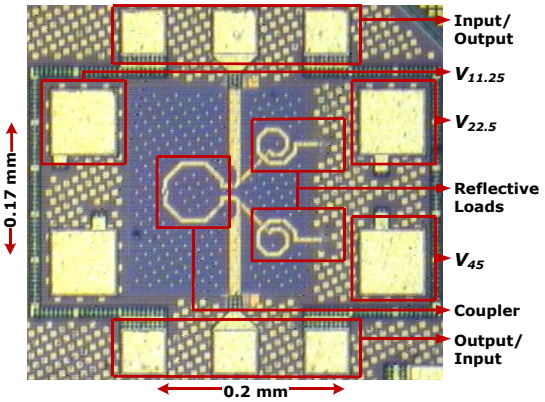
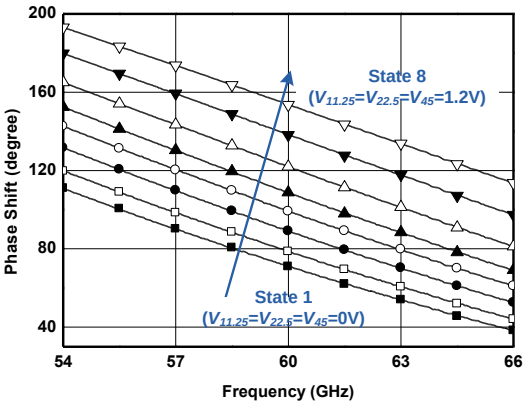
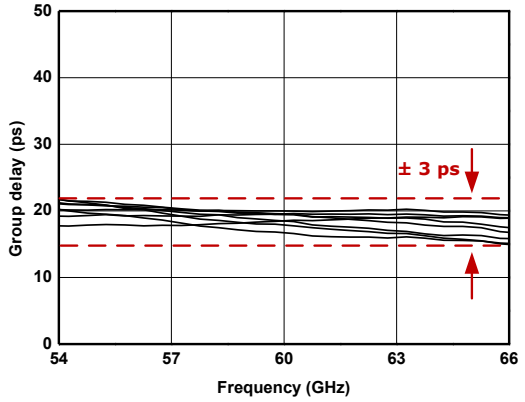


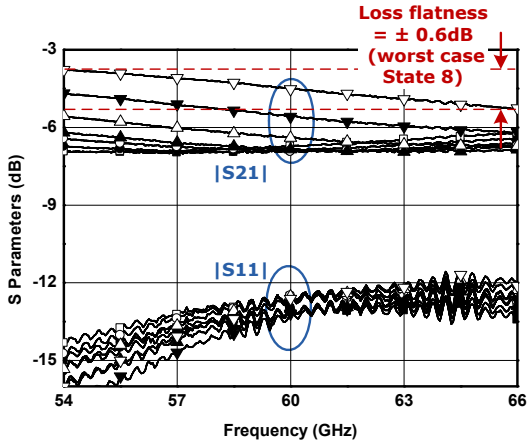
Fig. 3. Micrograph of chip die.



(a)



(b)



(c)

Fig. 4. Measured performance versus frequency: (a) phase shift; (b) group delay; (c) insertion loss and return loss.

ISM band. In Fig. 4(a), the phase shifter shows the eight output phases with phase-resolution of 11.25 °and an RMS phase error (calculated as in [6]) of 5.2 ° at 60-GHz. The measured group delays are within ±3 ps with absolute delay less than 20 ps as shown in Fig. 4(b). Fig. 4(c) depicts the insertion loss and return loss over the entire bandwidth. The worst loss flatness has a value of ± 0.6 dB and occurs in State 8. At 60-GHz, the average insertion loss is 5.69 dB with loss variation of ±1.22 dB across eight states.

Table II compares this work with other similar phase shifters. This work has the smallest circuit size and insertion loss among 90 °phase shifters. Moreover, this work is controlled directly by digital bits.

For systems requiring 360 ° phase-shifting range, switched-type 180 ° and 90 ° phase-shifting stages can be cascaded with the proposed phase shifter. The resulted 5-bit 360 ° phase shifter will have better performance than the conventional STPS, thanks to the low loss and compactness of the proposed phase shifter.

TABLE II
COMPARISON WITH OTHER SIMILAR PHASE SHIFTERS

Reference	[1]	[5]	[6]*	This work
Load Topology/ Step	RTPS/ Cont's	RTPS/ Cont's	STPS/ 3-bit	RTPS/ 3-bit
Technology	0.12-µm SiGe	90-nm CMOS	90-nm CMOS	65-nm CMOS
Freq. (GHz)	57-64	50-65	57-64	54-66
Phase-shifting range(°)	180	90	90	90
Insertion loss (dB)	6 ±1.8	6.25 ± 1.75	7.3 ±1.5	5.69 ±1.22
Return loss (dB)	-	> 12	-	> 12
DAC requirement	Yes	Yes	No	No
Size (mm^2)	0.18	0.08	0.17	0.034

* The 3-bit 90 ° phase shifter is used for comparison. The insertion loss is estimated by averaging the total insertion loss by the number of stages since the main loss is due to switch loss. The size is estimated from die photo.

IV. CONCLUSION

The miniaturized 3-bit phase shifter with switch-less digital reflective loads by using the binary-weighted varactor arrays was designed and implemented in 65-nm CMOS technology. The measured results showed that 3-bit phase-resolution has been achieved with total phase-shifting range of 90 ° covering the 60-GHz ISM band. Moreover, the characteristics of digital control, compact size and low insertion loss make the proposed design very suitable for 60-GHz phased-arrays.

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