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Triple Boundary Multiphase With Predictive Interleaving Technique for Switched Capacitor DC-DC Converter Regulation

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***Abstract*—In this paper, we propose a new technique to regulate multi-phase interleaved switched-capacitor DC-DC converters. Traditionally, SC converters are either regulated by modulating the switching frequencies directly through a voltage-controlled-oscillator or by using hysteretic control where separate control loops are used for each converter core. Achieving fast regulation by modulating VCO is difficult because it requires a high speed error amplifier and proper loop compensation. Conventional hysteretic controller achieves fast regulation, but it uses N comparators or one shared comparator that operates at N times the single phase switching frequency, where N is the level of interleaving. The proposed technique avoids these problems by using triple boundary hysteretic control, where one comparator is used for defining the reference voltage, and the other two comparators enable coarse/fine operation to achieve both fast recovery and tight regulation.**

Keywords—switched capacitor; DC-DC converter; hysteretic control; multiphase interleaving

I. INTRODUCTION

Power density, conversion efficiency and output ripple are the main considerations when designing a fully integrated switched capacitor (SC) DC-DC converter. State-of-the art SC converters achieve high power density with the aid of SOI technology and high density capacitors such as deep trench capacitors [1] and ferroelectric capacitors (Fe-Caps) [2]. These capacitors also help to reduce bottom plate losses significantly due to low bottom plate parasitic capacitances. However, to reduce the production cost, SC converters that can be built on standard CMOS processes are preferred. Therefore, circuit techniques to minimize converter losses remain a necessity. For example, the efficiency can be improved by controlling the amount of capacitance and width of switch so as to scale the bottom-plate and switching losses as the output load changes [3]. Multiphase interleaving is the dominant technique used to reduce the noise at both the input and output of SC converters. It is implemented by replacing a single SC converter with N smaller SC converters that are operated with different clock phases[4-6]. Interleaving is infeasible for SC converters using discrete components as it increases component count linearly with the level of interleaving. Fortunately, the integrated SC converters can utilize this technique to reduce noise with hardly any area and cost overhead.

Most applications require a SC converter to provide a regulated output voltage. Traditionally, by controlling a voltage-controlled oscillator (VCO), the switching frequency can be modulated to achieve regulation. This approach requires a high speed error amplifier and proper compensation must be designed to guarantee system stability. Therefore hysteretic control with one or more boundaries has becoming the more popular method due to its inherent stability and fast regulation [4],[7], [8].

In this paper, we propose a novel technique for regulating SC DC-DC converters. The proposed SC converter utilizes interleaving technique to achieve low output noise and is capable to scale the bottom plate and switching losses. Compared to standard multiphase interleaving, it reduces the number of comparators significantly, while providing only slightly degraded ripple performance. Section II gives a brief review of the standard multiphase hysteretic control, and presents the proposed regulation method. Section III presents the simulation results and conclusion is given in Section IV.

II. PROPOSED PREDICTIVE INTERLEAVED TRIPLE-BOUNDARY MULTIPHASE CONTROL

A. Multiphase Hysteretic Control

A conventional multiphase-interleaved SC converters is shown in Fig. 1. The N-level interleaved converter is regulated by N identical control loops. Each loop comprises a comparator, control logic and a set of switch drivers to control the switching activity for the respective converter core. Interleaving is implemented by applying phase shifted clocks to the comparators so that they sample and compare the output with the reference voltage at different times. For example, as clock $\phi 1$ goes high, the first comparator compares the output voltage with Vref. If Vout < Vref, the first control logic block decides that the first SC core must be switched in order to bring Vout closer to Vref. If Vout > Vref, the first converter core would remain with the current configuration to avoid delivering excessive charges to the output. The same control sequence occurs to the rest of the converter cores when their associated clocks become high. Therefore, within a switching period, $1/f_{sw}$, the output is compared to the reference voltage N times, and effectively been regulated at a frequency N times higher than f_{sw}.

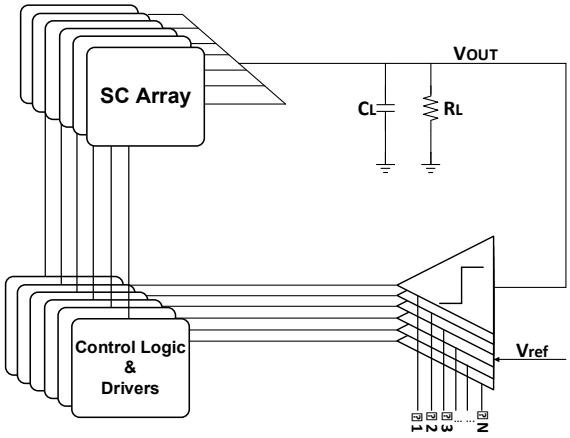

Fig. 1 Implementation of Conventional Single Boundary Multi-phase SC Converters with Hysteretic Control

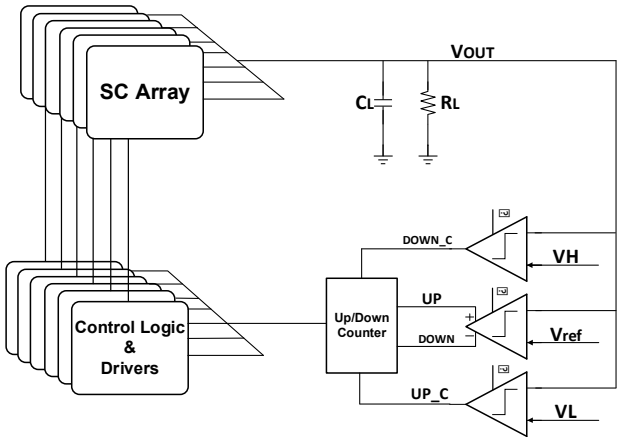

Fig. 2 Triple Boundary Multi-phase Control. The three comparators detect the crossing of the three boundaries respectively.

The use of separate control loop for each core results in control circuit complexity that increases linearly with the level of interleaving [5]. The use of multiple comparators poses additional difficulties. In practice, the multiple comparators consume more power and reduce the overall conversion efficiency. Moreover, the comparators are not exactly matched and are subjected to offsets different from each other. Therefore, each comparator effectively define a reference level different from those of other comparators, and this can degrade the output ripple performance. A solution to prevent the use of multiple comparators is to allow all converter cores to share a single comparator [7]-[9], however, this requires the comparator to operate at a frequency which is N times higher than that when multiple comparators are used.

B. Predictive Interleaving

The standard multiphase hysteretic control gives optimal output regulation at the cost of using multiple comparators or increasing comparator sampling frequency by N times. In this work, we propose a regulation method that perform less comparisons within each switching cycle, which results in sub-optimal regulation performance that, although slightly inferior to that of standard multiphase interleaving, but much better than that of using single big SC converter.

The proposed Triple Boundary Multiphase Control architecture is shown in Fig. 2. The SC converter comprises of N SC converter cores, three comparators for detecting the crossing of the three boundaries, an UP/DOWN counter that decides the number of converter cores to be switched in the following cycle, and N blocks of control logic and drivers that produce the gate signals. Fig. 3 shows the predictive interleaving used in this architecture to reduce the frequency of comparison between Vout and Vref from N to three times per cycle. Using this technique, only one single comparison between Vout and Vref is performed at the end of each clock cycle, and the comparison result is sent to a UP/DOWN counter which decides to either increase or decrease the number of converter cores that will be switched in the following cycle. The comparison results with VH and VL are used to enable coarse/fine operation, which is discussed in section II *C*. If Vout > Vref, the DOWN signal goes high, the counter counts down and the number of converter cores that will be switched in the following cycle is decreased by one. Similarly, if Vout < Vref, the UP signal goes high and the number of converter cores to be switched is increased by one.

Consider a seven-level interleaved (N = 7) SC converter. The switching of the seven converter cores can be controlled by a 3-bit signal ($B_3B_2B_1$) at the UP/DOWN counter output. Each bit controls one, two and four converter cores respectively. For example, if B1 is high, then the associated converter core SC4 is switched at $\phi 4$ during the next period. When both B1 and B2 are high, then three switching actions will be performed within the next cycle by SC2, SC4 and SC6 at $\phi 2$, $\phi 4$, and $\phi 6$ respectively. When maximum load is applied, all the three bits will go high, and the seven converter cores are switched in sequence within the switching cycle to deliver the maximum power to the output. The switching activities are made to distribute evenly in time within each clock period so as to minimize the output ripple as much as possible.

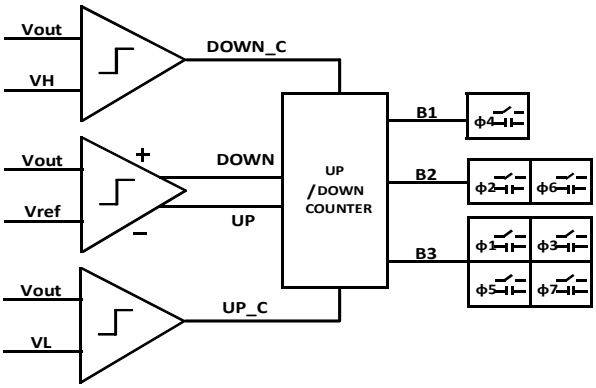

Fig. 3 Predictive interleaving

C. Triple Boundary Coarse/Fine Control

The load transient response of the standard multiphase interleaving DC-DC converter is inherently fast. By allowing every converter core to compare the output voltage with the reference, whenever there is change in load condition, the

converter core can react immediately when its respective clock signal becomes high. In our proposed design, the comparison is performed only at the end of each clock period. Therefore, coarse and fine modes control are used to help achieve the fast response to load changes and maintain tight regulation during constant load. This control is implemented with the aid of three boundaries as shown in Fig. 4.

The first control boundary corresponds to the reference voltage Vref, i.e. the desired output voltage level. The output voltage is compared to this voltage at the end of each cycle to decide the switching actions for the following cycle. During normal operation, $B_3B_2B_1$ is incremented/decremented with a minimum step size of one. This ensures small ripple at the output and is called the FINE mode control.

The second and third control boundaries VL and VH are employed to achieve fast load regulation. VL and VH denote the lower and upper boundaries that are being crossed when there is a sudden load change. When load current increases, the VL boundary may be crossed with Vout < VL, and the UP_C signal goes high, and $B_3B_2B_1$ is increased with a step size larger than one to quickly bring the output voltage back to the reference level. If there is a sudden load decrease, Vout can rise above VH, causing DOWN_C to go high and reduce the number of converter cores to be switched in the next cycle by more than one. The optimal step size of $B_3B_2B_1$ can be determined depending on the actual load condition and transient response speed requirement and etc.

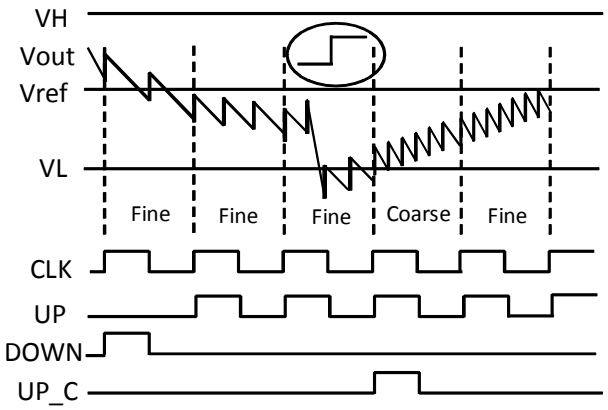

Fig. 4 Coarse/Fine Regulation

III. Simulation Results

The proposed regulation method is implemented in a 15-level interleaved voltage divider. Each converter core comprises of two identical converter units that are operated 180° out of phase, as seen in Fig. 5. Therefore there is always one of the flying capacitors that is connected between the output and the ground, and the other capacitor connected between the battery and the output node. With sufficient level of interleaving, the output buffer capacitor can be significantly reduced or eliminated. The SC converter is simulated using AMS 0.35 um CMOS process. The input voltage is 3 V and the output voltage is regulated at 1.35 V under system clock frequency of 12.5 MHz. Fig. 6 shows that the peak to peak output ripple of the proposed design is 35 mV without using the output capacitor,

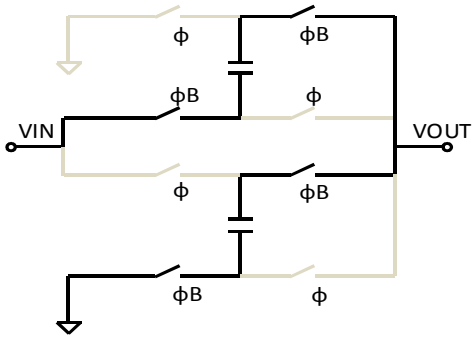

Fig. 5 Converter Core

when the load current is maintained at 1.2 mA. The ripple is slightly larger than that of using the standard multiphase interleaving control, which gives 30 mV ripple. Nonetheless, the performance is much better than that of a single phase SC converter which gives 700 mV output ripple under the same load condition.

The load transient response is simulated by changing the load current from 1 to 2 mA at t = 2 us. Fig. 7 shows that with the load change, the output voltage drops below VL and the signal UP_C goes high, causing the converter to switch from fine to coarse mode operation which is implemented by increasing the two more significant bits (A_4A_3), therefore increasing to a four-bit signal ($A_4A_3A_2A_1$) by a step larger than one. As shown in Fig. 8, when Vout falls below VL, $A_4A_3A_2A_1$ increases from 1001 (or 9 in decimal) to 1110 (or 14 in decimal), meaning that the number of SC cores that will be switched will be increased from 9 in the current cycle to 14 in the next cycle. The output voltage is brought back to the range between VL and VH within one clock cycle. Then after the fine mode operation is enabled and the number of active SC cores increases/decreases by one from cycle to cycle.

Table I shows the comparison with some of the recently published hysteretic controlled multiphase SC converters. In [4], 10 comparators are used for the 10-level interleaved SC converter. [7] and [9] use only one shared sampling comparator, which however operates at N times the single phase switching frequency.

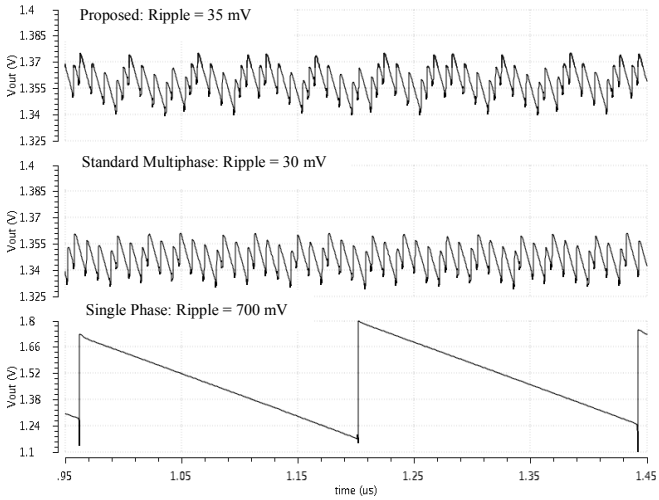

Fig. 6 Output Ripple Comparison with Standard Multiphase and Single Phase Converters with 1.2 mA Load Current

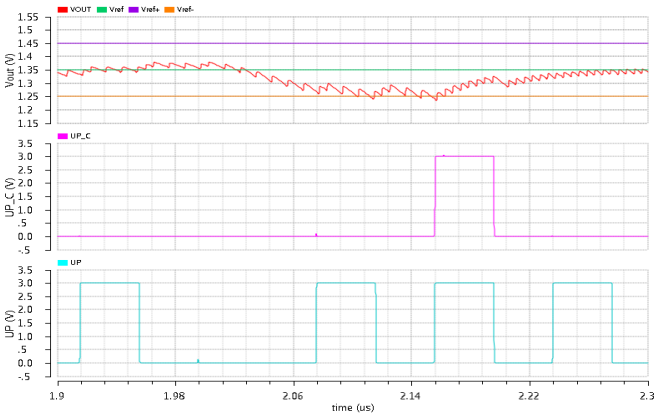

Fig. 7 Load Transient Response

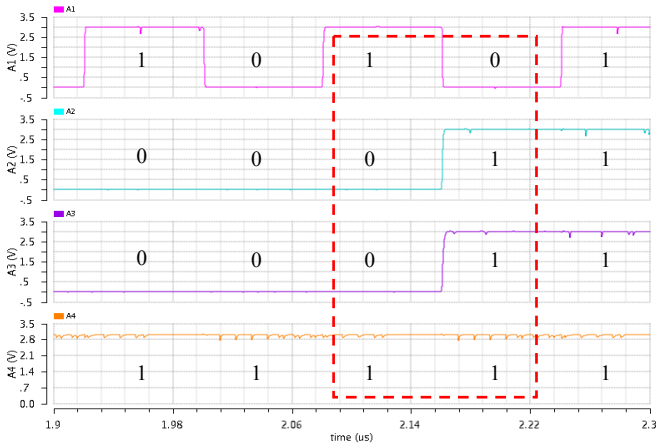

Fig. 8 Four-Bit UP/DOWN Counter Output

IV. CONCLUSION

In this paper, a Triple-Boundary Multiphase with Predictive Interleaving regulation technique is proposed for switched capacitor DC-DC converters. The technique contains a total of three comparators, one of which is used to compare the output with a reference voltage, and by using predictive interleaving, the comparator need not operate at very high frequency. Compared to the previous arts, where N (level of interleaving) comparators or one shared comparator operating at N times higher frequency is used for output regulation, this technique uses three comparators that operate at only the single phase switching frequency, therefore reduces control power and avoids the issue of mismatches among the multiple comparators. Triple boundaries are defined to enable coarse and fine mode of operation, helping to achieve fast load regulation and ensure small ripple at constant load. Moreover, by controlling the number of SC cores that are being switched, the amount of capacitances and switches and thus parasitic bottom-plate capacitance and gate switching losses can be made to scale with the output load.

Table I Comparison with Other SC Converters

Work	[4]	[7]	[9]	This Work
Technology	90 nm	65 nm	22 nm	0.35 um
Regulation Method	Single Boundary Hysteretic	Double Boundary Hysteretic	Single Boundary Hysteretic	Triple-Boundary Hysteretic
# of Phases	10	16	8	15
# of Comparators	10	1	1	3
SC Core Switching Frequency	35 MHz	220 MHz	250 MHz	6.25 MHz
Comparator Switching Frequency	70 MHz	3.5 GHz	2 GHz	12.5 MHz
C_{out}	3.2 nF	1 nF	100 pF	0
Output Ripple	5% Vo	4.4% Vo	5.7% Vo	2.6% Vo

REFERENCES

[1] L. Chang, R. K. Montoye, B. L. Ji, A. J. Weger, K. G. Stawiasz, and R. H. Dennard, "A fully-integrated switched-capacitor 2 : 1 voltage converter with regulation capability and 90% efficiency at 2.3A/mm^2," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2010, pp. 55-56.

[2] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2013, pp. 374-375.

[3] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 2557-2565, 2010.

[4] T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic Capacitive DC-DC Converter With Single Boundary-Multiphase Control and Voltage Domain Stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1715-1727, 2011.

[5] G. V. Pique, "A 41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 98-100.

[6] L. Hanh-Phuc, S. R. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2120-2131, 2011.

[7] L. Salem and Y. Ismail, "Fully integrated fast response Switched-Capacitor DC-DC converter using reconfigurable interleaving," in *Int. Conf. on Energy Aware Computing (ICEAC)*, 2010, pp. 1-4.

[8] M. Dongsheng, "Robust Multiple-Phase Switched-Capacitor DC-DC Converter with Digital Interleaving Regulation Scheme," in *Proc. 2006 Int. Symp. Low Power Electronics and Design, ISLPED.*, 2006, pp. 400-405.

[9] R. Jain, et al., "A 0.45-1 V fully-integrated distributed switched capacitor DC-DC converter with high density MIM capacitor in 22 nm Tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol.49, no. 4, pp. 917-926, Apr. 2014.