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0.18- μm CMOS Push-Pull Power Amplifier With Antenna in IC Package

Wei Wang and Y. P. Zhang

Abstract—A novel architecture of power amplifier with antenna implemented in a ceramic ball grid array (CBGA) package is presented. The monolithic power amplifier designed in a standard 0.18- μm CMOS technology offers 19.5 dBm maximum output power at 5.2 GHz to the antenna with the PAE of 32%. The antenna integrated in the CBGA package achieves impedance bandwidth of 3.86% and gain of 2 dBi at 5.2 GHz. Results demonstrate the feasibility of using this innovative configuration to the design of single-chip 5 GHz transmitter front-end.

Index Terms—CMOS power amplifier, integrated antenna, push-pull power amplifier, transmitter.

I. INTRODUCTION

THE growing wireless LAN market requires compact, low-cost, and low-power RF front-end. The power amplifier (PA) consumes most power, thus an efficient PA is crucial for any RF front-end.

Recently the push-pull PA implemented directly with an antenna to realize an efficient and compact PA has received considerable attention [1]–[3]. In these designs the output power of the push-pull PA is combined in the dual-feed planar antenna. The antenna acts not only as a radiating element but also as an out-of-phase combiner for the fundamental frequency and a tuned load for the higher harmonics. Since the PA is directly implemented with the antenna, the use of an output balun is avoided; as a result, the push-pull PA becomes relatively compact. The push-pull PA in the above designs employs discrete GaAs FETs and various types of planar antennas. The GaAs FETs are expensive while the planar antenna and the ring hybrid consume a large footprint.

More recently, the concept of implementing an antenna in an integrated circuit (IC) package has been proposed for the total solution of a truly single-chip RF front-end [4]. Within this framework, this letter presents a new architecture of a push-pull PA. Fig. 1 shows the new push-pull PA in contrast with an available design. Note that the dual-feed patch antenna is realized on a ceramic ball grid array (CBGA) package and the push-pull PA is designed in deep submicron CMOS. Obviously, the new design takes fully advantages of the standard CBGA package and the mainstream CMOS technology.

Fig. 1. Difference between the available design of the push-pull power amplifier with (a) integrated antenna and (b) the new architecture of the push-pull PA integrated with antenna in CBGA package.

Fig. 2. CBGA package with the microstrip antenna on the top layer and the CMOS chip in the cavity.

II. POWER AMPLIFIER AND ANTENNA

The push-pull PA in this design is a two-stage PA as shown in Fig. 2. The driver stage is biased to class A in order to obtain good linearity while the output stage is biased to class AB for good efficiency. In the single-chip RF front-end, the balanced mixer is often used, so the input ring hybrid for the push-pull PA is not needed any more. For the measurement purpose, the

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Fig. 3. Two-stage power amplifier.

two input ports of the driver stage are both matched to 50Ω . The input matching is achieved by adjusting capacitor C_b and inductors L_g and L_s . The inductor L_d is chosen to be tuned with the capacitive input of the output stage to get maximum gain at the desired frequency 5.2 GHz. Z_A is input impedance at one port of the antenna that is designed to be 50Ω . Matching network is needed to transform Z_A to the optimum load 20Ω of the PA. The transistors in the driver stage and the output stage are sized to be $600 \mu\text{m}/0.18 \mu\text{m}$ and $1500 \mu\text{m}/0.18 \mu\text{m}$ in order to deliver enough output power to the antenna.

The antenna in this design is a microstrip patch fabricated on the top layer of a cavity-down CBGA package. The package measures $15 \times 15 \times 2 \text{ mm}^3$ and the cavity in the middle layer has the size of $12 \times 12 \times 0.6 \text{ mm}^3$ which is big enough for the CMOS chip. The package ceramic material is alumina with dielectric constant of 9.8 and the package metallic material is copper with conductivity of $5.7 \times 10^7 \text{ S/m}$. The microstrip patch at the top surface of the package is sized to be $12 \times 9 \text{ mm}^2$. The feeding of the antenna is realized with two bond wires, two signal traces, and two vias through two apertures on the ground plane of the package. The two bond wires are copper with the length of 3.42 mm and the diameter of the via holes is $100 \mu\text{m}$.

Fig. 3 shows the PA performance designed in Chartered Semiconductor $0.18\text{-}\mu\text{m}$ 1.8/3.3 V Logic/Analog Mixed Signal/RFCMOS process. Note that the maximum output power of the PA is 19.5 dBm with the PAE of 32%. Also note that the power gain is 27 dB for a small-signal input and it drops to 15 dB for a large-signal input. Fig. 4 shows the results of a two-tone test. The output IP3 point is 11 dB higher than the 1-dB compression point. Fig. 5 shows the antenna performance.

Fig. 4. Performance of the PA. Output power, power gain and PAE versus input power.

Fig. 5. Two-tone test of the CMOS power amplifier in IC package ($f_1 = 5.2 \text{ GHz}$, $f_2 = 5.21 \text{ GHz}$).

The minimum return loss occurs at 5.2 GHz and the input impedance bandwidth is found to be 201 MHz from 5.101 GHz to 5.302 GHz (3.9%). The radiation is stronger in the upper hemisphere, i.e., in the direction normal to the microstrip patch. This feature of the radiation pattern is desirable because it not only helps improve the efficiency of the PA but also reduces the interaction of the antenna with the human body. The gain of the antenna is 2 dBi.

III. CONCLUSION

A new architecture of push-pull power amplifier integrated with antenna in CBGA package has been presented in this letter. The PA is designed in deep submicron CMOS and the dual-feed microstrip patch antenna is integrated in the package. Results demonstrate the feasibility of this novel total solution of a truly single-chip RF front-end.

Fig. 6. Antenna performance. The return loss at the two feeding ports versus frequency (a) and the far-field copolarized radiation pattern (b), E-plane, H-plane.

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