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The Manufacture and Performance of Diodes Made in Dielectrically Isolated Silicon Substrates Containing Buried Metallic Layers

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Abstract—Results are reported on the performance of diffused p^+n diode structures manufactured on a novel silicon-on-metal-on-insulator (SMI) substrate. This substrate consists of a thin single crystal silicon layer on top of a tungsten disilicide covered oxidized silicon wafer. The diodes show excellent characteristics with an exponential current-voltage ($I-V$) relationship over nine orders of magnitude and an ideality factor of 1.005, under forward bias conditions. The reverse leakage current is low with a minority carrier lifetime of typically 500 μs . The diodes show no evidence of stress induced defects or degraded performance due to W migration during processing. The SMI substrate is therefore shown to be compatible with standard manufacturing processes.

Index Terms—Buried metallic layers, silicon-on-insulator, silicon-on-metal-on-insulator, tungsten silicide.

I. INTRODUCTION

SILICON direct wafer bonding with grind/polish back is now becoming a commercial technique for the production of silicon-on-insulator (SOI) substrates. Major applications are in the dielectric isolation of bipolar analogue circuits for telecommunications and for smart power control IC's. The technology offers increased packing density and reduced collector-substrate capacitance leading to higher switching speed and lower power dissipation [1]. The thickness of the SOI layer in linear IC's is dictated by the width of the buried collector dopant profile which is relatively large in order to minimize collector resistance. Lateral isolation is provided by trench etching through the SOI layer ($\sim 1.5 \mu m$) and refilling with a dielectric. The incorporation of a buried metallic layer into the collector would decrease the collector series resistance and reduce the SOI layer thickness with a resultant decrease in the time consuming RIE trench etching step. The reduced topography could also allow the refill process to be eliminated further reducing the processing costs. In

Fig. 1. Cross section drawing of the diode structures manufactured on the novel substrate.

low power telecommunication circuits the highly conducting buried metallic layer would allow the f_{max} of the transistors to be maintained even for the output power devices. The technology can also be adapted to provide a conducting ground plane below the buried isolating oxide layer to minimize the inductance of the interconnect lines and so improve overall circuit performance [2]. Combining SOI technology with buried metallic drain/collector contact layers and metal filled contact droppers to minimize series resistance will also enable compact smart power circuits with multiple vertical output power devices to be implemented. These examples illustrate the potential of SMI technology. Direct silicon wafer bonding technology to produce SOI substrates incorporating buried silicide layers has been reported elsewhere [3], [4]. The main concerns about the technology are:

- 1) stress related defects in the SMI layer due to mismatch in thermal coefficients of expansion, leading to reduced carrier lifetimes and increased junction leakage currents;
- 2) metal migration in the silicon from the buried layer creating point defects and degrading device performance.

This letter addresses these issues and describes, for the first time, the electrical performance of devices manufactured in the SMI substrates and establishes its suitability for manufacture.

II. MANUFACTURING PROCESS

N-type epitaxial wafers were used as the starting material. The surface was implanted with an arsenic dose of $3 \times 10^{15} \text{ cm}^{-2}$ at an energy of 40 KeV. A layer of tungsten 50 nm thick was sputter deposited and this was capped with a polysilicon layer deposited by LPCVD. The polysilicon layer was polished and the wafer bonded to an oxidized handle wafer and annealed. This bonding technology which results in a WSi_2 layer of thickness 120 nm and sheet resistance $2.5 \Omega/\text{square}$ is described elsewhere in more detail

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Fig. 2. A typical I - V characteristic in forward bias.

[3]. Grinding and polishing techniques were employed to reduce the active wafer thickness to $2 \mu\text{m} \pm 0.25 \mu\text{m}$. Similar substrates have been produced by other authors using LPCVD layers of WSi_2 [4].

A five mask process was employed to produce diffused p^+n diodes in the substrate. The substrates were wet oxidized at 1000°C to produce a masking oxide layer thickness of approximately $0.5 \mu\text{m}$. This oxide was patterned and a p-type diffusion from a solid boron source was carried out at 1000°C for 20 min to form the p^+n junctions. An LPCVD oxide was deposited at 720°C from a TEOS source and densified at 1000°C for 10 min. The second mask was used to pattern this oxide and n^+ ohmic contact regions were diffused into the n layer. This was carried out at 1000°C for 20 min using a solid phosphorous source.

The substrates were again coated with LPCVD oxide and densified. The third masking step was employed to pattern the oxide and trench etch the silicon layer down to the buried WSi_2 . This was achieved by RIE in an HBr ambient stopping on the WSi_2 layer. A final passivation layer of LPCVD oxide was then deposited and densified. Device manufacture was completed by etching contact windows through the oxide followed by aluminium metallization. The final device structure is

shown in Fig. 1. The mask set incorporated rectangular diodes of equal area ($1.8 \times 10^{-4} \text{ cm}^2$) but varying perimeter. Circular reference diodes were also manufactured.

III. DEVICE CHARACTERIZATION

The current-voltage (I - V) characteristics of the diodes were measured in detail. Back contact to the diodes was achieved by probing the aluminum contacts on the exposed buried WSi_2 layer in the trenches. The forward bias turn on voltage was about 0.7 V and a sharp avalanche breakdown was observed at 6.8 V in reverse bias. The detailed forward bias characteristic is shown in Fig. 2. This characteristic is near ideal with good exponential increase in current flow over approximately nine orders of magnitude. The series resistance component is less than 20Ω and the measured n factor is 1.005 indicating little influence of generation/recombination effects. This is a very significant finding showing the silicon layer to be of device quality with no evidence that the presence of the buried silicide layer is leading to stress induced defects or tungsten penetration of the silicon. The reverse bias characteristic shown in Fig. 3 gives further evidence of the quality of the substrate. The leakage current observed is very

Fig. 3. Typical I - V characteristic in reverse bias.

Fig. 4. Reverse leakage current measured at a bias voltage of 1 V as a function of diode perimeter. Diode area = $1.8 \times 10^{-4} \text{ cm}^2$.

low, rising to about 5 nA as the diode approaches avalanche breakdown.

The combination of diode geometries manufactured allows the measured reverse current to be broken up into three components, i.e., area, perimeter and corner. The diodes were all measured at a fixed reverse bias of 1 V. After elimination of the current flow due to electric field crowding at the diode corners, the leakage current was found to be a linear function of perimeter length as shown in Fig. 4. The area and perimeter components of leakage current in reverse bias were given by

$$J_A = 34 \text{ pA/cm}^2 \quad I_p = 2.1 \text{ pA/cm.}$$

The doping concentration in the epitaxial layer was determined from capacitance measurements to be approximately 10^{17} cm^{-3} . The minority carrier lifetime τ was then estimated from the area component of leakage current to be approximately 500 μs . This value is similar to the values measured on MOS capacitors manufactured on SMI substrates published earlier by the authors [5].

From these results it can be concluded that the presence of the buried silicide layer is not causing any significant degradation of the device. The substrate has undergone standard silicon processing schedules and has been thermally cycled many times for processing at 1000 $^\circ\text{C}$ without evidence of stress induced defects. There is no evidence of deleterious effects caused by W migration during the manufacturing process stages. Judging by the quality of the I - V characteristics it may be that the WSi_2 layer is in fact acting as a gettering layer.

IV. CONCLUSIONS

Diffused p^+n diodes have been successfully manufactured on SMI silicon substrates. The diodes have near ideal characteristics with an exponential I - V relationship over nine orders of magnitude and an n factor of 1.005. An estimated minority carrier lifetime of approximately 500 μs also indicates high quality material with no evidence of stress-induced defects caused by thermal cycling. WSi_2 is present in the substrates throughout the entire device manufacturing schedule and there is no evidence of W migration leading to degraded device performance.

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REFERENCES

- [1] P. Saul, "The benefits of bonding silicon-on-insulator for bipolar IC's," *IEE Rev.*, pp. 263-266, Nov. 1994.
- [2] A. Plettner, K. Habberger, A. Englmaier, H. Hartmann, and K. Neumeier, "Interconnect scheme for improved high-speed IC's," in *Proc. IEDM*, Dec. 1994, pp. 121-124.
- [3] W. L. Goh, D. L. Campbell, B. M. Armstrong, and H. S. Gamble, "Buried metallic layers with silicon direct bonding," in *Spring Meet. Electrochem. Soc.*, May 1995, vol. 95-7, pp. 553-560.
- [4] R. Wilson, C. Quinn, B. McDonnell, S. Blackstone, and K. Yallup, "Bonded and trehched SOI with buried silicide layers," in *Spring Meet. Electrochem. Soc.*, May 1995, vol. 95-7, pp. 535-542.
- [5] W. L. Goh, J. H. Montgomery, S. H. Raza, B. M. Armstrong, and H. S. Gamble, "Electrical characterization of dielectrically isolated silicon substrates containing buried metallic layers," *IEEE Electron Device Lett.*, vol. 18, pp. 232-234, May 1997.