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Ultra Low-Power Full-Adder for Biomedical Applications

Eng Sue Chew, Myint Wai Phyu, and Wang Ling Goh*

Abstract—Addition is an essential function in fundamental arithmetic operations. It is also the most copiously used operation in application-specific processors and digital signal processing application (DSP). In this paper, we propose a novel 17-transistors full-adder based on the N-12T full-adder, which has a maximum of one threshold voltage (V_t) degradation for output voltage levels. The performance of the proposed full-adder is compared against other low-power full-adder via extensive HSPICE simulation using 100 random input vectors. The simulation results show that the proposed design permits the use of lower operating voltage to derive lower power consumption and hence, the power delay product (PDP). The advantages of the proposed full-adder has been evaluated by integrating the proposed full-adder into a multiplier-less finite impulse response (FIR) filter that is commonly used in the multirate filter bank for biomedical applications.

I. INTRODUCTION

Integrated circuits (ICs), particularly the complementary metal oxide semiconductor (CMOS) ICs, are playing an ever-increasing role in implantable biomedical systems. ICs must be designed to satisfy rigorous reliability and redundancy, not forgetting the error-checking requirements that are associated with life-sustaining medical devices. Both the low-voltage and low-power operations are also obligatory for battery-powered systems that may be implanted for as long as ten years.

The equipments used in biomedical signal processing are often influenced by noise. Hence, the resulting images may not provide the quality needed for desire analysis. Digital linear filtering is the method used to remove disturbances in real time. Full-adder with low operating power and low power consumption is important in the wavelet filter bank implementation since addition is one of the main operations in the finite impulse response (FIR) filter.

The major components of power consumption in digital CMOS VLSI circuits are:

- *Switching power* - consumed in charging and discharging of the circuit capacitances during transistor switching [1].
- *Short-Circuit power* - caused by short-circuit current switching transient [1].

The switching power and short circuit power are collectively called the dynamic power, which contribute mainly to the total power consumption in the digital VLSI system, and can be defined as that shown in Equation (1) [1].

$$P_{total} = P_{switching} + P_{short} \quad (1)$$

$$= f \cdot C_{load} \sum_i V_{swing} \cdot \alpha_i \cdot V_{DD} + V_{DD} \sum_i I_{sc}$$

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where V_{DD} is power supply voltage, V_{swing} is the voltage swing of the output which is ideally equal to V_{DD} , C_{load} is load capacitance at output node V_{out} , f is system clock frequency, α is switching activity at node V_{out} , and I_{sc} is short-circuit current at node V_{out} . The summation seen in Equation (1) refers to all the node capacitances of the circuit [1].

II. REVIEW OF EXISTING LOW-POWER 1-BIT FULL-ADDER

Several full-adder circuits featuring low-voltage and low-power have been published. The Sumeer Goel's full-adder [2], which is designed using the hybrid-CMOS design style, provides freedom in the selection of modules within a circuit, depending on application. It can be broken down into three modules: the XOR and XNOR intermediate signals are produced in Module I and are passed on to Module II and Module III for the generation of the Sum and C_{out} outputs. The Sum and C_{out} outputs are formed using the following expressions [2]:

$$Sum = H \cdot C_{in} + H' \cdot C_{in} \quad (2)$$

$$C_{out} = A \cdot H + C_{in} \cdot H \quad (3)$$

Hybrid full-adder [3] can also be divided into three sub-modules. The intermediate XOR and XNOR functions are generated separately using different sets of transistors so as to reduce the probability of producing spurious switching and glitches. Weak logic signal caused by the transistors is restored by the two complementary feedback transistors. The logical expressions for the intermediate signals and output are given as below:

$$Y = A \oplus B \quad (4)$$

$$Sum = Y \oplus C_{in} \quad (5)$$

$$C_{out} = A \cdot B + C_{in} \cdot Y \quad (6)$$

The ultra low-power full-adder (ULPFA) [4] is based on the 4-transistor low-power XOR gate and ultra low-power (ULP) diode. Low-logic level ultra low-power (ULP) diode restorer is used to restore the weak logic 0 for the input signals with combination of (0, 0). The leakage current of the standard diode is reduced when the transistors are reversed biased and operate with negative V_{gs} voltages.

The output of Complementary and level restoring carry logic (CLRCL) [5] full-adder is shown as below:

$$Sum = (A \oplus C_{in}) \cdot \overline{C_{OUT}} + (\overline{A \oplus C_{in}}) \cdot B \quad (7)$$

$$C_{out} = (A \oplus C_{in}) \cdot B + (\overline{A \oplus C_{in}}) \cdot A \quad (8)$$

The CLRCL full-adder [5] is a low complexity circuit, so as to achieve faster cascade operation. Proper level restoring technique with the inverter is used to solve the multiple threshold voltage V_t losses problem in the carry propagate chain.

The N-12T full-adder [6] generates its Sum and C_{out} outputs using the pass-transistor logic style. The advantage of this full-adder is that the V_t loss does not propagate to the output even if the inputs of the XNOR gates suffer a V_t loss when it is applied to input B. Circuit diagrams of the full-adder just described are all presented in Figure 1.

(a) Sumeer Goel's full-adder [2]

(b) Hybrid full-adder [3]

(c) ULPFA [4]

(d) CLRCL full-adder [5]

(e) N-12T Full-adder [6]

Figure 1. Low-power full-adder cells.

III. PROPOSED FULL-ADDER

Previous N-12T full-adder does not operate correctly at low power supply due to the accumulation of V_t losses. Here, we present a solution by modifying the N-12T full-adder so that for the worst-case scenario where $A = '1'$ and $B = '1'$, XNOR output is able to achieve full-swing instead of having $V_{DD} - V_t$. By connecting the gate of the level restoring pMOS to the output of XOR function, for every XNOR output with a V_t loss, the logic '0' of XOR will turn on the pMOS and pull the degraded XNOR output to V_{DD} .

The Sum output of N-12T full-adder has a maximum of one V_t loss. The pass transistor logic is substitute by the transmission gate so to ensure full voltage swing at the sum output. These modifications have increased the total number of transistors to 17 (see Figure 2).

Figure 2. Proposed full-adder.

IV. SIMULATION RESULTS AND DISCUSSION

The circuit simulation works are carried out using 100 random input vectors with HSPICE simulator. The sizes of all the transistors in the circuits discussed are optimized such that the circuits dissipate the lowest power. The simulation setup is shown in Figure 3. Worst-case delay, average power consumption, power-delay product (PDP) and corner simulation are used to evaluate the performance of the circuits.

Figure 4 illustrates the power consumptions of the full-adder at different supply voltages. At 1.8 V, the proposed full-adder consumes approximately 23%, 36%, 60%, 13% less power than the Sumeer Goel's full-adder, hybrid full-adder, ULPFA and CLRCL full-adder, respectively, but 34% more than the N-12T full-adder. However, at a power supply of 1.2 V, the proposed full-adder dissipates about 20% and

24% less power if compared to the Sumeer Goel's full-adder and hybrid full-adder, respectively.

Figure 3. Simulation testbench.

Figure 4. Power results in the full-adders at different supply voltage.

The cell delay is measured at the instant when the input reaches 50% of the voltage supply level (after the input buffers) to the same 50% voltage level of either the *Sum* or *C_{out}* signals, whichever the later (before the output buffers) [2]. Figure 5 depicts the delays of the variants full-adders at power supplies of 1.8 V, 1.5 V and 1.2 V. When operated at 1.2 V, the proposed full-adder illustrates an increment of roughly 1% and 2% in delay when compared to the Sumeer Goel's full-adder and hybrid full-adder, respectively.

Figure 5. Delay results in full-adders of different supply voltages.

PDP is the product of average power consumption and worst case delay of the full-adder, and is used to demonstrate the trade-off between the power consumption and delay.

Figure 6 shows that proposed full-adder can achieve the lowest PDP at 1.2 V. The proposed full-adder exhibits an improvement of 20% and 22% of PDP than Sumeer Goel's full-adder and hybrid full-adder, respectively, at 1.2 V. At 1.5 V, the proposed full-adder demonstrates 57% and 14% lower PDP than the ULPFA, CLRCL full-adder, respectively, but 38% higher than the N-12T full-adder.

Figure 6. PDP results in full-adder.

Corner simulations are used to investigate the differences due to process inaccuracies, temperature and other parameter variations. Hence, corners simulation is essential to check the influence of the parameter variations on IC. In the MOSFET model library, corners such as Fast nMOS Fast pMOS, Slow nMOS Slow pMOS, Fast nMOS Slow pMOS, Slow nMOS Fast pMOS and typical nMOS typical pMOS are included in the process kit. Table I tabulated the power consumption of Fast nMOS Fast pMOS, Slow nMOS Slow pMOS and typical nMOS typical pMOS corners of the proposed full-adder respectively. At a power supply of 1.2 V, the proposed full-adder shows difference of 3.46% and 8.05% between Fast pMOS Fast nMOS to typical nMOS typical pMOS and Slow nMOS Slow pMOS to typical nMOS typical pMOS.

V. IMPLEMENTATION INTO THE FIR FITLER

To evaluate the effectiveness of the proposed full-adder, the proposed design has been embedded into a wavelet filter bank. The proposed full-adder is designed in the form of soft-macro. Filter's constant coefficient multipliers are usually implemented in hardware using a sequence of shift and add operations, where the multiplication operations can be avoided since the filter coefficients can be represented as numbers of power of two. From [7], the coefficients of the low-pass and high-pass filters can be reproduced as shown in Equations (9) and (10).

$$LPF: H(z) = \frac{1}{8} + \frac{3}{8}Z^{-1} + \frac{3}{8}Z^{-2} + \frac{1}{8}Z^{-3} \quad (9)$$

$$LPF: G(z) = 2 - 2Z^{-1} \quad (10)$$

Presented in Figure 7 is the wavelet filter bank that finds many applications in biomedical signal and image processing. The main idea of using the filter banks is to separate the frequency domain of the signal under consideration, into two or more signals, or to combine two or more different signals

into single signal. Filter circuits engaged within the wavelet filter bank are illustrated in Figure 8 [7].

The proposed full-adder is implemented into the wavelet filter bank so to explore its advantage in the battery-powered portable biomedical applications. By incorporating the

TABLE I. RESULTS OF CORNERS SIMULATIONS OF THE FULL-ADDERS.

Full-adder	Power consumption (μW)								
	1.8 V			1.5 V			1.2 V		
	Typ.	SS	FF	Typ.	SS	FF	Typ.	SS	FF
Sumeer Goel's FA	8.58	7.54	11.2	5.25	4.71	6.29	3.07	3.19	3.20
Hybrid FA	10.3	8.59	11.3	6.09	5.06	7.18	3.20	3.07	3.68
CLRCL FA	16.6	1.39	2.08	9.30	7.74	1.23	N.A.	N.A.	N.A.
ULPFA	7.61	7.05	8.79	4.66	4.45	5.27	N.A.	N.A.	N.A.
N-12T FA	4.92	4.10	5.97	2.98	2.80	3.27	N.A.	N.A.	N.A.
Proposed FA	6.61	5.83	7.68	4.06	4.04	4.31	2.45	2.64	2.53

Figure 7: Wavelet filter bank [7].

Figure 8: Filter inside wavelet filter bank circuits [7].

The proposed full-adder is implemented into the FIR filter and the design dissipated an average power consumption of 25.2 μW at a frequency of 50 MHz. As shown in Table II, this design shows an improvement of 36.7% in power consumption when compared to the multiplier-less FIR filter using Sumeer Goel's full-adder.

CONCLUSION

In this paper, we proposed a 17-transistor full-adder that is able to operate at 1.2 V power supply. The performance of the full-adders is compared and the simulation results proved that proposed full-adder dissipate the lowest power consumption and lowest PDP.

proposed full-adder, the multiplier-less FIR filter can achieve an improvement of 36.7% in power consumption when compared to the Sumeer Goel's full-adder.

Table II. Power consumption comparisons of multiplier-less FIR filter.

Multiplier-less FIR filter using	Power consumption (μW) @ 50 MHz
Sumeer Goel's FA	39.8
Proposed FA	25.2

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