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Tan, Cher Ming; Sun, Lina; Wang, Chase

2009

Tan, C. M., Sun, L., & Wang, C. (2009). Going green for discrete power diode manufacturers. In proceedings of the 4th IEEE Conference on Industrial Electronics and Applications: Xian, China, (pp.3303-3306).

<https://hdl.handle.net/10356/99901>

<https://doi.org/10.1109/ICIEA.2009.5138814>

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Going Green for Discrete Power Diode Manufacturers

Cher Ming Tan

Nanyang Technological University,
School of EEE
Block S2, Nanyang Avenue,
Singapore 639798

ecmtan@ntu.edu.sg

Lina Sun

Nanyang Technological University,
School of EEE
Block S2, Nanyang Avenue,
Singapore 639798

Chase Wang

Sino-American Silicon Products Inc.
No. 8, Industrial East Road 2,
Science-based Industrial Park
Hsinchu, Taiwan, Republic of China.

Abstract—Owing to its deep diffusion requirement for discrete power diode of rating above 400V and 1A, the time and temperature for p+ and n+ diffusion of a typical p+nn+ discrete power diode are around 1100°C and more than 36 hours. This represents tremendous power consumption in the manufacturing of power diode. In this work, we propose an alternative method for producing the discrete power diode which requires only 400°C and 4 hours of fabrication duration. Experimental results show that the diode produced do possess typical diode electrical characteristics.

Index Terms—power diode, wafer bonding, energy consumption, junction interface characterization

I. INTRODUCTION

Owing to the deep diffusion requirement for discrete power diode of rating above 400V and 1A, the time and temperature required for p+ and n+ diffusion of a typical p+nn+ discrete power diode is around 1100°C and more than 36 hours. This represents tremendous power consumption in the manufacturing of power diode.

In view of the effort to reduce energy consumption globally, an alternative way to fabricate power diode is introduced. This fabrication method leverage on the low temperature direct wafer bonding technology developed recently [1]. Using this method, the time and temperature of fabricating any rating of power diode are 4 hours at 400°C.

In this work, diodes are fabricated using this novel method and electrical characterization as well as junction interface characterizations of the diodes are performed.

II. DIRECT LOW TEMPERATURE Si TO Si WAFER BONDING METHODOLOGY

Conventional wafer bonding requires high temperature annealing above 800°C, and the time required for complete bonding is usually more than 100 hours [2]. Recently, we have developed a medium vacuum wafer bonding (MVWB) for Si-SiO₂ and Si-Si with a vacuum level of 0.001 mbar which can be easily obtained using standard vacuum furnace. High bonding strength (larger than 20 MPa) is achievable at the bonding temperature of only 400°C, and the annealing time for complete bonding is only several hours (less than 5 hours). [1]

The bonding procedure is shown schematically in Figure 1. Pull test is used to assess the bonding strength and Scanning acoustic microscope is used to determine the bonding efficiency, i.e. the percentage of the bonded area over entire wafer area. Table I shows the comparison of the bonding strength of MVWB with the conventional wafer bonding. With 400°C annealing for 2 hours, we also found that 94% of the wafers are bonded without any void under the clean room environment of class 1000.

Another feature of the MVWB is that no force is needed to push the wafers together. In fact, bonding strength is stronger without any applied load as shown experimentally [3]. The mechanism of such a MVWB is described in Reference [4]. Hence, it is possible to perform wafer bonding in a standard vacuum furnace in batches just as the standard diffusion method for wafers in power diode fabrication.

Figure 1 Bonding Process of MVWB

Table I Comparison of the bonding strength (MPa) between the Conventional Standard Wafer Bonding and MVWB.

Time (hour)	Temperature (°C)					
	200		300		400	
	Standard Bonding	MV WB	Standard Bonding	MV WB	Standard Bonding	MVWB
1	4	11	2.6	14	7	20
2	3	10.3	3.2	24	8.5	28
3	3.9	14	5.1	19	9.4	27
4	4.5	16	4.3	23	9.1	28
5	4.9	15	6	20	12	28

III. FABRICATION OF POWER DIODES

Figure 2 Experimental Procedure for this work

With the MVWB method described above, it is reasonable to explore the use of MVWB for discrete power diode fabrication. Before we embark in the actual power diode fabrication, we applied the MVWB to fabricate a pn+ junction using a boron doped p type wafer with doping concentration of $5 \times 10^{14} \text{ cm}^{-3}$ and a Arsenic doped n+ wafer with doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$. Both wafers are 6".

In order to characterize the bonded junctions, we perform the I-V and C-V measurement for the junctions. From the I-V and C-V measurement results, we compute the generation lifetime profile that indicates the interface defect profile due to the wafer bonding. The profile is obtained using a simple procedure described in References [5, 6]. DLTS analysis is also performed to determine the nature of the defects at the interface. The experimental procedure is shown in Figure 2

The wafer bonding is according to MVWB with annealing temperature of 400°C for 4 hours. The withdrawal speed of the wafers from the furnace is 500 mm/min as too slow the speed will reduce the through-put, and too high the speed will induce excessive interface mechanical stress that can damage the mechanical integrity of the bonded interface. The maximum interface stress at 500 mm/min is below 17 MPa as computed using ANSYS as shown in Figure 3, and it is below the bond strength of 20 MPa.

Figure 3 Hydrostatic stress at the bonding interface due to the non-uniform temperature distribution of the bonded wafer pair as they are withdrawn from vacuum furnace at 400°C with a withdrawal velocity of 500 mm/min.

IV. CHARACTERIZATION RESULTS OF POWER DIODES

Both I-V and C-V measurement of the diced samples is carried out, and the results obtained are used for the calculation of generation lifetime at the interface region. I-V and C-V profiles are obtained using HP4156A and HP4284A respectively,. Voltage supply ranges from 5 volts to -40 volts for CV profiling, and from 10 volts to -200 volts for IV profiling, due to the function limitation of the equipment.

Figure 4 shows the I-V curve of the pn junction fabricated which is promising, though the reverse current is slightly higher. The generation carrier lifetime of a fabricated pn junction is shown in Figure 5 which shows that the defect region is about 10 μm into the p region. This large region is believed to be due to the combination of the initial sub-surface wafer defect region and the bonding itself. The reason for such a belief is that the 10 μm defect region remains the same regarding of the change in the bonding condition. Further investigation on the nature of the length of the defect region will be explored, and with such a reduction, the reverse leakage current will also be reduced.

Figure 4 I-V curve for two of the pn junction fabricated. (a) entire I-V curve; (b) the reverse bias I-V curve

Figure 5 Typical carrier Generation Lifetime Profile into the p wafer measured from the pn junction of the junction fabricated.

To understand the nature of the defect region further, DLTS is employed. Deep-level Transient Spectroscopy (DLTS) analysis is carried out to obtain the defect activation energy and defect density at the sample bonding interface. The principle of the DLTS is through observing the capacitance transient associated with the change in depletion region width as the diode returns to equilibrium from an initial non-equilibrium state. The capacitance transient is measured as a function of temperature (usually in the range from liquid nitrogen temperature to room temperature 300K or above). By using a double box-car averaging technique, peaks at a particular emission rate are found as a function of temperature from the emissions at different rates and the temperature of the associated peak. The DLTS system used in this work is the Bio-Rad DL8000 Deep Level Transient Spectrometer System.

From the DLTS analysis, we found that there are two types of traps in the defect region. One of them is at the energy level of 0.29 eV above the valance band with a concentration of $3.82 \times 10^{10} \text{ cm}^{-3}$ and a capture cross-section area of $5.9 \times 10^{-18} \text{ cm}^2$, and hence this defect type is believed to be the Fe impurity [7]. This defect can be removed through proper wafer processing.

Another type of defect is at the energy level of 0.34 eV above the valance band with a concentration of $1.3 \times 10^{11} \text{ cm}^{-3}$ and a capture cross-section area of $5.9 \times 10^{-18} \text{ cm}^2$, and hence it is believed to be the dislocation [7]. This defect may be able to reduce through prolonged annealing time and higher temperature.

V. CONCLUSION

In this work, we propose an alternative way to fabricate pn junction by simply putting a p-wafer and a n-wafer together using the technique of medium level wafer bonding method.

This method can save tremendous amount of energy during fabrication, and also provide a fast turn-around time.

Extensive characterization of the formed junction is performed in this work, and typical diode I-V characteristic is obtained. The large reverse leakage current of the junction fabricated is stem from the interface defects due to a combination of the initial sub-surface damage in the wafer, the presence of Fe impurity on the surface and the wafer bonding process. Further fine tuning of the wafer processing is believed to be able to bring this wafer bonding process into a mature wafer fabrication process for discrete power diode, saving energy and at the same time, improve the though-put.

ACKNOWLEDGMENT

The authors would like to appreciate the support from NTU Characterization room for our characterization work, Kunshan Sino Silicon Technology Co. Ltd for providing the wafer bonding facilities and SIMTech for providing the scanning acoustic microscopy and dicing facilities required in this work.

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