

This document is downloaded from DR-NTU, Nanyang Technological University Library, Singapore.

Title	A low-power, reconfigurable smart sensor system for EEG acquisition and classification
Author(s)	Sukumaran, Dinup; Enyi, Yao; Shuo, Sun; Basu, Arindam; Zhao, Dongning; Dauwels, Justin
Citation	Sukumaran, D., Enyi, Y., Shuo, S., Basu, A., Zhao, D., & Dauwels, J. (2012). A low-power, reconfigurable smart sensor system for EEG acquisition and classification. 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp.9-12.
Date	2012
URL	<a href="http://hdl.handle.net/10220/16338">http://hdl.handle.net/10220/16338</a>
Rights	© 2012 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. The published version is available at: [ <a href="http://dx.doi.org/10.1109/APCCAS.2012.6418958">http://dx.doi.org/10.1109/APCCAS.2012.6418958</a> ].

# A Low-power, Reconfigurable Smart Sensor System for EEG Acquisition and Classification

Dinup Sukumaran<sup>1</sup>, Yao Enyi<sup>1</sup>, Sun Shuo<sup>1</sup>, Arindam Basu<sup>1</sup>, Dongning Zhao<sup>2</sup> and Justin Dauwels<sup>1</sup>

<sup>1</sup>School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798

<sup>2</sup>Institute of Microelectronics, 11 Science Park Road, Singapore 117685

Email: dinup1@e.ntu.edu.sg; eyao1@e.ntu.edu.sg; arindam.basu@ntu.edu.sg;

**Abstract** — We describe a smart sensor for EEG acquisition comprising a programmable gain low-noise amplifier followed by an integrated feature extraction and classification circuits. The feature extraction block comprises a bank of four band-pass filters followed by a wide dynamic range peak detector. The output of the peak detector is fed into a spiking neural network implementing the extreme learning machine (ELM) for classification. The advantage of ELM is that it has been shown to attain comparable performance to support vector machine (SVM) but with fewer computational nodes. We describe simulation results of each block designed in 0.35 um CMOS and demonstrate system level performance by using this to detect seizure onset in epileptic patients. The system can be reconfigured for other applications like speech classification.

## I. INTRODUCTION

The electroencephalogram (EEG), micro volt signals that results on the scalp from brain activity, provides a non-invasive method of recording a person's brain waves. In the traditional non-invasive EEG recording systems, EEG sensors acquire brain signals from the scalp and transmit the digitized raw EEG data to a base station for further analysis and processing. EEG data can be used for the diagnosis and treatment of neurological disorders including epilepsy, dementia, coma and sleep disorders. Another application is brain computer interface (BCI) that transforms brain signals to commands that can control external assistive devices or applications for rehabilitative support in completely paralyzed or seriously disabled patients with spine injury, central nerve damage and motor disabilities[1]. EEG signal analysis and processing for different pattern recognition/classification are very important for EEG based communication as well as for clinical diagnosis and control.

EEG data often contains large bulk of redundant and irrelevant data with very little data related to rare or subtle patterns associated with desired medical conditions. For wearable applications like continuous long term recording for neural disorder diagnosis and treatment, wireless transmission of data is necessary and a large bulk of data for wireless transmission implies significant power overheads[2]. This large volume of data requires large memory for storage and more time and resource intensive data processing and analysis. Data reduction by local signal processing to identify relevant

patterns, while rejecting diagnostically useless background brain activity can reduce the amount of EEG data by several orders of magnitude. This can enable quick processing and interpretation of EEG data that is essential for prompt feedback in applications like portable closed-loop epileptic seizure controller, BCI and augmented cognition solutions[2].

This paper presents a smart sensor IC designed in 0.35 um CMOS for scalp EEG acquisition that integrates local processing on the sensor node itself. By increasing the processing power on the sensor with ultralow power electronic circuits, and transmitting less information, the power consumption of the system can be reduced increasing operational life time and reducing battery size as well as weight.

The proposed smart sensor consists of a low-noise amplifier (LNA) for signal acquisition from a single electrode, followed by feature vector extraction and machine learning classification of feature vectors. Analog signal processing and classification methods are employed for improved power and area performance. A spiking neuron based Extreme Learning Machine (ELM) pattern classification hardware is used in this design. ELM possesses similar classification capabilities as a support vector machine (SVM), but requires less nodes for classification[3]. Also ELM requires random weights in the first stage which can be obtained from the inherent threshold voltage variations of transistors. The mismatch inherent in analog VLSI circuits, which is seen as a disadvantage in most of the analog designs, is thus exploited in ELM hardware implementation.

Depending upon the application a number of smart sensors can be collated to make EEG based communication or diagnosis/treatment system. For example, in the case of epileptic seizure detection, a number of smart sensors can be worn to achieve spatial correlation. The output from individual classifiers can be combined to detect the epileptic seizure onset.

The remainder of the paper is organized as follows. In section 2 system architecture is discussed, followed by detailed description of different sub blocks. Results are

included in Section 3 and finally we present conclusions in the last section.

frequencies. The WLRT achieves a subtraction of the output voltages of two adjacent LPFs and forms one low pass filter and 3 band pass filters finally. To preserve linearity in the

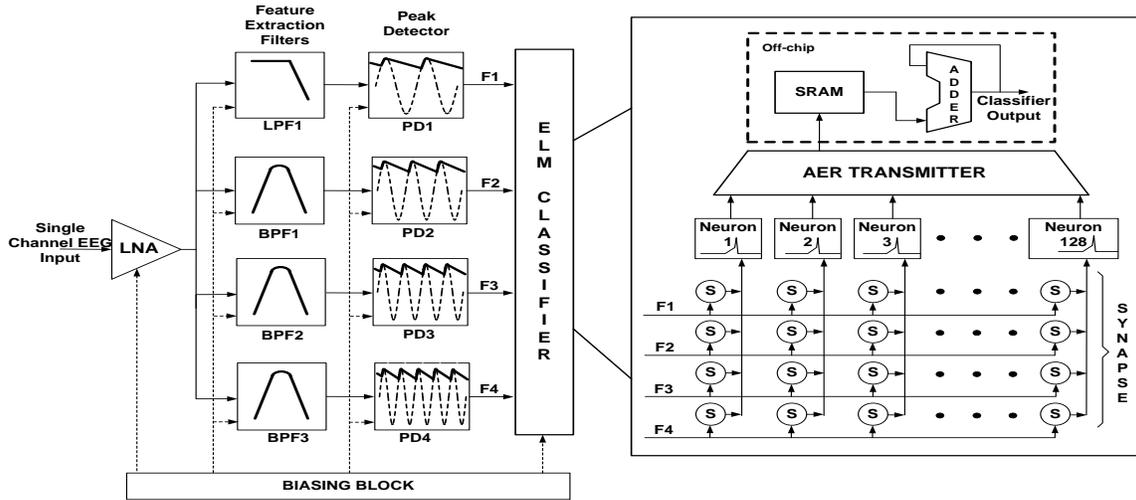


Fig. 1: System Architecture of the smart sensor with LNA, feature extraction and classification blocks.

## II. SYSTEM ARCHITECTURE

The proposed smart sensor block diagram is as shown in Fig.1. It integrates an LNA, feature vector extraction filters, peak detectors and an ELM pattern classifier. The system extracts the spectral energy of the signal in four different frequency bands to form a feature vector. This feature has been shown to be useful in many applications including seizure onset detection[4]. Feature vectors are then provided to an analog ELM classifier (as currents) to classify them into categories. Since this topology is also useful in a wide set of applications, we have made the system reconfigurable so that it can be used for signals in the audio frequency range as well. Next, we describe each sub-block in the system.

### A. LNA

The LNA uses a capacitive amplifier topology commonly used in neural recording applications[5]. A MOS-bipolar pseudo-resistor is used to bias the input node which creates a high pass corner at very low frequencies (<0.1 Hz). The circuit has five programmable gain settings of 1, 20, 25, 50 and 100 by varying capacitor ratios. It dissipates 12 uW for a noise floor of 3 uV rms in the EEG signal band of 0.1-200 Hz.

### B. Band-pass Filters

Figure 2 shows the topology of the low power filter bank comprising 4 low pass filters (LPF) each followed by a wide linear range transconductor (WLRT). The LPF circuit is same as the LNA; but the bias currents are chosen much smaller to set the desired corner frequencies. The closed loop gain,  $A_M$  is fixed to 10. The bias currents of 4 LPFs are set to be 1: 2: 4: 8 creating octave spacing in the corner frequencies. By tuning the master bias current using a current splitter[6], this circuit can be applied in different applications with different

signal chain, a capacitor divider composed of two capacitors  $C_3$  and  $C_4$  is added at input terminals of the traditional transconductor. Thus, only a fraction of the input differential voltage (proportional to  $C_3/C_3+C_4$ ) will be coupled to the input node effectively increasing the linear range of the

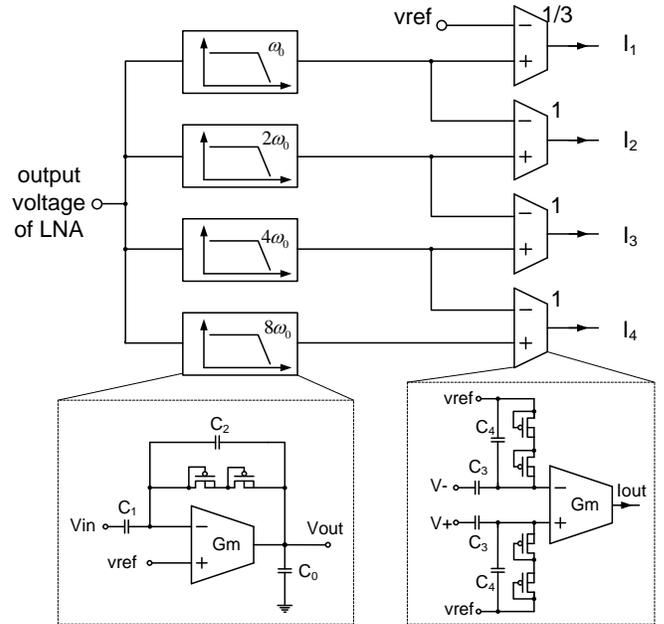


Fig. 2: Band pass filters are created by taking the difference of outputs of two low-pass filters with different corner frequencies..

transconductor. Pseudo-resistors are again used to bias the input nodes. Figure 3(a) shows the SPICE simulation result of the LPF and BPFs for EEG applications. When the corner frequencies are 2Hz, 4Hz, 8Hz and 16Hz respectively, the total power consumption for this part is only 36nW.

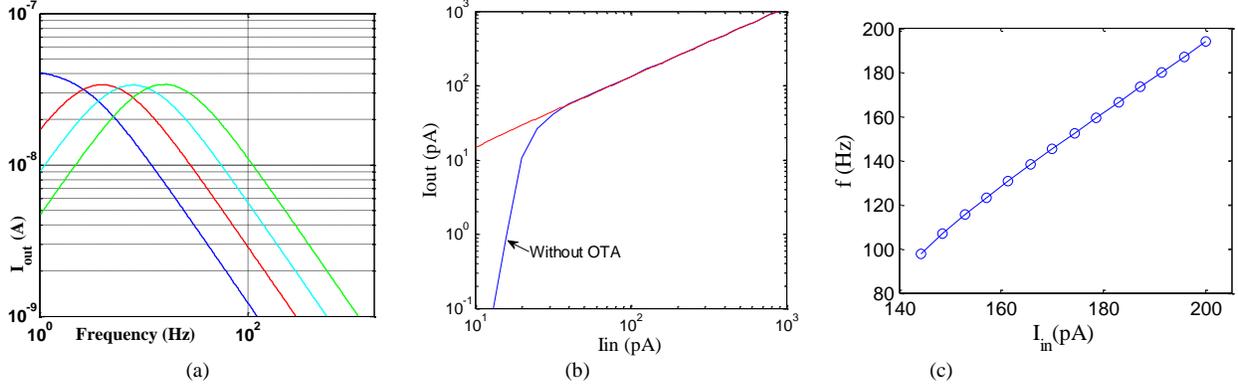


Fig. 3: (a) Simulation results of the low pass filter and band pass filters with EEG application: corner frequencies are 2 Hz, 4 Hz, 8 Hz and 16 Hz. (b) Envelope detector output showing wide dynamic range. (c) Output spike frequency versus input current for the spiking neuron.

A major problem in the WLRT is increased effective input offset due to the capacitive attenuation before the differential pair. In our design, a 6 bit signed current splitter using one-eighth of the bias current is employed to reduce the offset current for 9 bit precise operation.

### C. Envelope Detector

Envelope detection is a significant process in the feature extraction part since it provides an estimate of relative strengths of the signals in different frequency bands. We chose envelope detection over energy detection due to the large output dynamic range needed by the squaring operation in energy detection. To keep the system configurable and allow wide input dynamic range, we used a current rectifier followed by current-mode peak detection[7] as shown in Fig. 4. A class B current conveyor is used as a rectifier; though both positive and negative currents can be obtained from this circuit, we only use the positive half. For positive currents only  $M_p$  conducts while only  $M_n$  conducts in the negative half of the input current waveform. In order to reduce the dead zone of the current rectifier (caused by insufficient time available to small currents to charge the parasitic capacitance at the input), an OTA is employed in a feedback loop to reduce the input impedance by a factor equal to its open-loop gain. Minimum transistor size is adopted for  $M_n$  and  $M_p$  to reduce the parasitic capacitor at input due to miller effect. We found that for the extremely low signal frequencies in EEG applications, the OTA is not necessary; however it is very important even for audio frequencies of a few kHz. Hence, we have an option of switching off the OTA when the desired signals are of very low frequency saving the 400 nW/channel consumed by this design.

The peak detector (PD) uses current mode topology[7] with adjustable attack and release times obtained by tuning the bias current  $I_a$  and  $I_r$ . While  $I_a$  is same for all four frequency bands,  $I_r$  is set in proportion to the corner frequency of the respective band. To avoid an extra voltage bias as needed in [7], the source of  $M_1$  and  $M_4$  can be biased with a transistor diode connected to  $V_{dd}$ . Figure 3(b) depicts the performance of the envelope detector with the X-axis showing peak value of the input sinusoid while the Y-axis plots the DC output

current. In this case, the frequency of the sinusoid is kept at 1 kHz to show the advantage of using the OTA. The power dissipation of this block is signal dependent with an average value of 50 nW/channel.

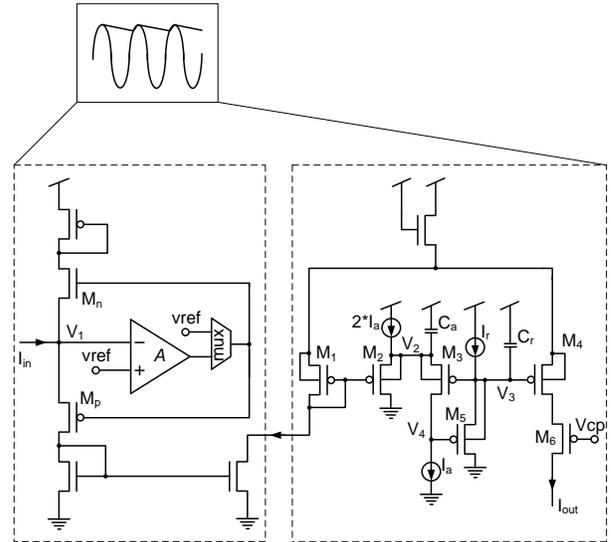


Fig. 4: Schematics of current rectifier and peak detector

### D. Spiking Neuron based ELM classifier

We have earlier demonstrated that a spiking neural network can be used to efficiently implement an ELM[8]. The spiking neuron essentially implements a sigmoid-like transfer function where the input is a current and output is a spike rate. In this chip, we have used the diff-pair integrator (DPI) based neuron[9] though other simpler structures would suffice. The primary reason for this is to enhance the usability of this chip in bio-realistic neural network simulations as well. Figure 3(c) shows the current-frequency relationship of this neuron. The input current for the neuron comes from the PD output. Transistor  $M_4$  and  $M_6$  in Fig. 4 are replicated 'N' times (where N is the number of neurons) for each frequency band and the input current for each neuron is obtained by summing the four PD outputs for that neuron. These current copies of the PD output will be different due to the inherent

mismatch between transistors—this exactly fits the requirement of random weights for the input stage of the ELM! In fact, smaller transistors have more mismatch; this is a unique property of our implementation which makes it favorable for VLSI scaling.

### III. SYSTEM SIMULATIONS

The simulation for the whole processing chain from the LNA to the peak detector output is shown in Fig. 5. The input frequency was increased from 2 Hz to 16 Hz in this simulation. Figure 5 plots the outputs of the four peak

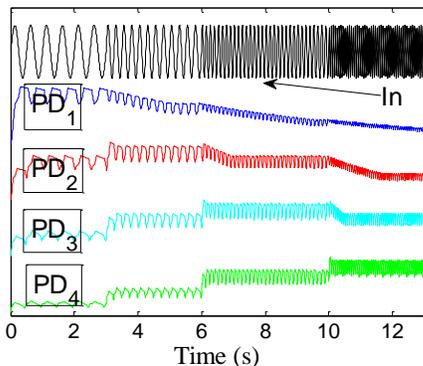


Fig. 5: SPICE simulation of the whole signal processing chain showing peak detector outputs for an input signal with varying frequencies. Absolute values are not shown for ease of viewing.

detectors for one of the neurons. We can see that the output currents of each band reach a maximum value when the input signal has a frequency that best matches the frequency of that band demonstrating correct operation.

To test the classification performance of this system in a real application, we chose the task of seizure onset detection. We have implemented the proposed algorithm, for seizure detection application, in MATLAB and evaluated the detector performance using the dataset available in CHB-MIT EEG database downloadable from the Physionet website: <http://physionet.org/physiobank/database/chbmit/>.

EEG dataset from 3 patients, consisting of around 110 hours of data having 19 seizures, is used as test data. The seizure detector performance is characterized in terms of sensitivity, specificity and latency and we employed a leave-one-record-out cross-validation scheme for evaluation[4]. To compare the performance of the analog processor with a reference, we have also implemented a digital version of the algorithm using 100 tap FIR filters and energy detection as the gold standard. An example of a simulation for the whole processing chain in MATLAB using digital and analog processing is shown in Fig.6. The results of the experiment are summarized in Table I. It can be seen that though the latency and sensitivity of the analog processor is comparable to the digital one, its specificity is much worse. This has been traced to the first order filters used in this design and points to an obvious modification of increasing the order of the filters in the next design iteration. This analog processor can still be used as a wakeup engine for a power hungry but accurate digital processor or can be used to trigger data collection.

TABLE I. CLASSIFICATION RESULTS FOR SEIZURE ONSET DETECTION

Feature vector implementation	ELM Classification Results		
	Sensitivity	Specificity	Latency
Digital feature vector	100%	8	4.5s
Analog feature vector	95%	30	5.5s

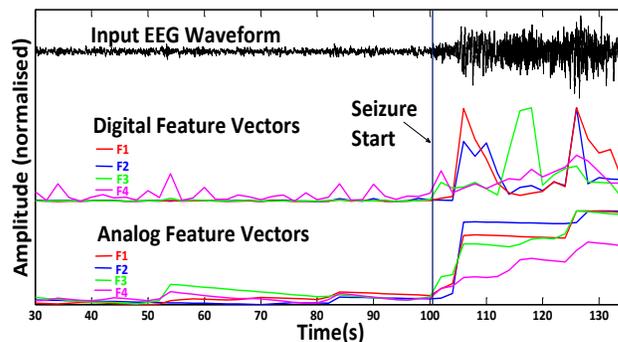


Fig.6: Simulation of whole processing chain showing feature vectors extracted using digital and analog processing. Absolute values are not shown.

### IV. CONCLUSION

We presented a reconfigurable smart sensor system for EEG acquisition and classification. The feature extracted from the raw signal is indicative of the signal strength in octave spaced frequency bands, with the actual frequency configurable according to application by current splitters. The features are classified using a spiking neuron implementation of ELM which utilizes the variability prevalent in VLSI to perform a computation intensive step in the algorithm. System simulations show that the analog features can be used for epileptic seizure detection.

### V. REFERENCES

- [1] G. Pfurtscheller, D. Flotzinger, and J. Kalcher, "Brain-computer interface—A new communication device for handicapped people," *J. Microcomput Appl.*, pp. 293–299, 1993.
- [2] A. Casson, D. Yates, S. Smith, J. Duncan, and E. Rodriguez-Villegas, "Wearable electroencephalography," *Engineering in Medicine and Biology Magazine, IEEE*, vol. 29, no. 3, pp. 44–56, Jun 2010.
- [3] Guang-Bin Huang, Qin-Yu Zhu, and Chee-Kheong Siew, "Extreme learning machine: a new learning scheme of feedforward neural networks," *IEEE Transactions on Neural Networks*, vol. 2, pp. 985–990, July 2004.
- [4] Shoeb, A. and J. Guttag, "Application of Machine Learning To Epileptic Seizure Detection." *Proceedings of International Conference on Machine Learning*, Haifa, Israel, 2010.
- [5] R.R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 958–965, June 2003.
- [6] T. Delbruck and A. van Schaik, "Bias generators with wide dynamic range," *Analog Integrated Circuits and Signal Processing*, vol. 43, pp. 247–268, 2005.
- [7] S. Zhak, M. Baker, and R. Sarpeshkar, "A Low Power Wide Dynamic Range Envelope Detector," *IEEE Journal of Solid State Circuits*, vol. 38, no. 10, pp.1750-1753, 2003.
- [8] A. Basu, S. Shuo, H. Zhou, G. Huang and M. Lim, "Silicon Spiking Neurons for Hardware Implementation of Extreme Learning Machines," *Neurocomputing*, accepted, 2012.
- [9] G. Indiveri et.al., "Neuromorphic Silicon Neuron Circuits," *Frontiers in Neuroscience*, vol. 5, DOI=10.3389/fnins.2011.00073, 2011.