Title	Integrated circuits design for neural recording sensor interface
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Citation	Xiaodan, Z., Lei, L., Tan, Y. S., Je, M., & Yeo, K. S. (2012). Integrated circuits design for neural recording sensor interface. 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp.17-20.
Date	2012
URL	http://hdl.handle.net/10220/16343
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Integrated Circuits Design for Neural Recording Sensor Interface

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***Abstract*—Neural signal recording is attracting more and more attention, as it provides an necessary approach to read brain activities, understand the brain operation and restore the lost motor function of the body. One of the most important modules in the neural recording system is the sensor interface IC, which captures, amplifies, filters, and digitizes the weak neural signal. In order to preserve free movement of the subject under testing and minimize the risk of infection, the sensor interface IC is usually implanted under the skin or skull with wireless transmission. The nature of the neural signal and its recording scenarios impose rigid design specifications to the sensor interface IC, such as low noise, low power, low cut-off frequency and minimum chip size. Many designs have been reported recently to tackle these challenges in neural recording system. In this paper, design techniques for neural recording sensor interface IC will be introduced, including the design of system architecture and neural amplifier. Methods to realize low power, low noise and low cut-off frequency are investigated. In addition, the methods to achieve system power and area optimization are also discussed.**

Keywords- neural recording, neural amplifier, biomedical circuit, low-noise, low-power, noise power trade-off, biomedical system optimization

I. INTRODUCTION

Millions of people are affected by paralysis in the world, which greatly impact their lives. Affected people are unable to move without losing their ability to think about moving [1]. Cortical neural prosthetics is a possible way to help paralyzed patients by recording their thoughts directly from the brain and decoding them to control external devices such as computer interfaces, robotic limbs and muscle stimulators [1]. By using implantable microelectromechanical system (MEMS) electrode arrays, neuroscientists and clinicians are able to observe the simultaneous activity of many neurons in the brain. This has allowed researchers to begin understanding how the brain processes information. Recent clinical trials with paralyzed human volunteers have shown that it is possible to develop neuroprosthetic devices—machines controlled directly by thoughts—if the activity of multiple neurons can be observed [1-3]. It proves that neural prosthesis based on intracortical neural recording could provide a valuable new neuro technology to restore independence for humans with paralysis. This finding has raised great expectation among the paralyzed patients for a neural prosthetic device. Other applications of neural recording include treating spinal cord injuries, deep brain stimulation to treat Parkinson's disease, etc.

One of the most challenging milestones in the advancement of neural prosthesis has been the development of the neural recording instrumentation. To successfully carry out long term multiunit recordings, the ideal system would be a fully implantable device which is capable of amplifying the signals and transmitting them to the outside world. Moreover, in order to study the brain state dynamics accurately, neuroscientist and clinician are interested in collecting the entire neural signals in raw data form without losing any information. This calls for the development of multi-channel neural recording interface chip which is able to perform simultaneous recording of neural signals over a large number of electrodes from the brain and the body. The miniaturization of these functional blocks presents significant circuit design challenges. In this paper, the general design techniques for neural recording sensor interface will be investigated and discussed.

II. CIRCUIT DESIGN CONSIDERATIONS

A. Properties of Neural Singals

Neuron is an excitable cell in the nervous system that processes and transmits information by electrochemical signaling. An action potential (AP), sometimes called "spike", occurs when a neuron sends information down an axon, away from the cell body. A group of neurons form a near DC background voltage, which is named local field potential (LFP). Depending on the probe characteristics and instruments used to recording neural information, the recorded signal may vary due to the difference in electrode-tissue interface and the electronic devices. Some commonly used neural signal characteristics are tabulated in Table 1.

TABLE 1. NEURAL SIGNAL CHARACTERISTICS[4-5]

Neural AP amplitude	Neural AP bandwidth	LFP amplitude	LFP bandwidth
50~500 μV	300 ~ 5kHz	Up to 5mV	1 ~100Hz

B. Characteristics of Neural Probes

A microprobe transduces a voltage in the extracellular space into a voltage at the amplifier input. Each amplifier in a multi-channel integrated circuit connects to its own signal probe (electrode). The probe impedance through the interface is a very important factor, which affects the amplifier attributes. The most common way to model this impedance is just a simple capacitor, where its capacitance is related to the area and material of the electrode. Process variations lead to large differences in probe capacitance and the variation of the probe impedance must be carefully considered during the amplifier design. A smooth metal surface produces 0.2pF/μm^2, and rougher surfaces may have five times this capacitance [6]. For example, a 36μm diameter probe (1000μm^2) may have a capacitance of 200pF, equivalent to 0.8MΩ impedance at 1kHz. The probe impedance is also affected by implementation time, as with the increase of the implementation time, the tissue will grow around the probe and encapsulate the electrode. This will block the neural signal acquisition and the electrode-tissue impedance may be doubled or even worse [7]. The electrode impedance and the input impedance of the neural amplifier will

form a voltage divider, which will reduce the amplitude of the captured signal. In order to obtain clear and non-degraded signal, large input impedance is needed for the neural amplifier, especially for long term monitoring.

C. Design Requirements for Sensor Interface IC

The neural recording system interfacing IC comes just after the neural multi-electrode array and is in charge of amplification, filtering, and digitization of the acquired neural signals. To study the brain state dynamics more accurately, the number of recording channel must be large enough. For the neuroscience research potentially improve SNR and reduce the power consumption are required. While for the clinical application, reduced the risk of infection and damage, improved user comfort level and enhanced mobility are very important. The detailed requirements for the design of the neural recording systems are illustrated as follows:

First of all, the main challenge is associated with the nature of neural signals. The amplitudes of these signals are in the order of tens of μV to a few mV and the frequencies span from DC to a few kHz. To capture such weak signals, the input referred noise of the analog front-end amplifier is a very critical parameter, especially in the low frequency range, where minimizing the flicker noise becomes an important work. Due to the signal weakness, the signal shall be amplified only in the frequency band of interest to minimize the interference from other frequency bands. Furthermore, a good analog front-end design needs to be able to accommodate the high dynamic range of different neural signals, since the action potential and local field potential can be as large as 1-2mV. Besides, the neural signals captured from the electrodes are usually accompanied by high DC component, which is resulted from the electrode-tissue interface. Hence, a high-pass filter will be necessary, whose cut-off frequency can be adjusted to sub 1Hz if LFP recording is required. Compact size calls for a fully integrated system. Battery-less operation is desirable, especially for the implantable devices, where the energy may be collected from human body or wireless power link. As a result, low voltage operation is an essential requirement for battery supply or energy harvesting device. Furthermore, ultra low power consumption is very critical to lengthen the battery lifetime and avoid any issue damage due to overheat. It is especially crucial for multi-channel applications, where slightly higher power consumption for an individual channel will result in much more heat dissipation if hundreds of channels are implemented. These strict requirements call for carefully planned system architecture to balance the trade-offs among these system specifications.

III. Circuit Deisgn Technique

A. System Architecutre

Conventional multi-channel biomedical recording sensor interface IC requires signal conditioning and digitization blocks, which are usually realized by low-noise preamplifier and analog to digital converter (ADC). The Successive Approximation Register (SAR) ADC is widely adopted in biomedical recording system due to its low power, high resolution and moderate speed. In order to maintain low power consumption and relax the wireless transmission burden, some reported design adopts data compression or spike detection algorithm [8-10]. However, this approach may lose some useful information and lead to inaccurate outcome. Therefore, complete and raw neural data is preferred for neural activity analysis and diagnosis. As a result, an ADC with at least 8 bit resolution will be necessary in neural recording system. Due to chip area restraint, one ADC is usually shared by multiple

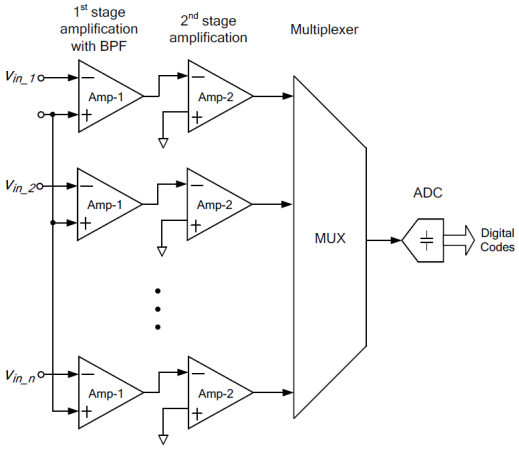

Figure 1 Typical system architecture for neural recording sensor interface.

analog front-end recording channels by employing an n-to-1 multiplexer [11-12]. A typical system architecture for neural recording sensor interface is shown in Figure 1.

In Figure 1, the signal conditioning and digitization are handled in a forward path. Recently, there are many reported designs using mixed analog and digital approach with feedback path to further enhance the system performance. For example, an ultra low high-pass corner frequency was realized using digital IIR filter and feedback network to the input of the preamplifier [13], and power line interference was suppressed by using 50/60 Hz notch filter, which was achieved using digital feedback [14]. By mixing both digital and analog blocks and applying feedback some restrict specifications can be achieved with easy and accurate control compared to system using only analog circuit. However, such mixed system architecture is still under investigation in term of system power and chip area. In addition, pseudo-digital system structure was also reported by conditionally reset or periodically reset certain signal nodes along the recording path to the reference voltage level [15]. This approach will effectively relax the maximum voltage swing requirement for both preamplifier and ADC, resulting in better signal linearity. However, further signal recovery is required to restore the original signal waveform.

B. Neural Amplifer Design

1) Amplifier topology

The neural amplifier comes the first after the neural probe array and provides sufficient gain to amplify the weak neural signals. According to the electrode and background noise floor and resolution of ADC, the gain of the neural amplifier ranges from several hundred to few thousand. The gain of the amplifier can be realized either by close loop or open loop configuration.

Close loop topology is more commonly used due to its accurate gain control and better signal linearity. The gain of the close-loop amplifier can be realized either by ratio of resistor or capacitor. However, as the resistor feedback configuration usually consumes large current, capacitive feedback is widely adopted to achieve low power consumption, as shown in Figure [16]. One problem with capacitive feedback configuration is that additional DC biasing circuit is needed. This is handled by the two serially connected PMOS transistors in Figure . Meanwhile, the two transistors also achieve ultra low high-pass corner frequency, and this will be explained in the later section. Another problem with the capacitive feedback is large chip size if accurate capacitor ratio is required, due to the relatively large unit area of the capacitor. Usually, the gain of such amplifier structure is 100 or less, and an additional second gain stage will be needed to get sufficient gain [4][9][12][17].

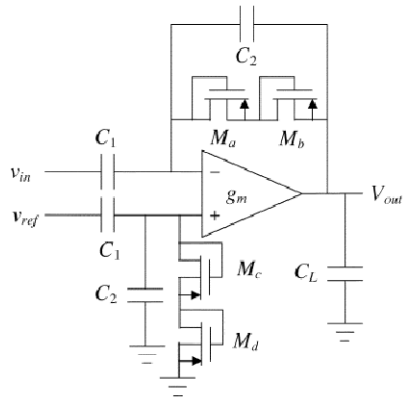

Figure 2. Typical neural amplifier structure adopting capacitive feedback

Open loop configuration is the other choice for neural amplifier. It has advantage in term of stability and usually consumes smaller chip area and current. However, it is very hard to obtain precise gain control and the signal linearity is usually degraded. A promising example with open loop amplifier is reported in [17]. The input transistors operate in weak inversion region, where the g_m value is linearly proportional to its drain current. The gain of the open loop amplifier can be well controlled by control the current passing through the transistors.

2) Low- noise and low-power technique

Noise figure is one of the most important benchmark for neural amplifier, since it determines the noise performance of the overall system. It is well known that low noise floor can be achieved by boosting large current. However, the tight power budget prohibits this approach. As a result, optimum noise to power trade off is becoming more and more important.

High current efficiency is one of the essential conditions to achieve good noise to power trade-off. MOS transistor operating in sub-threshold region produces larger g_m that is proportional to its drain current, giving better current efficiency compared to transistor in saturation region. Furthermore, in order to boost the input g_m, large portion of the total amplifier current should be allocated to the input branches. Meanwhile, the noise from the non-gain element such as the load transistor and the current mirror should be minimized, by applying small biasing current or choosing small width and large length for their gate dimensions. In addition, using both NMOS and PMOS transistors as input pair will effectively increase the input g_m and lower the thermal noise floor [12].

Neural signal occupies the bandwidth from hundred Hz up to 10kHz, where the flicker noise is not a dominant noise source and chopper amplifier is usually not employed in neural recording system. However, for certain CMOS process technology, flicker noise may be prominent in this frequency band, so PMOS transistor is preferred; and for some other technologies, flicker noise may not be an issue, and NMOS transistor is commonly adopted as it provides large g_m and less noise with a given current. Sometime, LFP may need to be included in the amplifier bandwidth, which will induce considerable flicker noise in the low frequency range. However, flicker noise is still not the dominant noise source compared to thermal noise, and it can be suppressed by choosing suitable input devices and proper gate area.

Neural amplifier noise is contributed mainly from two noise sources-thermal noise and flicker noise. Limiting the amplifier bandwidth to fit with the neural signal bandwidth is another way to effectively reduce the noise figure from both of the two noise sources, as the noise outside the amplifier bandwidth will not be amplified and it contributes very insignificant portion to the total noise level.

3) Low cut-off frequency

As the frequency spectrum of the neural signal occupies low frequency range, especially when the LPF signal is considered, the high-pass corner frequency of the neural amplifier can reach as low as sub-1Hz. Using passive devices to achieve such low cut-off frequency requires external components due to the chip area limitation. This will greatly increase the electronics size especially for large number of channels. Besides the approach mention previously which uses feedback of digital filter, R.R. Harrison proposed an active pseudo-resistor structure where MOS-bipolar transistors are used to generate a huge resistance in the order of GΩ, as shown in Figure . Thereby fully integrated sensor interface IC can be realized using on-chip capacitors. This approach provides a promising and effective way to design biomedical amplifiers with low power, low noise and small area, and has been borrowed by many other designs. Some of them modify the pseudo-resistor structure to get tunable resistance as shown in Figure (a) [17], so as to control the cut-off frequency of the amplifier. One problem associated with most of the published pseudo-resistor structure is its non-linear resistance with the change of the amplitude and polarity of the voltage across it. The design reported in [17] improves the conventional tunable pseudo-resistor topology by souring the control voltage locally instead of externally, as shown in Figure (b). The linearity of the generated resistance was improved significantly, as well as the signal distortion of the neural amplifier.

Another approach to realize the ultra low cut-off frequency with on-chip component is adopting a small transconductance OTA in the feedback path as shown in Figure 4 [19]. In order to avoid large capacitor, the g_m of the feedback OTA must be very small to achieve the small cut-off frequency. Some technique such as current cancellation scheme [20] or series-parallel current division structure [21] can be applied to realize the ultra small g_m OTA. Compared to the pseudo-resistor approach, where it is difficult to get accurate resistance value, this method is more accurate and easy to control the cut-off frequency by tuning the biasing current. However, it will be a great challenge to obtain small and precise reference current. In the reported design, the current consumption for the OTAs are from 8.8pA to 48pA, but the method to obtain such small current was not introduced and further investigation and experiment on this issue will be needed.

One concern with the ultra-low cut-off frequency is the

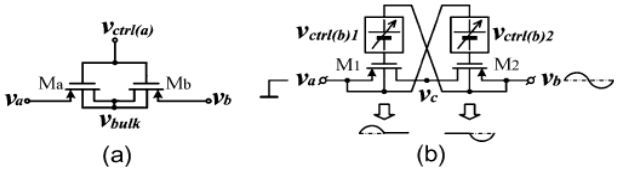

Figure 3. Tunable pseudo-resistor structure [17].

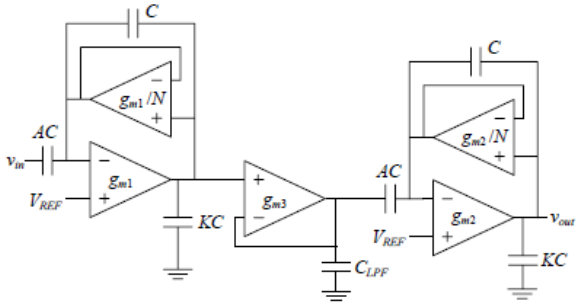

Figure 2 Neural amplifier with small g_m OTA in the feedback path [19].

slow settling time of the system due to the large RC constant. It is common to take few minutes to get the system on track during start-up. Other disruptions such as change of electrode position or loose contact between electrode and tissue will also take long time for the system to settle down. In order to deal with such situation, the common practice is to add one reset control to the neural amplifier, so that the amplifier can be brought to normal working condition quickly when any disturbance presents [9][12].

C. System Optimization

Recently reported designs have put much effort on reducing the power consumption of individual functional block, such as low-noise preamplifier and ADC, which can be realized with few μW power consumption [12]. However, little has been done in optimizing overall system power consumption. For example, a preceding buffer of ADC can draw tens of μW power, simply overriding the power of preamplifier and ADC, resulting in a high total power consumption of the system [12]. A power and area optimal system requires careful plan to achieve each specification. Integrating as many functional block as possible into one module may not necessarily result in small system power, as more power may be consumed by other blocks to compensate the performance degradation of the integrated module [22]. Total system gain is usually achieved by two-stage amplification to optimize area and power usage. Due to the narrow bandwidth of the neural amplifier, a dedicated buffer is usually necessary before the ADC to drive the S/H capacitor [24]. Unity gain or low gain of 2 may be applied to the buffer, but higher gain is highly non-desirable for the buffer as power consumption will increase dramatically. In currently published designs, the system bandwidth is usually determined by the first pole of the neural amplifier. However, this will require relatively large Miller or load capacitor to push the pole to low frequency since the input g_m of the neural amplifier is quite large, resulting in large chip area. An alternative way is to set the system bandwidth at the second gain stage, where a small g_m is acceptable [25]. This will effectively relax the bandwidth requirement of the first stage and minimize the area of the system. Other system optimization methods such as sequentially turning on multi-channel recording front-end [12], putting unnecessary blocks in sleep modes [22], and reducing the system bandwidth or ADC resolution when accurate recording is not required [17], etc, are also adopted in the reported designs.

IV. CONCLUSION

In this paper, the general design guidelines for neural recording sensor interface are discussed to tackle various design challenges imposed by the fully integrated implantable miniature device. In the future, more effort is needed to focus on practical issues such as implementation safety control, to make the highly integrated micro-system more robust and safer for long term monitoring.

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