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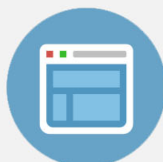

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Recovery from ultraviolet-induced threshold voltage shift in indium gallium zinc oxide thin film transistors by positive gate bias

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The effect of short-duration ultraviolet (UV) exposure on the threshold voltage (V_{th}) of amorphous indium gallium zinc oxide thin film transistors (TFTs) and its recovery characteristics were investigated. The V_{th} exhibited a significant negative shift after UV exposure. The V_{th} instability caused by UV illumination is attributed to the positive charge trapping in the dielectric layer and/or at the channel/dielectric interface. The illuminated devices showed a slow recovery in threshold voltage without external bias. However, an instant recovery can be achieved by the application of positive gate pulses, which is due to the elimination of the positive trapped charges as a result of the presence of a large amount of field-induced electrons in the interface region. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4830368]

Thin film transistor (TFT) based on amorphous indium gallium zinc oxide (IGZO) is promising in the application of next generation flat-panel display (FPD) due to its high field-effect mobility, low thermal budget, and good stability.[1–3] In the display application, device instability induced by both light illumination and gate bias could be a serious issue.[4,5] On the other hand, ultraviolet (UV) light is commonly used in the cleaning to remove the particles and impurities on the surface in the TFT fabrication.[6] It has been reported that an UV exposure can cause a shift in the threshold voltage of IGZO TFT,[7,8] which poses a problem to normal device operation. In this work, we demonstrate that an instant recovery can be achieved by the application of positive gate pulses. The mechanisms of the UV-induced instability and the recovery have been investigated in this work.

The fabrication process of the TFT devices started on a heavily doped n-type Si substrate with a resistivity of less than 0.001 Ω-cm, which served as the gate electrode. A 30 nm Al_2O_3 gate insulator was first deposited with the atomic layer deposition (ALD) process at 250 °C using Trimethylaluminium (TMA) of 99% in purity. Subsequently, a 50 nm thick IGZO film was sputtered onto the Al_2O_3 thin film via radio frequency (RF) sputtering. The IGZO target is 2 inches in diameter and 3 mm thick, with mole ratio of In:Ga:Zn:O = 1:1:1:4. The sputtering was carried out in the argon/oxygen ambient with RF power of 100 W during sputtering. The chamber pressure was maintained at 3 mTorr. The pattern of a-IGZO channel was delineated through standard photolithography followed by the wet etching process. Finally, Ti/Au (10 nm/200 nm) pads were deposited by electron-beam evaporation to form the source and drain electrodes. The channel length (L) and channel width (W) were 20 μm and 20 μm, respectively. A schematic cross-section diagram of the TFT is shown in the inset of Fig. 1. Current-voltage (I–V) characteristics of the TFTs were measured with a Keithley 4200 semiconductor characterization system at room temperature. A HAMAMATSU LC8 365 nm UV spot light source with power density of 5 mW/cm^2 was used in the UV exposure experiments. The gate electrode of the TFTs was floating during the UV illumination (no significant difference in the UV effect between gate floating and gate grounding was observed).

To examine the stress effect of the gate bias (V_G) on the TFT, +10 V and −10 V were applied to the gate of the device, respectively, for 5 min without any exposure to UV illumination, with the source and drain maintained at zero bias. The transfer characteristics of the TFT before and after the applications of the positive and negative biases are shown in Fig. 1. As can be observed in the figure, the gate bias did not produce a significant change in the transfer characteristic of the TFT, indicating that trap generation and/or charge trapping in the TFT due to the gate bias stress were negligible. Therefore, the gate stress effect can be ignored for the UV-exposure study discussed below.

The experiment of UV exposure with various durations was conducted on an as-fabricated TFT. The transfer characteristic of the TFT was measured in dark after each UV exposure. Figure 2(a) shows the transfer characteristics of the TFT before UV exposure and after the exposures of 3, 10, and 60 s. As shown in the figure, an UV exposure led to a shift in the transfer characteristic to the negative voltage side, showing a decrease in the threshold voltage of the TFT. Figure 2(b) shows the threshold voltage shift (ΔV_{th}) as a function of the exposure duration. As can be observed in the figure, an exposure led to a decrease in the threshold voltage, with a fast decrease rate for short exposure durations

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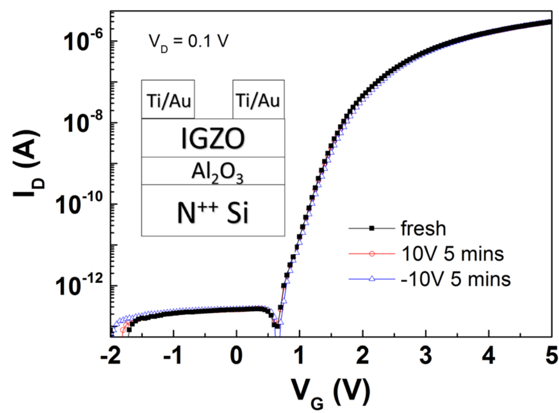

FIG. 1. Transfer characteristics of the TFT measured at the source-drain voltage of 0.1 V before and after constant gate bias stresses at +10 V and −10 V, respectively, for a duration of 5 min. The inset shows the schematic cross-sectional diagram of the bottom gate IGZO TFTs with Al_2O_3 gate dielectric.

($<\sim$10 s) and a slow decrease rate for longer durations ($>\sim$10 s).

The negative shift in the threshold voltage could be attributed to the positive charge trapping at the channel/dielectric interface or in the dielectric layer and the increase in the free electron concentration in the channel. In the first mechanism, electron-hole pairs are generated by UV illumination, and the photon-generated holes are trapped at the channel/dielectric interface or in the dielectric layer, leading to a decrease in the threshold voltage after the UV light is off.[9–11] In the second mechanism, the concentration of free electrons in the channel layer is increased as a result of the creation of oxygen vacancies, which act as donors providing free electrons in the channel layer, during UV illumination. The threshold voltage decreases with increasing free-electron concentration because the IGZO TFT has an n-type conduction channel. The creation of oxygen vacancies during UV illumination could be due to the reaction of the UV-activated oxygen from the ambient with the oxide layer[6] or the direct creation of the oxygen vacancies by UV illumination.[10] The two mechanisms have been examined with the experiments described below.

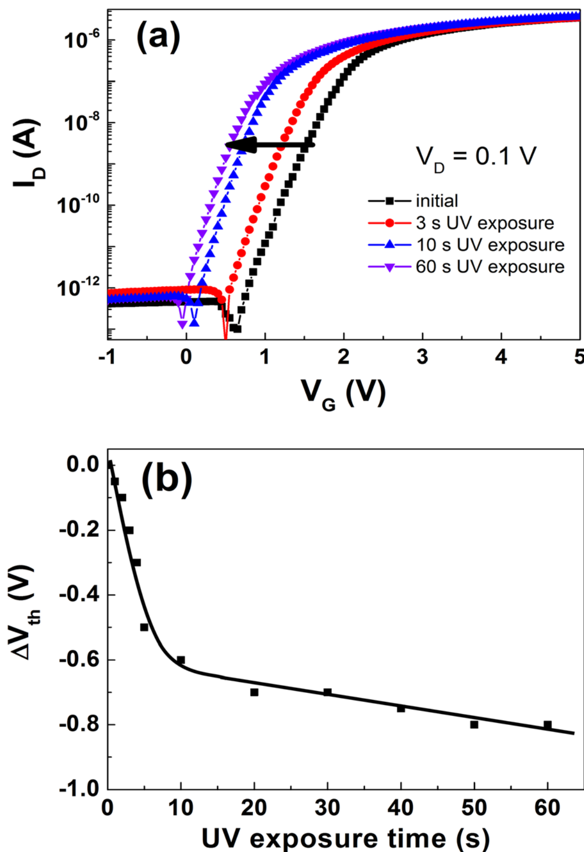

FIG. 2. (a)Transfer characteristics of the fresh device and after the UV exposures of 3 s, 10 s, and 60 s. (b) Threshold voltage shift (ΔV_{th}) as function of UV exposure time.

The second mechanism can be tested by examining the exposure duration dependence of the resistivity of the IGZO channel layer. The resistivity of the IGZO layer deposited on a glass substrate was measured with a four-point probe in dark. Figure 3 shows the channel resistivity as a function of the UV exposure duration. It can be observed from the figure that there was no significant change in the resistivity within 160 s of UV exposure. This indicates that the UV exposure did not produce a significant change in the free-electron concentration of the channel. In contrast, as shown in Fig. 4, an exposure of 120 s caused a large decrease of 0.75 V in the threshold voltage of the TFT. Therefore, the UV exposure-induced decrease in the threshold voltage cannot be attributed to the increase of the free-electron concentration as a result of oxygen vacancy generation in the oxide layer by UV illumination.

On the other hand, if the negative shift in the threshold voltage is due to the positive charge trapping at the channel/dielectric interface or in the dielectric layer, the post-exposure threshold voltage is expected to show a very slow change with waiting time. This was indeed observed in the waiting-time experiment. In the experiment, the TFT was first exposed to UV illumination for 120 s, and then its threshold voltage was monitored in dark for an extended period of time without applying any electrical bias. (The device was kept in a dry cabinet to ensure that the device was not exposed to any UV light in the environment during the extended period.) Figure 4 shows the waiting-time dependence of the post-exposure threshold voltage at room temperature. As can be seen in this figure, the recovery in the threshold voltage was very slow, e.g., the waiting time of 1×10^6 s led to a recovery of only 0.1 V in the threshold

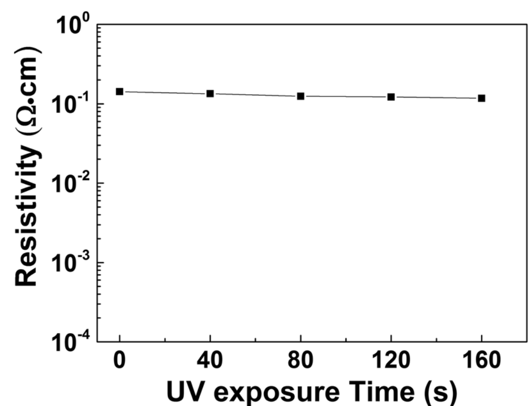

FIG. 3. Resistivity of the IGZO layer versus UV exposure time.

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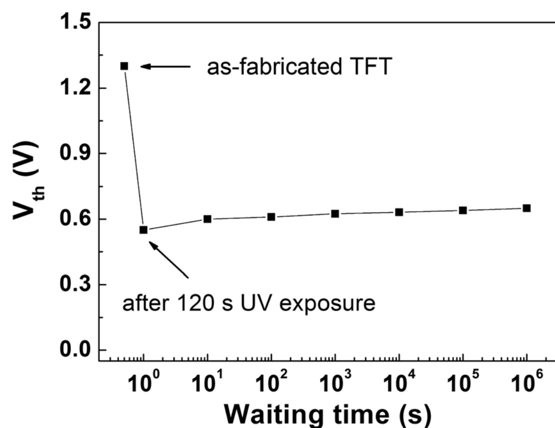

FIG. 4. Post-UV exposure V_{th} measured in dark at various waiting times. The device was first exposed to UV illumination for 120 s.

voltage. It is believed that the slow recovery in the threshold voltage was due to the release of the positive charges trapped at the channel/dielectric interface or in the dielectric layer, which was a very slow process at room temperatures without the assistance of applied fields.

In contrast to the very slow recovery under the condition without applied bias, the threshold voltage could be easily recovered with a positive gate pulse. Figure 5 shows the transfer characteristics of the TFT with the following sequent conditions, including the as-fabricated device, after UV exposure of 120 s, after a waiting time of 10^5 s in dark, and after applications of voltage pulses of -10 V/1 s and $+10$ V/1 s. As shown in Fig. 5(a), the 120 s UV exposure caused a large shift in the transfer curve towards a lower threshold voltage. The device was then kept in dark for 10^5 s, and only a small recovery was observed (Fig. 5(b)). Subsequently, a -10 V pulse with 1 s duration was applied to the gate electrode; no significant change in the transfer characteristic was observed (Fig. 5(c)). However, when a $+10$ V pulse with 1 s duration was applied to the gate electrode, the transfer curve was shifted back to the original state immediately (Fig. 5(d)), showing that the UV-induced shift could be fully recovered by the application of the positive voltage pulse. As IGZO is an n-type metal oxide semiconductor, electrons are the majority carriers in the IGZO channel layer. Electrons were accumulated in the interface region under the positive gate voltage. Therefore, the V_{th} recovery is expected from the neutralization of the positive charges (i.e., holes) trapped in the interface region as a result of the presence of a large amount of free electrons in the region. Our result indicates that the application of a positive gate pulse is a simple and effective way to recover from the UV-induced threshold voltage shift.

An investigation of the influence of pulse voltage/duration on the recovery performance was conducted. Figure 6(a) shows the threshold voltage recovery after 120 s UV exposure as a function of the gate bias duration with the pulse voltage fixed at $+10$ V. ΔV_{th} just after the UV exposure was ~ -0.65 V; the magnitude of the ΔV_{th} decreased with the pulse duration; and it reached 0 V when the pulse duration

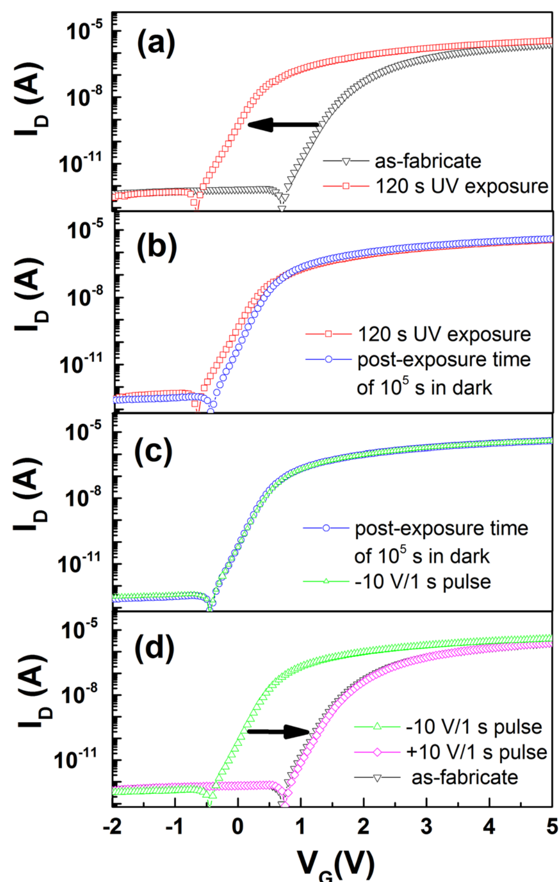

FIG. 5. Transfer characteristics of the TFT with the following sequent conditions, including the as-fabricated device, after UV exposure of 120 s, after a waiting time of 10^5 s in dark and after application of voltage pulses of -10 V/1 s and $+10$ V/1 s.

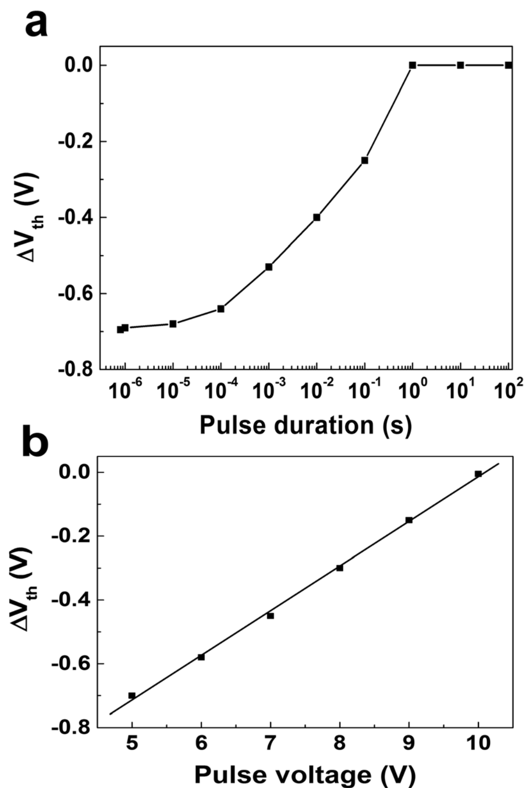

FIG. 6. (a) Threshold voltage recovery as a function of the gate pulse duration with the pulse voltage fixed at $+10$ V (ΔV_{th} just after the 120 s UV exposure was ~ -0.65 V). (b) Threshold voltage recovery as a function of pulse voltage with pulse duration fixed at 1 s (ΔV_{th} just after the 120 s UV exposure was ~ -0.70 V).

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was 1 s, showing that the device was fully recovered. No positive V_{th} shift was observed for the pulse durations longer than 1 s. Figure 6(b) shows the threshold voltage recovery as a function of pulse voltage with pulse duration fixed at 1 s. The threshold voltage shift induced by the 120 s UV exposure is ~ -0.7 V; this value remained unchanged after the application of the pulse of +5 V/1 s. However, the magnitude of ΔV_{th} decreased linearly with the pulse voltage, and it reached ~0 V at the pulse voltage of 10 V.

In conclusion, the negative threshold voltage shift caused by UV exposure is attributed to the positive charge trapping in the dielectric layer and/or at the channel/dielectric interface. The illuminated TFTs show a slow recovery in threshold voltage without external bias. However, an instant recovery can be achieved by the application of positive gate pulses, which is due to the elimination of the positive trapped charges as a result of the presence of a large amount of field-induced free electrons in the interface region.

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