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<td><strong>Author(s)</strong></td>
<td>Fan, J.; Tu, L. C.; Tan, Chuan Seng</td>
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High-Al2O3 material in low temperature wafer-level bonding for 3D integration application

J. Fan, L. C. Tu, and C. S. Tan

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High-$\kappa$ Al$_2$O$_3$ material in low temperature wafer-level bonding for 3D integration application

J. Fan, L. C. Tu, and C. S. Tan

MOE Key Laboratory of Fundamental Physical Quantities Measurement, School of Physics, Huazhong University of Science and Technology, Wuhan 430074, People’s Republic of China

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This work systematically investigated a high-$\kappa$ Al$_2$O$_3$ material for low temperature wafer-level bonding for potential applications in 3D microsystems. A clean Si wafer with an Al$_2$O$_3$ layer thickness of 50 nm was applied as our experimental approach. Bonding was initiated in a clean room ambient after surface activation, followed by annealing under inert ambient conditions at 300 $^\circ$C for 3 h. The investigation consisted of three parts: a mechanical support study using the four-point bending method, hermeticity measurements using the helium bomb test, and thermal conductivity analysis for potential heterogeneous bonding. Compared with samples bonded using a conventional oxide bonding material (SiO$_2$), a higher interfacial adhesion energy ($\sim$11.93 J/m$^2$) and a lower helium leak rate ($\sim$6.84 $\times$ 10$^{-10}$ atm.cm$^3$/sec) were detected for samples bonded using Al$_2$O$_3$. More importantly, due to the excellent thermal conductivity performance of Al$_2$O$_3$, this technology can be used in heterogeneous direct bonding, which has potential applications for enhancing the performance of Si photonic integrated devices. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [http://dx.doi.org/10.1063/1.4867089]

I. INTRODUCTION

In order to augment Moore’s law scaling, three-dimensional (3D) integration technology has been considered as the most plausible choice to substitute for the two-dimensional architecture, as it can provide a higher connection density and better performance. Furthermore, and maybe the most attractive, this technology enables the possibility of heterogeneous integration of disparate functional blocks, such as micro-electro-mechanical system (MEMS) sensors and complementary metal-oxide-semiconductor (CMOS) circuit integration in a vertical and seamless way, as well as in InP-Si heterogeneous direct bonding to enhance the performance of Si photonic integrated devices.

A great number of materials have been applied to achieve wafer-level bonding for 3D integration circuit (IC) applications; the most popular include polymer adhesive materials, intermetallic compounds, diffusion metal materials (such as gold, aluminum, and copper), and silicon oxide. Amongst these different materials, copper and oxide are most attractive as they are widely used as the interconnectors and interlayer dielectrics based on CMOS backend processing. Some studies have indicated that Cu-to-Cu wafer-level thermo-compression bonding is typically performed at 350–400 $^\circ$C. With developments in surface treatments, especially the application of pre-bonding passivation based on a self-assembled monolayer (SAM), high bonding quality can be obtained at an adequately low temperature (typically 300 $^\circ$C or below). However, the application of this bonding technology is hindered by its strict bonding conditions, which require the wafer pair

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to be held for certain duration while heating and pressing. Oxide fusion bonding can be achieved by rapid prebonding followed by an annealing process which can maximize the throughput. In recent years, high-κ dielectric materials have been considered the mainstream candidate to increase gate capacitance without the consequent gate leakage effects. Some thin layers of high-κ dielectric materials used in low temperature PE-TEOS bilayer oxide bonding, such as Al2O3, HfO2, and TiO2,19 have already been investigated to achieve high bonding strength for a given annealing temperature and duration. Even though low temperature bonding of the high-κ dielectric material Al2O3 has been explored rather extensively in 3D ICs, further in-depth study is required to use monolayers of high-κ dielectric materials in low temperature bonding and to understand bonding strength, hermetic sealing and thermal conductivity for potential applications in 3D integration.

This paper presents an investigation of bonding quality that consists of mechanical support and a hermetic seal with low temperature Al2O3-Al2O3 fusion bonding. SiO2-SiO2 direct bonding (SDB) was also included for comparison. The four-point bending test was used for the quantitative bonding strength analysis through interfacial adhesion energy measurements. The interfacial adhesion energy achieved with Al2O3 was much better than that obtained with the conventional SiO2 layer. Helium leak rate measurements, which are based on the specifications described by the MIL-STD-883E standard, were applied for hermeticity tests. Excellent helium leak rates, which were at least 10 times smaller than the reject limit (5 × 10^-8 atm.cm^3/sec), were observed. Thermal conductivity analysis showed that the high-κ dielectric (Al2O3) material layer presented excellent heat dissipation.

II. EXPERIMENT

Silicon wafers (6" in diameter, thickness of 625 μm, p-type, (100), resistivity of 10–15 Ω.cm) were used in the bonding experiment. Wafer cleaning was first performed in piranha solution (H2O2 : H2SO4 = 1:3 by volume) followed by a rinse in DI water. Then, in order to obtain a hydrophilic surface to facilitate the Al2O3 deposition process, ultraviolet ozone (UVO) exposure was performed at room temperature in an ambient atmosphere for 3 min. Subsequently, a 50 nm layer of Al2O3 was deposited by atomic layer deposition (ALD) using the precursor trimethylaluminum (TMA). Since low temperature bonding was desired, the wafers with a thin layer of Al2O3 were activated by short (~15s) oxygen plasma exposure to obtain a low surface contact angle. In order to hydroxylate the wafer surfaces with hydroxyl (OH) groups for hydrophilic bonding, the wafers were rinsed in DI water and dried with N2 gas. The wafer pairs were brought into contact and bonded spontaneously on a commercial double-side aligner at room temperature. After bonding, the wafer pairs were annealed in an atmospheric N2 ambient for 3 h at 300 °C to form stronger covalent Al-O-Al bonds.

III. RESULTS AND DISCUSSION

Fig. 1 illustrates the atomic force microscope (AFM) 3D surface roughness scan images of the Al2O3 surfaces after the surface activation process. The RMS roughness of the samples was 0.25 nm,
which was estimated based on the 5 \( \mu \text{m} \times 5 \mu \text{m} \) AFM scan images. The water contact angle was measured by a water droplet contact angle goniometer. As indicated in Fig. 2, the contact angle was about 3\(^\circ\), which indicates a suitable hydrophilic surface.

The four-point bending method was applied for bonding strength analysis. The wafer pair was diced into rectangular pieces for measurement after bonding. Fig. 2 presents a typical measurement process. The four-point bending test begins with an incision in the top wafer as a pre-crack notch. If the force loaded on two inner load pins reaches a critical level \( F_c \), the pre-crack will initiate a new interfacial crack on bonding interface. Then, the crack will spread at the bonding interface and the force loaded will almost maintain at a plateau value \( F_p \). The interfacial adhesion energy \( G \), which refers to the bonding strength, can be calculated as follow:\(^4\),\(^20\)

\[
G = \frac{21 \times (1 - \nu^2) \times F_p^2 \times L^2}{16 \times E \times b^2 \times h^3}
\]

where \( \nu \) is Poisson’s ratio of silicon, \( E \) is the elastic modulus of silicon, \( L \) is the space between the inner and outer load pins, \( b \) is the specimen width, and \( h \) is the thickness of the silicon wafer.

In order to set up a benchmark for comparison with Al\(_2\)O\(_3\)-Al\(_2\)O\(_3\) wafer-level bonding, a similar pair of wafers coated with 50 nm of PETEOS for SiO\(_2\)-SiO\(_2\) fusion bonding was included. Fig. 3 shows the comparison of the measured interfacial adhesion energy. It must be noted that the interfacial adhesion energy of Al\(_2\)O\(_3\)-Al\(_2\)O\(_3\) bonding was at least six times greater than that of SiO\(_2\)-SiO\(_2\) bonding. It was much greater than the critical bond strength required (5 J/m\(^2\)) during subsequent processes such as grinding.\(^21\)

According to the theoretical research work by Tao et al.,\(^22\) the minimum internal volume for a helium leak rate test based on the MIL-STD-883E standard (method 1014.10) is 10\(^{-3}\) cm\(^3\). Cavities with a volume of about 1.4 \( \times \) 10\(^{-3}\) cm\(^3\) and seal rings with a depth of 120 \( \mu \text{m} \) were formed by deep reactive-ion etching (DRIE). Cross-sectional scanning electron microscopy (SEM) images of the
chips are shown in Fig. 4. The width of seal ring was about 50 μm. As shown in Fig. 4, no cracks were observed after bonding. The hermetic test consists of a fine leak test and a gross leak test. All samples under test were subjected to the gross leak test using a standard bubble test with fluorocarbon liquids (FC-72, FC-43) according to the MIL-STD-883E standard. In our study, all samples successfully passed the gross leak test. No bubbles were observed during the test. The helium leak rate test, which was used as the fine leak test for leak rates below $10^{-4}$ atm.cm$^2$/sec, consists of helium bombing and helium leak rate detection. Twenty samples were first placed in a helium over-pressure (75 Psi) chamber for an exposure time over 2 h (helium bombing). Subsequently, the samples were unloaded from the helium bombing chamber and tested by a mass spectrometer. Samples using PETEOS for SiO$_2$-SiO$_2$ fusion bonding were also included for comparison. Fig. 5 shows the comparison of the helium leak rate for samples with different bonding materials. All the samples presented an excellent helium leak rate which was at least one order of magnitude smaller than the reject limit ($5 \times 10^{-8}$ atm.cm$^2$/sec) prescribed by the MIL-STD-883E standard. However, it can be clearly
FIG. 5. Comparison of the helium leak rate for samples with different bonding materials.

FIG. 6. Infrared image of heterogeneous bonding of the 2'' InP wafer to the 6'' Si wafer.
TABLE I. Effective thermal conductivity for the bilayer structure.

<table>
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<tr>
<th>Bilayer structure</th>
<th>Intermediate layer (nm)</th>
<th>50</th>
<th>100</th>
<th>500</th>
<th>1000</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Si Substrate (μm)</td>
<td></td>
<td></td>
<td></td>
<td>625</td>
</tr>
<tr>
<td>K_{eff_Al2O3} (W m(^{-1}) K(^{-1}))</td>
<td>148.95</td>
<td>148.91</td>
<td>148.53</td>
<td>148.06</td>
<td></td>
</tr>
<tr>
<td>K_{eff_SiO2} (W m(^{-1}) K(^{-1}))</td>
<td>147.81</td>
<td>146.63</td>
<td>137.86</td>
<td>128.29</td>
<td></td>
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</table>

Fig. 7 presents the heat transfer simulation results for different intermediate layer thicknesses.

observed that the samples using Al\(_2\)O\(_3\)-Al\(_2\)O\(_3\) bonding (6.84 \times 10^{-10} \) atm.cm\(^3\)/sec) presented better hermeticity than those using PETEOS SiO\(_2\)-SiO\(_2\) bonding (8.67 \times 10^{-10} \) atm.cm\(^3\)/sec). Comparing with the results on hermetic packaging in the literature\(^3,^{23-26}\) these results present comparable or even better hermeticity than reported values.

The most attractive advantage of Al\(_2\)O\(_3\)-Al\(_2\)O\(_3\) bonding technology is heterogeneous integration. Since it is very difficult to obtain high quality III-V heteroepitaxy layer growth on a silicon substrate, bonding technology is very important for III-V compound semiconductor on non-lattice matched Si substrate integration.

Fig. 6 presents 2" InP wafer to 6" Si wafer bonding using Al\(_2\)O\(_3\) as the intermediate layer. Bonding was achieved at room temperature followed by a 300 °C annealing step for 3 hr. Although SiO\(_2\) is the most common intermediate layer for III-V epitaxial layer transfer, poor heat dissipation is always identified as the bottleneck in the development of Si photonic devices. Table I summarizes the effective thermal conductivity for the bilayer system. When the thickness of the intermediate layer was varied from 50 nm to 1 μm, the difference in effective thermal conductivity between the Al\(_2\)O\(_3\)/Si system and SiO\(_2\)/Si system changed from ~1 to ~20. As a direct result of the decrease in effective thermal conductivity, the heat will accumulate in the bilayer system, which will result in a rapid system temperature increase. Fig. 7 shows the COMSOL simulation results for bilayer systems with different intermediate layer thicknesses. In order to simplify the simulation, the thickness of
the Si substrate and the power density were fixed at 100 μm and 10,000 W/cm², respectively. The temperature increase was not significant (<10°C) until the thickness increased to 100 nm. Nevertheless, the surface temperature of Al₂O₃ was still much lower than that of SiO₂. It was clearly observed that the temperature increased rapidly when the SiO₂ layer was thicker. If the thickness increased to 1 μm, the surface temperature of SiO₂ rapidly reached around 105°C. Meanwhile, the surface temperature of Al₂O₃ remained at a very low level (~36°C). There was hardly temperature increase when using Al₂O₃. In an earlier study, the measurement results obtained by an Au Kelvin structure for thermal characteristic tests verified that high-κ dielectric (Al₂O₃) materials provide more effective heat dissipation.

IV. SUMMARY AND CONCLUSION

This paper systematically investigates Al₂O₃-assisted low-temperature wafer level bonding. The research work consisted of three parts: mechanical support, hermetic sealing and heterogeneous bonding. As compared with SiO₂-assisted hydrophilic bonding, the high-κ dielectric (Al₂O₃) material had many advantages, such as higher bonding strength, better hermeticity, and more effective heat dissipation for the III-V compound to Si heterogeneous bonding. The experimental results show that Al₂O₃ is an ideal substitute for conventional dielectric (SiO₂) use in the semiconductor industry.

ACKNOWLEDGMENTS

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