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Kalya Shubhakar, Kin Leong Pey, Michel Bosman, Sunil Singh Kushvaha, Sean Joseph O'Shea, Miyuki Kouda, Kuniyuki Kakushima, and Hiroshi Iwai

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Leakage current and structural analysis of annealed HfO₂/La₂O₃ and CeO₂/La₂O₃ dielectric stacks: A nanoscopic study

Kalya Shubhakar
Division of Microelectronics, School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore 639798 and Engineering Product Development (EPD), Singapore University of Technology and Design (SUTD), Singapore 138682

Kin Leong Pey
Engineering Product Development (EPD), Singapore University of Technology and Design (SUTD), Singapore 138682

Michel Bosman, Sunil Singh Kushvaha, and Sean Joseph O’Shea
Institute of Materials Research and Engineering (IMRE), A*STAR (Agency for Science, Technology and Research), 3 Research Link, Singapore 117602

Miyuki Kouda, Kuniyuki Kakushima, and Hiroshi Iwai
Tokyo Institute of Technology, 4259 Nagatsuta, Midoriku, Yokohama 227-8502, Japan

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Grain boundaries in the polycrystalline microstructure of post-annealed high-κ (HK) dielectrics are a major limitation in the reliability of HK dielectrics used for advanced CMOS technologies. Another challenge in the field of HK dielectrics is to ensure higher drain drive current in CMOS, while maintaining low leakage current. In this work, the authors demonstrate enhanced performance of HfO₂ and CeO₂ dielectrics by incorporating lanthanum. The resulting stacks show promising dielectric characteristics with reduced leakage current and uniform (amorphous) crystal structure. The improved HK characteristics were shown to occur even over nanometer-length scales using scanning probe microscopy and transmission electron microscopy, in agreement with previous studies based on micron-scale device-level measurement. © 2014 American Vacuum Society.

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I. INTRODUCTION

Hafnium (Hf)-based oxides have been the most suitable replacements for SiO₂/SiON in high-κ (HK) based CMOS technology applications.¹⁻³ CeO₂ is another promising HK dielectric, especially for future CMOS technology nodes, considering its good dielectric strength (κ ~ 20–25), large bandgap (Eg ~ 5.5 eV), high thermal and chemical stability, and low lattice mismatch with silicon substrates.⁴⁻⁵ Both HfO₂ and CeO₂ are studied in this work, as well as the addition of lanthanum (La) into the gate dielectric stack.

Lanthanum-incorporated HK dielectrics are suitable candidates for direct deposition on Si substrates.⁴⁻⁸ The lanthanum oxide (La₂O₃) itself has good dielectric properties (κ = 25–30, bandgap (Eg) ~ 5.5 eV), but it is also significant to note that lanthanum forms a La-silicate interfacial layer (IL) (κ ~ 14) on Si, after high-temperature annealing up to 1000 °C.⁹⁻¹¹ Thus, direct deposition is possible without the need of IL of SiO₃ₓ<sub>2</sub>_, enabling more aggressive scaling of the equivalent oxide thickness (EOT).

La₂O₃ is chemically unstable in ambient air and is rapidly transformed (in a few hours) to La(OH)(OH)₃, leading to layer swelling.¹⁰ Fortunately, when a La₂O₃ layer is inserted at the HK/Si interface, such hydration is not observed.⁵⁻⁶ Capping layers can also be used to protect the HK and it has been reported that CeO₂ is the best capping layer for La₂O₃.⁵,¹²

La incorporation into HK dielectrics has attracted much attention due to the beneficial effects of improved EOT and direct deposition. Further, La-incorporated HK shows additional improvements at the device level, such as increased crystallization temperature, reduced leakage current, and an increased dielectric constant “κ” value.⁵⁻⁸,¹³⁻¹⁶ Most studies to date on La-incorporated HK dielectrics are based on conventional device-level electrical analysis.⁵⁻⁸,¹³⁻¹⁶ This approach is likely to mask out any possible local variation in electrical and physical information due to area-averaging. In this work, a detailed measurement of the nanoscale physical and electrical characteristics is undertaken. Results showed no significant difference between the macro- and nanoscale behavior of these dielectric stacks.

II. EXPERIMENTAL METHODS

Scanning tunneling microscopy (STM) and atomic force microscopy (AFM) experiments were carried out in ultrahigh vacuum (10⁻¹⁰ Torr). Platinum–iridium (Pt-Ir) and Si tips were used in STM and tapping-mode AFM experiments, respectively.

In the STM experiment, the current was measured from the tip while the bias was applied to the sample. Since vacuum has a dielectric constant of 1, a significant proportion of the applied sample bias drops across the vacuum gap,
and the voltage drop across the HK layer is typically around 50% of the applied sample bias.\textsuperscript{17,18} The HK gate dielectric topography was observed under constant-current imaging mode, where the feedback circuit maintained a constant tunneling current through the gate dielectric material by adjusting the vacuum gap between the STM tip and sample surface. Also, by acquiring current–voltage (I-V) curves while scanning the topography, a constant-current topographical image and spatially resolved I-V characteristics were simultaneously obtained. From the I-V characteristics, the tunneling current at each pixel at a defined constant voltage was mapped to form a current imaging tunneling spectroscopy (CITS) image,\textsuperscript{17,18} which profiles the spatial gate dielectric leakage current over a given area of the dielectric stack and helps in deconvoluting the electrical properties from the morphology.

In the sample preparation, first La\textsubscript{2}O\textsubscript{3} (~1 nm) and then HfO\textsubscript{2} (~4 nm) were deposited on the Si substrate using e-beam evaporation and the stack was annealed at 600 °C, resulting in La-incorporated HfO\textsubscript{2}. HfO\textsubscript{2} (~5 nm) deposited on Si substrate and annealed at 600 °C was used as a reference sample (i.e., no La was present) and compared with the characteristics of La-incorporated HfO\textsubscript{2}. For the Ce-based samples, first La\textsubscript{2}O\textsubscript{3} (~2 nm) and then CeO\textsubscript{2} (~2 nm) were deposited on a Si substrate using e-beam evaporation and annealed at 500 °C. The nanoscale characteristics of La-incorporated CeO\textsubscript{2} were compared with CeO\textsubscript{2} deposited on Si substrate annealed at 500 °C.

### III. RESULTS AND DISCUSSION

#### A. La-incorporated HfO\textsubscript{2}

Figures 1(a) and 1(b) show transmission electron microscopy (TEM) micrographs of annealed HfO\textsubscript{2} (~5 nm) and La-incorporated HfO\textsubscript{2} (~5 nm) dielectrics, respectively, on Si substrate. The TEM micrograph shows the SiO\textsubscript{x} IL layer and a polycrystalline structure in HfO\textsubscript{2}, and an amorphous-like layer with uniform crystal structure in La-incorporated HfO\textsubscript{2}. To understand the composition and mixing of the dielectric layers, energy dispersive x-ray spectroscopy (EDX) line profiles were used to create the compositional profiles of Hf, oxygen, and silicon in HfO\textsubscript{2} [Fig. 1(c)] and Hf, La, oxygen, and silicon in La-incorporated HfO\textsubscript{2} [Fig. 1(d)]. The results clearly show the diffusion of La through the dielectric stack and the presence of La elements on the Si surface. The reactivity of lanthanum with SiO\textsubscript{x} reduces the SiO\textsubscript{x} interfacial layer thickness, thus lowering device EOT.\textsuperscript{14} Hence, a thin layer of La\textsubscript{2}O\textsubscript{3} inserted at the HfO\textsubscript{2}/Si interface can form a suitable HK dielectric for advanced CMOS applications.\textsuperscript{6,14} It has been reported that the addition of La\textsubscript{2}O\textsubscript{3} into HfO\textsubscript{2} improves the “κ” value of the film because of the high dielectric polarizability of La\textsuperscript{3+} in La\textsubscript{2}O\textsubscript{3} and even a slight amount of La offers a higher dielectric constant (~28) than pure HfO\textsubscript{2} (~25).\textsuperscript{13} This gives La-incorporated HfO\textsubscript{2} an advantage over other Hf-based amorphous dielectric materials such as HfSiO\textsubscript{x} and HfAlO\textsubscript{x}.\textsuperscript{13}

![Cross-sectional TEM micrograph](image)

**Fig. 1.** (Color online) Cross-sectional TEM micrograph of (a) HfO\textsubscript{2} (~5 nm)/SiO\textsubscript{x} (~1 nm) on Si substrate, annealed at 600 °C and (b) La-incorporated HfO\textsubscript{2} (~5 nm) on Si substrate, annealed at 600 °C. EDX line profile of (c) HfO\textsubscript{2} and (d) La-incorporated HfO\textsubscript{2} on Si substrate. The results show the diffusion of La through the HfO\textsubscript{2} dielectric and negligible SiO\textsubscript{x} IL formation. Si/SiO\textsubscript{x} interface location was estimated from the dielectric thickness obtained from the TEM micrographs (a) and (b).
Figures 2(a) and 2(b) show tapping-mode AFM topographic images for the annealed HfO2 and La-incorporated HfO2 dielectrics, respectively. The root mean square (rms) roughness of the surfaces is 0.67 nm for HfO2 and 0.49 nm for La-incorporated HfO2 dielectrics. The smoother surfaces of the La-incorporated dielectrics further improve device performance by establishing a good gate-dielectric interface.

Figures 3(a) and 3(b) show the STM topographies (bias conditions, +3.5 V, 30 pA) of HfO2 and La-incorporated HfO2 dielectrics, respectively. Again, an amorphous morphology was revealed, showing a decrease in the surface feature sizes and roughness of HfO2 dielectric with La incorporation.

Figures 4(a) and 4(b) show the STM CITS maps at +4 V of HfO2 and La-incorporated HfO2, respectively. The results show that La-incorporated HfO2 exhibited a reduced number and intensity of leakage spots compared to HfO2. To quantify the data, we normalized a cumulative count of the tunneling leakage current from each pixel of the CITS current map to the total number of pixels. A narrow distribution of tunneling leakage current was observed for the La-incorporated HfO2 [Fig. 4(c)]. The distribution of the tunneling leakage current was plotted for different 50 × 50 nm² areas using a box-plot, where the tunneling current was normalized to the minimum current value, 30 pA [Fig. 4(d)]. As evident from the figure, a slight decrease in the leakage current distribution was noted, i.e., a smaller spread for La-incorporated HfO2.

In the HfO2 dielectric, the grain boundaries (GB) serve as paths of higher leakage current and produce a larger variation of local electrical leakage. In La-incorporated HfO2, the reduced leakage current is mainly attributed to the substantial increase in the crystallization temperature of the composite dielectric. The La-incorporated HfO2 dielectric appears to be amorphous and does not have a “lower-k” interfacial layer [Fig. 1(b)]. Hence, the GBs would not be expected to play an important role. In addition, Umezava et al. reported that the introduction of La also decreases the oxygen vacancies in HfO2 dielectrics. Hence, the reduced leakage current distribution (~15% at 50% on distribution scale [Fig. 4(c)]) in La-incorporated HfO2 can be attributed to an increase in crystallization temperature and decrease in oxygen vacancies.

B. La-incorporated CeO2

Figure 5(a) shows a TEM micrograph of CeO2 (~4 nm) on Si substrate exhibiting a polycrystalline structure. In
FIG. 4. (Color online) STM CITS maps (at +4 V) of (a) HfO$_2$ and (b) La-incorporated HfO$_2$ dielectric. (c) Box-plot of normalized tunneling leakage current distribution in HfO$_2$ and La-incorporated HfO$_2$ dielectric stack, as determined by the analysis of the corresponding CITS maps normalized to the minimum tunneling leakage current, 30 pA (area 1 and area 2 were obtained from HfO$_2$, and area 3 and area 4 were obtained from La-incorporated HfO$_2$).

FIG. 5. (Color online) Cross-sectional TEM micrograph of (a) CeO$_2$ (~4 nm) and (b) La-incorporated CeO$_2$ (~4 nm) on silicon substrate annealed at 500°C with tungsten (W) gate electrode. A direct HK/Si structure is confirmed in (b). (c) Normalized intensity counts by EDX of Si, oxygen, and cerium in CeO$_2$ on Si substrate. Si/SiO$_x$ interface location and SiO$_x$-Ce$_2$O$_3$ thickness were estimated from the dielectric thickness obtained from the TEM micrograph, (a). (d) Normalized intensity counts by EDX of Si, oxygen, lanthanum, and cerium in La-incorporated CeO$_2$ on Si substrate. Si and La-incorporated CeO$_2$ interface location was estimated from the dielectric thickness obtained from the TEM micrograph, (b).
contrast, the La-incorporated CeO$_2$ stack transforms into a La-incorporated CeO$_2$ directly on Si, without crystallization, as shown in the cross-sectional TEM micrograph [Fig. 5(b)]. Figure 5(c) shows the EDX line profile of Ce, oxygen, and Si in CeO$_2$ on the Si structure. It can be observed that oxygen spreads into the entire dielectric stack and at the interface of CeO$_2$ and Si. The presence of all the three elements (Ce, O, and Si) results in the formation of a thin layer of Ce-silicate (Ce$_2$O$_3$–SiO$_x$). It has been previously reported that CeO$_2$ reduces to its suboxide, Ce$_2$O$_3$, near the Si interface and a very thin layer of SiO$_x$ forms at the interface of Ce$_2$O$_3$ and the Si substrate, resulting in the Ce$_2$O$_3$–SiO$_x$ (Ce-silicate) at the interface.$^{4,22}$ Figure 5(d) shows the EDX line profiles of the elements Ce, La, oxygen, and Si in La-incorporated CeO$_2$. The interface between different layers is not abrupt [Fig. 5(d)], i.e., there is an intermixing of the dielectric layers, with La and Ce spreading throughout the dielectric stack. The presence of significant quantities of both La and Ce presumably leads to the formation of LaCe-silicate on the Si substrate.

Tapping-mode AFM topographic images of CeO$_2$ and La-incorporated CeO$_2$ are shown in Figs. 6(a) and 6(b), respectively. The surface roughness (rms) values of the images are 0.62 nm for CeO$_2$ and 0.45 nm for La-incorporated CeO$_2$. This slightly lower surface roughness for the La-incorporated CeO$_2$ dielectric, with more uniform contrast compared to the CeO$_2$ dielectric shows lesser variation in the granular structures. Figures 7(a) and 7(b) show the STM topographies (+3 V, 30 pA) of CeO$_2$ and La-incorporated CeO$_2$, respectively. Again, a more uniform, smooth surface morphology was observed for the La-incorporated CeO$_2$ dielectric. The smoother gate-dielectric interface in La-incorporated CeO$_2$ will help in improving device performance.

Figures 8(a) and 8(b) show the STM CITS maps at +3.5 V of CeO$_2$ and La-incorporated CeO$_2$, respectively. The CITS map of the La-incorporated CeO$_2$ dielectric stack shows very uniform electrical characteristics across the dielectric film with considerably reduced number and intensity of leakage sites compared to the CeO$_2$ dielectric. The higher leakage current in the CeO$_2$ dielectric is due to high leakage current at the grain boundaries.$^{23}$ Figure 8(c) shows the distribution of the CITS current (normalized to the minimum current of the current map, 30 pA) of CeO$_2$ and La-incorporated CeO$_2$ dielectrics. The current distribution of the CeO$_2$ shows a much larger spread compared to the La-incorporated CeO$_2$ dielectric, suggesting a decrease in the defect density by inserting the La$_2$O$_3$ film. The
combination of La$_2$O$_3$ and CeO$_2$ reduces the fixed charges present in La$_2$O$_3$, with CeO$_2$ acting as an oxygen reservoir. The intermixing of La and Ce atoms also suppresses the neutral oxygen vacancies (V$_{0}$) due to the strong ionic character of the La-oxygen bond.$^{24}$ The significant decrease in the leakage current distribution of Fig. 8(c) ($\sim$40%) in the La-incorporated CeO$_2$ dielectric suggests that the intermixing of La and Ce that occurs upon annealing suppresses the incidence of defects. An increase in the crystalline temperature together with defect reduction, greatly improves the electrical properties of the La-incorporated CeO$_2$ dielectric. In comparison to La-incorporated HfO$_2$, the La-incorporated CeO$_2$ shows better HK properties. This can be attributed to the fact that Ce and La have similar atomic and chemical properties,$^{25}$ thus allowing a ready intermixing of the two species in the stack.

IV. SUMMARY AND CONCLUSIONS

The effect of La incorporation on HfO$_2$ and CeO$_2$ dielectrics was studied in this work by analyzing surface morphology, crystalline structure, and local electrical homogeneity obtained by STM, AFM and TEM. An insertion of La$_2$O$_3$ at the HfO$_2$/Si interface and the CeO$_2$/Si interface resulted in the formation of ILs with “k” values higher than SiO$_2$, considerably reduced leakage current for La-incorporated CeO$_2$, and an increase in the crystalline temperature of the overall dielectric stack. These results have been shown previously$^{5-8,13-16}$ at the device level. The STM/AFM data complement these findings and demonstrate that these effects are manifested even at nanometer-length scales. In particular, we showed that STM can be used to measure local leakage sites and directly show how La incorporation affects leakage. These results are for e-beam deposited samples, and it is anticipated that similar observations would be found for atomic layer deposited films.$^{26-28}$

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