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Analysis of Correlated Gate and Drain Random Telegraph Noise in Post-Soft Breakdown TiN/HfLaO/SiO\textsubscript{x} nMOSFETs

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Abstract — We investigate correlated gate (I\textsubscript{G}) and drain (I\textsubscript{D}) random telegraph noise phenomena observed in post breakdown regime on nMOSFET TiN/HfLaO/SiO\textsubscript{x} gate stacks. We observe two different I\textsubscript{G}-I\textsubscript{D} correlation patterns (i.e. of the same and opposite polarities) that we attributed to charge trapping into oxygen vacancy traps of different kinds located in the SiO\textsubscript{x} close to the Si/SiO\textsubscript{x} interface. Results reported in this letter provide useful information for improving the understanding of I\textsubscript{G}/I\textsubscript{D} RTN phenomena and its impact on the reliability of post-SBD nanometer MOSFETs.

Index Terms — Random Telegraph Noise (RTN), gate current RTN, drain current RTN, soft breakdown (SBD).

I. INTRODUCTION

Random telegraph noise (RTN) is considered one of the most critical issues for the reliability of advanced CMOS devices and circuits [1]. Despite being a largely investigated phenomenon [2], a comprehensive understanding of RTN is still missing. One of the most interesting aspects that have still to be clarified is the correlation between gate (I\textsubscript{G}) and drain (I\textsubscript{D}) RTN signals that has been reported recently for unstressed SiON and high-\textkappa/metal gate MOSFETs [3], [4].

In this scenario, the aim of this work is to investigate the I\textsubscript{G}-I\textsubscript{D} RTN signal correlation in TiN/HfLaO/SiO\textsubscript{x} nMOSFET gate stacks. Differently from previous studies, we measure I\textsubscript{G} and I\textsubscript{D} RTN signals on devices stressed up to soft breakdown (SBD). This allows analyzing the properties of stress-generated defects and understanding the impact of I\textsubscript{G} and I\textsubscript{D} RTN on post-SBD MOSFET reliability. The results obtained in this work reveal that correlated and uncorrelated I\textsubscript{G}-I\textsubscript{D} RTN phenomena are due to traps located in proximity of the Si/SiO\textsubscript{x} interface and in the HfLaO layer, respectively.

II. DEVICES AND EXPERIMENTS

Devices studied in this work are small area high-\textkappa/metal gate nMOSFETs (channel length L=0.09-0.5\mu\text{m} and width

Fig. 1. Typical gate current characteristics measured before and after SBD (I\textsubscript{G}=10\mu\text{A}) on a TiN/HfLaO nMOSFET with W=0.15\mu\text{m} and L=0.25\mu\text{m}. There is a significant increase in I\textsubscript{G} after the SBD induced by the stress.

W=0.15-0.50\mu\text{m}) with an ultrathin gate dielectric stack of 20Å HfLaO and 6Å SiO\textsubscript{x} interfacial layer (IL). HfO\textsubscript{2} and a thin LaO capping layer were deposited by ALD, with PVD TiN as metal gate (gate first), annealed at 750°C in N\textsubscript{2} for 30min. All devices were subjected to a positive constant voltage stress until a SBD event was detected. A gate current compliance (I\textsubscript{gl}) of 1-10\mu\text{A} was used to avoid hard BD and keep the devices functional even after degradation. The measurements were performed on a Keithley 4200 semiconductor characterization system with a resolution up to the femtoampere current level. The best time resolution achieved is typically ~20ms.

III. RESULTS AND DISCUSSION

In this study we considered 27 devices, where drain and gate current noise was measured both before and after SBD. Before stress, I\textsubscript{G} RTN was observed in roughly 30% of the cases, whereas no I\textsubscript{D} RTN fluctuations were measured on any devices, confirming the low occurrence (2-3%) of this phenomenon as reported in the previous studies [3], [4]. RTN observations increase significantly after SBD due to the large
number of active defects generated in the dielectric stack during the electrical stress. Almost all devices exhibit \( I_D \) RTN fluctuations and in roughly 10% of the cases they are correlated to the \( I_D \) RTN signal. It is worth noting that \( I_D \) RTN was observed only in sub-\( V_T \) regime. This is related to the discrete nature of the channel doping in nano-scale MOSFETs that leads to the confinement of the current flow into small percolation paths associated with the position of dopants [5], [6]. In the sub-\( V_T \) regime, the local \( V_T \) increase due to the electron trapping can affect the current into the channel percolation paths, provided that the trap is located close to the silicon interface, inducing significant \( I_D \) fluctuations. On the other hand, increasing the gate voltage above-\( V_T \) forces the channel in strong inversion: the current flow becomes more uniform, and the effect of a single trap on the total reduces \( I_D \) and RTN fluctuations become much more difficult to be observed.

Figure 2 shows an example of the currents measured at gate and drain terminals simultaneously after SBD on a device biased in sub-\( V_T \) regime. Clear RTN signals are observed. The gate and drain currents exhibit RTN fluctuations of either the same (both \( I_G \) and \( I_D \) decrease, Fig. 2(a)) or of the opposite polarity (\( I_G \) decreases while \( I_D \) increases, Fig. 2(b)). In a previous study on correlated \( I_G-I_D \) noise in SiON transistors [4], RTN fluctuations of the same polarity were observed in n-type devices, while correlated RTN signals of the opposite polarity in p-type MOSFETs. The mechanism proposed in [4] to explain these two \( I_G-I_D \) RTN correlation patterns is simply related to the majority carrier charge. The trapping of electrons (holes) in nFETs (pFETs) increases \( |V_T| \) thus reducing \( I_D \), while it lowers (raises) the electric field within the oxide, thus explaining the \( I_G \) reduction (increase). In this work, \( I_G-I_D \) RTN patterns with same and opposite polarities are both observed in nMOSFETs, and therefore they cannot be attributed to the different charge carriers as in [4].

We attributed the different \( I_G-I_D \) RTN correlation patterns in Figs. 2(a) and (b) to electron trapping/emission into/from defects in the SiO\(_2\). A wide variety of defects originating from dangling bonds (Pb centers) and oxygen vacancies (the E’ centers) have been reported in the literature to explain reliability phenomena such as NBTI [7] and \( I_D \) noise. E’ centers with different charge states (e.g. neutral E’, positive E’+, negative E’- [8]) and atomic configurations are naturally “available” inside the SiO\(_2\), also because of the amorphous nature of its atomic network [8]. Such defects exhibit properties (i.e. thermal ionization and relaxation energies) depending on their atomic configuration and charge state, which can thus be altered by an electron capture or emission [9]. Oxygen vacancies at certain charge state were shown to be the defect supporting the electron Trap-Assisted Tunneling (TAT) [10] that is the dominant charge transport mechanism in dielectric stacks. The change in thermal ionization and the relaxation energies (induced by trapping/detrapping) of such defects affect the electron tunneling rates through them [9]-[10], thus inducing fluctuations in the TAT \( I_G \) current [9]. On the other hand, the charge trapping affects also the local \( V_T \), generating \( I_D \) current fluctuations.

In this scenario, we think that the variety of (also unexplored) SiO\(_2\) defect configurations allows explaining the experimental \( I_G-I_D \) trend. The simultaneous decrease of both \( I_G \) and \( I_D \), Fig. 2(a), could be attributed to the electron capture, which changes the thermal ionization and relaxation energies of defects (e.g. neutral E’ center) [9], [11]-[12], making it less effective to support TAT and thus reducing \( I_G \). The \( I_D \) reduction is simply due to the local \( V_T \) increase [4], [11]. On the contrary, \( I_G-I_D \) fluctuations of opposite polarity, Fig. 2(b), could be attributed to defects (e.g. positive E’+, centers) that becomes less effective to support TAT after an electron emission, thus explaining the simultaneous \( I_G \) increase and \( I_D \) decrease.

Interestingly, both the correlated and uncorrelated \( I_G-I_D \) fluctuations were observed during the same measurement. Figs. 3(a) and (b) show the \( I_G \) and \( I_D \) RTN signals measured concurrently on a post-3µA SBD nMOSFET at 150K in sub-\( V_T \) regime. \( I_G \) exhibits four fluctuation levels indicating the presence of two active traps, whereas only two levels (i.e. a single trap) are observed in the \( I_D \) RTN signal. The \( I_D \) RTN signal is correlated to the \( I_G \) fluctuations induced by one of the
two traps observed in the $I_D$ RTN. This concurrent presence of both correlated and uncorrelated traps is due to the position of the trap with respect to the paths in which the channel current is confined [5]. The trap inducing $I_D$ RTN fluctuations generates correlated $I_D$ RTN only if it is located close to one of the channel current percolation paths [5]. Therefore, traps that are either laterally misaligned with respect to the $I_D$ percolation path or located far from the Si/SiO$_x$ interface will not contribute to $I_D$ fluctuations. This is also the reason why the $I_D$ RTN occurrence is significantly lower than $I_G$ RTN.

We estimated the vertical position of the traps inside the stack from the dependence of capture ($\tau_c$) and emission ($\tau_e$) times on the gate voltage using the method proposed in [13], which was adapted to the two-layer HfLaO/SiO$_x$ dielectric stack considered in this work. Note that, according to our interpretation, $\tau_c$ corresponds to the upper (lower) $I_G$ state in the case of $I_G$-$I_D$ correlated signals of the same (opposite) polarity, as depicted in Figs.2(a) and(b). Starting from the simplified expressions of $\tau_c$ and $\tau_e$ proposed in [15] we calculated the derivative of $\ln(\tau_c/\tau_e)$ with respect to $V_G$ as

$$\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_G} = x_T(\alpha + \beta x_T V_G),$$

where $\alpha$ and $\beta$ (their expressions are omitted for brevity) depend on trap (thermal ionization and relaxation energies [14]) and dielectric (dielectric constant, conduction band offset, effective oxide thickness of the stack, etc.) properties. $x_T$ is the trap distance from the bottom interface of the layer. Fig. 4(a) shows the $\ln(\tau_c/\tau_e)$ vs. $V_G$ for both correlated and uncorrelated traps. Even though an accurate extraction of defect positions would probably require more data, the limited data set in Fig. 4(a), which results from the very small $V_G$ range allowing a clear RTN observation, is adequate for an approximated evaluation. The two opposite $\ln(\tau_c/\tau_e)$ vs. $V_G$ trends observed for correlated (both polarities) and uncorrelated traps are due to the different positions of the defects [13]. The trap position $x_T$ calculated from the measurements using (1) show that traps responsible for the correlated $I_G$-$I_D$ fluctuations of the opposite (Fig.3) and same (Fig.2(a)) polarities are located in the SiO$_x$ IL respectively at $\sim 3\pm 0.5\AA$ and $\sim 4.5\pm 0.5\AA$ from the Si/SiO$_x$ interface, as schematically represented in Fig. 4(b). Conversely, the trap generating uncorrelated $I_G$-$I_D$ fluctuations in Fig. 3 is located in the HfLaO layer at $\sim 22\AA$ from the Si/SiO$_x$ interface, i.e. $14\AA$ inside the HfLaO layer as schematically represented by the red circle in Fig. 4(b).

IV. CONCLUSION

We investigated correlated $I_G$-$I_D$ RTN signals in post-SBD metal gate HfLaO/SiO$_x$ nMOSFETs. The $I_G$-$I_D$ RTN correlation is attributed to the electron trapping into defects in the proximity of the silicon interface. Two different $I_G$-$I_D$ correlated patterns (of same and opposite polarities) were identified, which are attributed to defects of different nature supporting the TAT charge transport. These results allow both understanding the impact of $I_G$-$I_D$ RTN signals on the post-SBD MOSFET reliability and optimizing the dielectric stack in order to mitigate the post-SBD RTN phenomena.

REFERENCES