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Influence of post-deposition annealing on interfacial properties between GaN and ZrO2 grown by atomic layer deposition

Gang Ye, Hong Wang, Serene Lay Geok Ng, Rong Ji, Subramaniam Arulkumaran, Geok Ing Ng, Yang Li, Zhi Hong Liu, and Kian Siong Ang

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Influence of post-deposition annealing on interfacial properties between GaN and ZrO$_2$ grown by atomic layer deposition

GangYe,$^1$ HongWang,$^{1,a}$ Serene LayGeokNg,$^2$ RongJi,$^2$ SubramaniamAruulkumaran,$^1$

GeokIngNg,$^1$ YangLi,$^1$ ZhiHongLiu,$^3$ and KianSiongAng$^1$

$^1$Novitas, Nanoelectronics Center of Excellence, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore
$^2$Data Storage Institute, Agency for Science Technology and Research (A-STAR), 5 Engineering Drive 1, 117608, Singapore
$^3$Singapore-MIT Alliance for Research and Technology, 1 CREATE Way, Singapore 138602, Singapore

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Influence of post-deposition annealing on interfacial properties related to the formation/annihilation of interfacial GaO$_x$ layer of ZrO$_2$ grown by atomic layer deposition (ALD) on GaN is studied. ZrO$_2$ films were annealed in N$_2$ atmospheres in temperature range of 300 $^\circ$C to 700 $^\circ$C and analyzed by X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy. It has been found that Ga-O bond to Ga-N bond area ratio decreases in the samples annealed at temperatures lower than 500 $^\circ$C, which could be attributed to the thinning of GaO$_x$ layer associated with low surface defect states due to “clean up” effect of ALD-ZrO$_2$ on GaN. However, further increase in annealing temperature results in deterioration of interface quality, which is evidenced by increase in Ga-O bond to Ga-N bond area ratio and the reduction of Ga-N binding energy.

ZrO$_2$ dielectric layers were deposited on GaN-on-sapphire substrates by using ALD method. The un-doped GaN-on-sapphire wafers were grown by Metal Organic Chemical Vapor Deposition (MOCVD) using a commercial reactor. For the investigation of ZrO$_2$/GaN interface, samples with 2 nm thick ZrO$_2$ on GaN surface were utilized for XPS measurements while ZrO$_2$ dielectric layers with a thickness of 10 nm were deposited for HR-TEM characterization. To deposit the ZrO$_2$ on GaN, the GaN-on-sapphire wafers were initially degreased for 10 min in acetone and subsequently in isopropyl alcohol (IPA). Before loaded into the ALD chamber, samples were treated by buffered oxide etchant (BOE) solution to remove surface native oxide and then followed by a rinse in flowing de-ionized (DI) water. ZrO$_2$ dielectric layers were deposited by a Cambridge Nanotech Savannah ALD system. The tetrakis-(diethylamino)-zirconium and $\text{H}_2\text{O}$ pulse of H$_2$O and Zr sources were introduced into the chamber by a rinse in flowing de-ionized (DI) water. ZrO$_2$ dielectric layers were deposited by a Cambridge Nanotech Savannah ALD system. The tetrakis-(diethylamino)-zirconium and H$_2$O were used as the precursors. Chamber pressure and substrate temperature were set at 0.6 Torr and 250 $^\circ$C, respectively. During the deposition, sequential 400 ms and 40 ms pulse of H$_2$O and Zr sources were introduced into the chamber separately. After each pulse of precursor, the chamber was purged with N$_2$ for 6 s to remove excess precursors and by-product gases. High purity N$_2$ was used as the precursor carrier and purging gas. The growth rate for ZrO$_2$ was ~0.09 nm per ALD cycle. After dielectric layer deposition, different post-deposition anneals (PDAs) using rapid thermal annealing (RTA) in N$_2$ atmospheres for 30 s were performed under five different temperatures (300 $^\circ$C, 400 $^\circ$C, 500 $^\circ$C, 600 $^\circ$C, and 700 $^\circ$C). The XPS measurements were carried out by using X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HR-TEM).

GaN-based heterostructure devices such as high electron mobility transistors (HEMTs) have been used extensively for high frequency,$^1$ high power,$^2$ and low noise applications.$^3$ However, a layer of gallium sub-oxide (GaO$_x$) layer can be formed on GaN surface by reaction with oxygen even at room temperature.$^4$ Surface-related defect states associated with the GaO$_x$ layer result in large current leakage$^5$ and severe current collapse at high frequency,$^6$ which may inhibit the formation of interfacial high-k dielectric layer and semiconductor substrate for semiconductor devices. On the other hand, from device fabrication point of view, post-deposition annealing (PDA) could serve as an effective way to improve interfacial properties between high-k dielectric layer and semiconductor substrate for semiconductor devices.$^7,8$ By virtue of its high dielectric constant along with reasonably high conductance and band offset (CBO) and valance band offset (VBO) aligned to GaN substrate, ZrO$_2$ is a promising dielectric material candidate for GaN MISHEMTs.$^9$ Excellent electrical characteristics of GaN MISHEMTs utilizing ZrO$_2$ as gate dielectrics are reported recently.$^{10-15}$ Nevertheless, several material issues should be considered for further improvement of the electrical properties for GaN MISHEMTs using ZrO$_2$ as gate insulators. Above all, the interface between dielectric layer and underlying GaN substrate is critical, and thermal stability of the dielectric layer at the interface is one of the most challenging requirements for application of ZrO$_2$ as a gate dielectric. However, so far, few studies have been carried out on the ZrO$_2$ dielectric layers on GaN, especially in regard with the interfacial properties between ZrO$_2$ and GaN. On the other hand, from device fabrication point of view, post-deposition annealing (PDA) could serve as an effective way to improve interfacial properties between high-k dielectric layer and semiconductor substrate for semiconductor devices.$^4$

$^a$Electronic mail: ewanghong@ntu.edu.sg
out using a monochromatic Al K\textsubscript{α} X-ray source of energy 1486.7 eV. The spectra are curve-fitted with a combination of Gaussian and Lorentzian line shapes using a Shirley-type background subtraction. All peaks were referenced to the C 1s peak at 284.6 eV to compensate for any variations in the peak core-level positions due to binding energy (BE) shift caused by surface charging. The schematic structure of the sample used for investigating the ZrO\textsubscript{2}/GaN interface by XPS measurements is shown in Fig. 1, where the photoelectron take-off angle is defined as $\theta$. Here, the take-off angle $\theta$ was set at 15°, which enabled sensitivity analysis of chemical states at interface between ZrO\textsubscript{2} layer and GaN substrate.\textsuperscript{9}

Ga 3d core-level XPS spectra obtained under different post-deposition annealing temperatures are depicted in Fig. 2. It can be seen from Fig. 2 that each Ga 3d spectrum could be deconvoluted into two components, corresponding to the Ga-N and Ga-O bonds. The existence of the Ga-O spectrum for the as-deposited sample (indicated by N.A in Fig. 2) may be attributed to the parasitic oxidation of the GaN surface after cleaning during ALD deposition process.\textsuperscript{16,17} Apparently, the Ga-N bonds show an obvious increase in binding energies (BEs) with the increase of annealing temperatures when the annealing temperatures are lower than 500 °C. Further increase in annealing temperature shows a reduction of the BEs. As a polar semiconductor, GaN surface is sensitive to fabrication process. Sharp upward band bending at GaN surface due to large polarization combined with possible surface Fermi-level pinning caused by surface defects and contaminations may occur.\textsuperscript{18,19} In our previous report for ALD ZrO\textsubscript{2} on GaN, such strong upward band bending was observed through XPS measurements.\textsuperscript{9} Meanwhile, as can be obtained from Fig. 2, the integrated XPS intensity of Ga-O bond to Ga-N bond ratio also shows variations related to annealing temperatures. For clarity, the dependence of Ga-N bond binding energies and ratio of the Ga-O to Ga-N XPS peak area on annealing temperatures are plotted in Fig. 3. It can be seen that the Ga-N bond binding energies are strongly coincident with the ratio of Ga-O to Ga-N peak area. In general, the decrease in the ratio of Ga-O to Ga-N peak area leads to the increase of Ga-N bond binding energy. This suggests that the Fermi-level position at GaN surface is affected by surface-related defect states associated with GaO\textsubscript{x} layer. The surface states contribute to upward band bending at GaN surface. A higher defect density at ZrO\textsubscript{2}/GaN interface could cause stronger upward band bending thus lower Ga-N bond binding energy. The annihilation or formation of the gallium sub-oxide layer at the interface is highly related to annealing temperatures. Under annealing temperature of 500 °C, the Ga-N bond binding energy shows the highest value along with the smallest Ga-O to Ga-N peak area ratio. The decrease in Ga-O bond concentration may suggest a “clean up” effect, which is most likely due to the formation of a Ga-O-Zr environment to passivate Ga-O bond. Such clean up effect is widely reported on ALD deposited high-k dielectrics on III-V semiconductor interfaces such as Al\textsubscript{2}O\textsubscript{3}/Al\textsubscript{2}O\textsubscript{3}/III-N.\textsuperscript{22,23}

HR-TEM is used to further characterize the interfacial properties between ALD ZrO\textsubscript{2} and GaN. Cross sectional TEM micrograph for as-deposited sample (N.A) and samples annealed at 500 °C and 700 °C are shown in Fig. 4. Obviously, compared with the as-deposited sample, ZrO\textsubscript{2} thin films get further crystallized with the increasing of the annealing temperatures, which is consistent with the report in literature.\textsuperscript{24} For the as-deposited film shown in Fig. 4(a),

![FIG. 1. A schematic cross-sectional diagram for GaN with 2 nm ALD-ZrO\textsubscript{2} dielectric layer for XPS measurements. The definition of take-off angle $\theta$ is also shown.](image1)

![FIG. 2. The measured (open circles) and fitted (lines) XPS Ga 3d core-level spectra for ALD ZrO\textsubscript{2} on GaN samples measured at take-off angle $\theta$ of 15° under different PDA temperatures. The as-deposited sample is indicated as N.A.](image2)

![FIG. 3. Change of Ga-N bond BE and integrated XPS intensity ratio of Ga-O bond to Ga-N bond for ZrO\textsubscript{2}/GaN samples under different PDA temperatures. The as-deposited sample is indicated as N.A, and the dashed lines are a guide for the eye to show the change trend.](image3)
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