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# TSV-less 3D stacking of MEMS and CMOS via low temperature Al-Au direct bonding with simultaneous formation of hermetic seal

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## Abstract

3D integration has been widely recognized as the next generation of technology for integrated microsystems with small form factor, high bandwidth, low power consumption, and possibility of heterogeneous More-than-Moore integration. Heterogeneous integration of MEMS and CMOS is critical in future development of multi-sensor data fusion in a low-cost chip size system. MEMS/CMOS integration was primarily done using monolithic and hybrid/package approaches until recently. In this work, 3D CMOS-on-MEMS stacking without TSV using direct (i.e. solder-less) metal bonding is demonstrated. This MEMS/CMOS integration leads to a simultaneous formation of electrical, mechanical, and hermetic bonds, eliminates chip-to-chip wire-bonding, and hence presents competitive advantages over hybrid or monolithic solutions. We present the fabrication flow and verify the performance of the stacked MEMS/CMOS microsystem in this paper.

The micro-electro-mechanical system (MEMS) accelerometer is fabricated using bulk micromachining technology with silicon-on-insulator (SOI) substrate. The CMOS readout circuit for the capacitive MEMS accelerometer, implemented in 0.35μm (2P4M) process, consists of three essential circuit blocks: (i) low noise, band-pass gain stage, (ii) synchronous demodulator and (iii) off-chip, low-pass filter. The MEMS chip is metallized with a single layer of Au for electrical contact and sealing ring prior to bulk etching and release. Au is chosen to withstand harsh process conditions. The CMOS chip contains four Al metal layers. The top most layer is patterned for electrical contact and sealing ring that match those of the MEMS chip. In order to ensure proper operation, the delicate micro-structures (MEMS) should be protected from the ambient. In this approach, a hermetic seal ring is formed simultaneously during face-to-face stacking of CMOS on MEMS and hence eliminating the need for post-processing hermetic encapsulation. Face-to-face stacking also eliminates the need for chip-to-chip wire bonding. Effectively, the CMOS layer acts as an "active cap". In addition, I/Os to the MEMS chip are routed through the CMOS metal layers to simplify the MEMS process. Since the I/O count is low, TSV is not used and electrical feed-through is achieved by peripheral pads. As no solder is applied, the top passivation layer of the CMOS chip is partially recessed to expose the CMOS metal layer for ease of direct bonding with the MEMS metal layer. The metal surfaces are carefully treated and bonded. The bonded samples are packaged inside 44-pin J-leaded ceramic package for testing.

The functionality of the readout circuit is verified first, using off-chip MEMS, followed by verification of the bonded CMOS/MEMS chip. In both cases, the MEMS is excited by anti-phase sinusoid carriers within the frequency range 50kHz-1MHz. The variation in the peak-to-peak amplitude of the gain stage output is observed as the MEMS is flipped between -1g/+1g orientations. In addition, the phase of the output signal agrees with the flip direction.

Testing for hermeticity of the Al-Au thermo-compression bond is done in accordance with the MIL-STD-883E standard. Passive sealed cavities with volume of about $1.4 \times 10^{-3}$ $cm^3$ are fabricated and bonded at 300 °C under a bonding pressure of around 8.4MPa for 10 mins. The cavity chips are created by deep reactive ion etching (DRIE) on silicon followed by the deposition of 50 nm of Cr adhesion layer and 150 nm of Au with electron beam evaporation method. The blanket capping chips are deposited with 100 nm of $SiO_2$ by plasma-enhanced chemical vapor deposition (PECVD) and 150 nm of Al by sputtering. Bubble test is used for gross leak and helium test is used for fine leak inspection. For shear strength measurement, test samples are prepared using the same processes for the samples in hermetic test, without the creation of cavities. The bonding parameters are kept the same. Results from the hermeticty and shear tests are presented and discussed.

## Introduction and Motivations

Advancements in packaging co-design, low-cost materials and reliable interconnect technologies are critical in enabling the innovative packaging solutions required to help drive the electronic industry forward. Packaging semiconductor devices is becoming a challenge for the industry. As process technologies become smaller as a result of rigorous Moore's Law scaling, the performance and power limitations in interconnects and packaging became prominent. The traditional interconnect and packaging solutions starts to slow down signal transmission and consumers substantial amount of power. 3D packaging has been identified as a technology platform to ensure continuous performance enhancement ("More Moore") and functional diversification ("More than Moore") in future integrated systems.

3D integration for heterogeneous More-than-Moore integration of MEMS and CMOS provides competitive advantages over hybrid or monolithic solutions. In this work, 3D CMOS-on-MEMS stacking without TSV using direct (i.e. solder-less) metal bonding is demonstrated. This MEMS/CMOS integration leads to a simultaneous formation of electrical, mechanical, and hermetic bonds, eliminates chip-to-chip wire-bonding. The CMOS die also serves as a capping medium to isolate the MEMS from the ambient removing the need of hermetic packaging, thus reducing the thickness of the overall package. Both the MEMS and CMOS dies are fabricated with standard industry processes. SOI MEMS will be used in this work and will be tested after the integration

with the CMOS die to ensure that the thermo-compression bonding does not damage the device. We present the fabrication flow and verify the performance of the stacked MEMS/CMOS microsystem in this paper.

Low-temperature (300 degrees Celsius) Cu-Cu thermo-compression bonding has been demonstrated in previous study to obtain hermetic packaging of 3D microsystems in accordance with the MIL-STD-883E standard [1]. 3D integration of MEMS and CMOS via low-temperature (300 degrees Celsius) Cu-Cu thermo-compression bonding has also been proposed [2]. However it is difficult to produce SOI MEMS dies with Cu pads as the insulator release process will also strip away common Cu barrier materials.

In this paper, Al-Au thermo-compression bonding will be used to simultaneously form of hermetic seal and connections as shown in Figure 1. Au is chosen as it is a common pad material for MEMS dies and Al-Au bonding is commonly found in wire-bonding. In this paper, Al-Au thermo-compression bonding will be evaluated according to MIL-STD 883 for shear strength [3] and leak test [4]. SOI MEMS are created with the sealing ring for direct bonding with the CMOS sealing ring. The integrated 3D system is evaluated for its functionality and reliability.

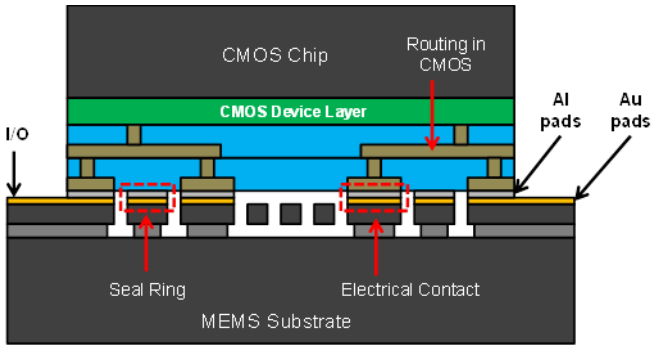



**Fig. 1** 3D stacking of MEMS and CMOS

## Al-Au Thermo-compression Shear Strength Experiment

Au-Al die level thermo compression bonding are produced and tested for die shear strength. Silicon wafers (600µm thick) are used in the thermo-compression bonding experiment. The wafer is deposited with 50 nm of Cr followed by 150 nm of Au. The Cr is deposited to ameliorate the adhesion between Au and Si. Dicing of the wafer is done to produce 5 mm × 5 mm size dies. A second blank wafer is PECVD deposited with 500 nm of $SiO_2$ and sputtered with a layer of Al of 150 nm thickness. This wafer is diced into 10 mm × 10 mm dies.

The 5mm × 5 mm die with Au and 10mm × 10 mm die with Al are placed with the metal layers facing each other. They are bonded with a die bonder with an applied force of 210 N at different bonding temperature for 10 minutes. Subsequently, the dies are annealed at the same temperature as the respective bonding temperature. The bonding temperatures and annealing temperature used are 350, 300, 290 and 280 °C, respectively. The dies are shear strength tested and the results are shown in Figure 2. The points in Figure 2 are the mean values (sample size of 5) of the shear strength at the corresponding bonding temperature while the standard deviations are depicted in the bars. The requirement of shear strength indicated in MILSTD-883E standard is 5 kg of force.

From Figure 2, it is shown that with a bonding temperature at 290 °C and above, the produced bonding strength is acceptable. When the samples are bonded with 280 °C bonding temperature, the average shear strength of the dies is below 5 kgf. Figure 3 shows the C-SAM image of the samples bonded at 290 °C. The C-SAM shows that good bonded areas are presented in only half of the dies. This non-uniformity of bonding is due to the non-uniform application of force from the die bonder.

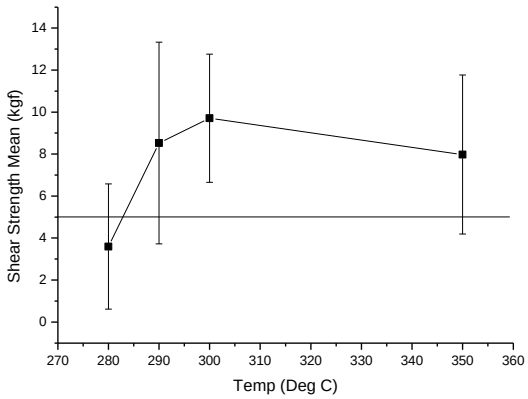



**Fig. 2** Shear strength test results with varying bonding temperature

## Al-Au Thermo-compression Hermeticity Experiment

Au-Al die level thermo-compression bonding are produced and tested for hermeticity. Silicon wafers are used in the thermo-compression bonding experiment. Deep reactive-ion etching (DRIE) is used to form the cavities and the seal rings to a depth of 120 $\mu$m using photo-resist as an etching mask (Figure 4). All cavities are designed and etched to a volume of $1.4\times10^{-3}$ $cm^3$. The surrounding air channel is formed to separate the sealed cavities from the dummy area and to provide a path for helium gas flow during bombing and leak test. After DRIE, the patterned wafer is deposited with 50 nm of Cr and 150 nm of Au. Dicing of the wafer is done to produce 10 mm × 10 mm sized dies with the cavity in the center.

**Fig. 3** Shear strength test results with varying bonding temperature C-SAM image of samples bonded at 290°C

A blank wafer is PECVD deposited with 500 nm of $SiO_2$ and sputtered to form Al layer of 150 nm. This wafer is diced into 15 mm × 15mm dies. The 10 × 10 mm die with Au and 15 × 15 mm die with Al are placed with the metal layer

facing each other. The samples are bonded using a bonding force of 2100N and bonding temperature of 300 degree Celsius. The samples are held under 2100N and bonding temperature for 10 minutes and annealed at 300$^{o}$C for 1 hour in wafer bonder. The schematic of the formation of sample dies for hermetic testing is shown in Figure 5.

After the dies are bonded, they are tested for hermeticity according to MILSTD-883E standard. Helium leak test have been performed on the bonded dies. The bonded samples are placed in a chamber filled with helium gas at a pressure of 75 Psia (~0.52 MPa) for an exposure time over 2 hr (helium bombing). Then the samples are tested for helium leak using a mass spectrometer within 1 hr. The leak rates for the samples are less than the rejection limit ($5 \times 10^{-8}$ atm-cc/s) stated in the MILSTD-883E standard with a mean leak rate of $2.7 \times 10^{-8}$ atm-cc/s.

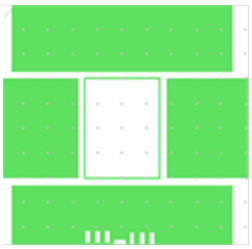


**Fig. 4** Seal cavity mask pattern for DRIE for hermetic test dies

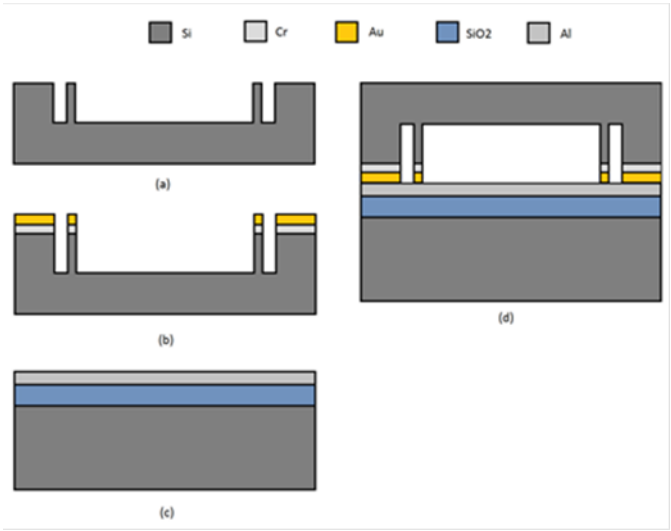



**Fig. 5** Schematics of the formation of sealed cavity for helium leak rate detection: (a) forming of cavities, seal rings and air channel using DRIE etching; (b) sequential deposition of Cr layer and Au bonding layer; (c) deposition of SiO2 isolation and Al bonding layer; (d) Au-Al thermo-compression bonding of the cavity wafer to the capping wafer.

Subsequently, perfluorocarbon gross leak test is performed by submerging the dies in fluorocarbon FC-72 ($C_6F_{14}$) in a pressurized chamber of 75 Psia for 3 hours. The dies are taken out and allowed to dry for 2 minutes. The dried dies are place in a beaker of fluorocarbon FC-43 ($C_{12}F_{27}N$) at 125 degrees Celsius. If a stream of small bubbles (shown in Figure 6) or a single big bubble is observed, the sample would have failed the gross leak test. The samples have to pass both the helium fine leak test and the gross leak test. Only the samples that passed the gross leak test are considered in the mean fine leak rate calculated in the previous paragraph. Figure 7 shows the C-SAM image of a few samples and the sealing rings are visible and continuous.


**Fig. 6** Example of a stream of bubbles observed in gross leak test

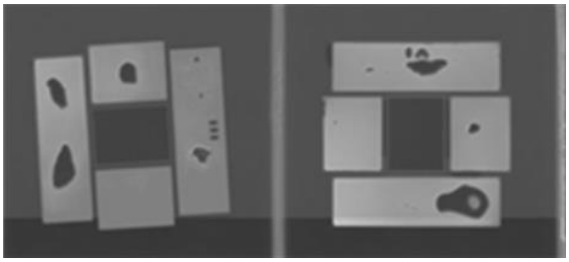


**Fig. 7** C-SAM image of hermetic test dies

**TEM and EDX Observation of Al-Au Interface**

A different sample with dies specification similar to shear strength tested dies is bonded using a bonding force of 1200N and bonding temperature of 300 degree Celsius. The samples are held under 1200N and bonding temperature for 10 minutes and annealed at 300 degree Celsius for 1 hour in wafer bonder. This sample is inspected with TEM and EDX. Figure 8 shows the location of observation marked by the dotted line.

Figure 9 shows the TEM image of the Al-Au interface of the sample at the observation location. There is no distinct interface observable. EDX line scan is performed in the location shown in Figure 10a and the result of the line scan is shown in Figure 10b. It is observed that Al and Au are evenly distributed throughout the original Au and Al layer. This shows that all the original Al and Au layers have mixed and formed intermetallic.

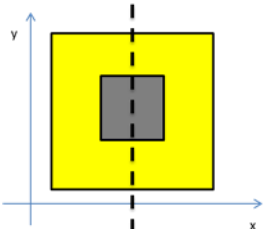
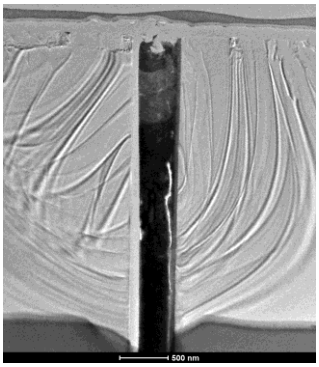



**Fig. 8** Location of TEM and EDX observation on the sample

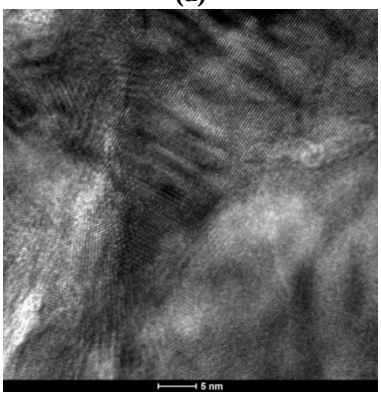
**CMOS Readout Circuit**

The circuit for MEMS readout comprises of a low noise, band-pass gain stage, a fully differential synchronous

demodulator and an off-chip, low-pass filter. The block diagram for the readout circuit is shown in Figure 11.

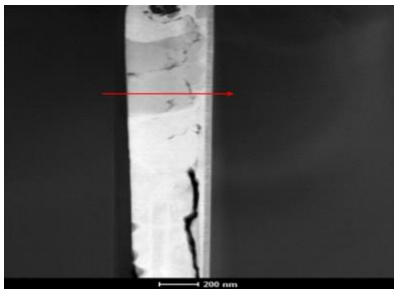



**(a)**

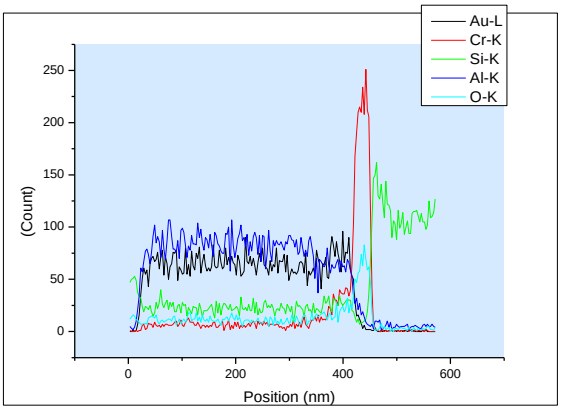



**(b)**

**Fig. 9** TEM image of a sample with increasing magnifications from (a) to (b)




**(a)**




**(b)**

**Fig. 10** EDX line scan location (a) and line scan results (b)

The low noise, band-pass gain stage is realized by using two identical single-ended output amplifiers, as shown in Figure 12. These single-ended output amplifiers are based on folded-cascode topology, which offers the advantages of a much improved common-mode input range and an increased output swing. This allows more flexibility in selecting the gain factor and which can be conveniently set externally via tunable feedback capacitance $C_f$. The flexibility in selecting the gain factor enables the same readout circuit design to work well with a wider range of accelerometer designs, in terms of output capacitance and sensitivity. It is also desirable to have very large feedback resistance $R_f$ since the lower corner of the band-pass gain stage is determined by $1/2\pi R_f C_f$. Using a very large feedback resistor however means an inefficient utilization of on-chip space. This can be taken care of by using pseudo-resistors in place of real resistors which can provide very high feedback resistance, of the order of MΩ, while consuming minimal space. The unity gain bandwidth of the folded-cascode single-ended output amplifiers decides the upper corner frequency of the band-pass gain stage. The lower and the upper corner frequency limits of the gain stage thus determine the working carrier frequency range, which are 10 kHz and 18 MHz respectively for the reported readout design. The first amplifier of the gain stage boosts up the MEMS sensor's input while the second amplifier works as an inverting stage to generate a second differential input for the synchronous demodulator.

A fully differential synchronous demodulator is the second building block of the readout circuit. Demodulation is done through envelope detection, by implementing a four-switch full-wave rectifier. The demodulator helps in easing the filtering requirements and reduces the second order harmonic distortion at the same time. The fully differential synchronous demodulator makes it possible to move the low-pass filter off-chip and which greatly helps in saving on-chip space. Moreover, as a result of ease in filtering requirements, there is no longer any need of using an active filter and this minimizes the overall circuit's power consumption. The implemented filter is a passive, second order low-pass filter with a cut off frequency of 200 Hz. The die diagram is shown in Figure 13.

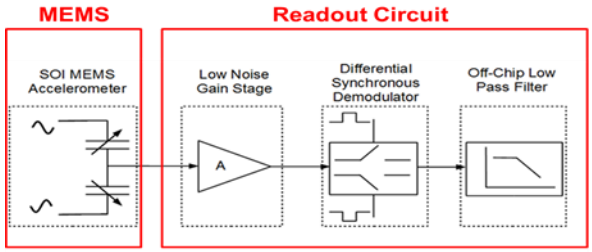



**Fig. 11** System block diagram for the readout circuit. The gain factor 'A' is determined by Cf. Implementing the low-pass filter off-chip saves on-chip space

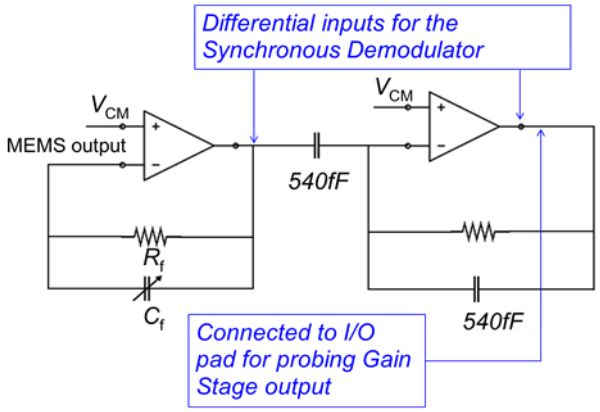



**Fig. 12** Schematic diagram of the low noise, band-pass gain stage which consists of two single-ended output amplifiers based on folded-cascode architecture. Pseudo-resistors are used in the feedback path of the amplifiers. Tunable feedback capacitance allows variable gain.

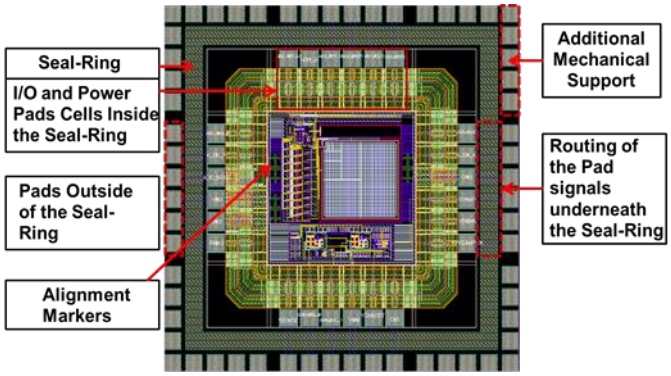



**Fig. 13** Die Micrograph of the readout circuit fabricated through MPW (0.35µm, 2P4M process). Key components are highlighted and specific ones are seal ring, mechanical support and alignment marks to assist the MEMS-CMOS bonding.

**Standalone Validation of the Readout Circuit – Results and Discussion**

The working of the readout circuit was verified with a commercial MEMS accelerometer chip. The accelerometer is driven by differential sinusoid excitation carriers and its corresponding output, based on change in differential capacitance, drives the CMOS readout.

The results shown in Figure 14 below are obtained when the MEMS chip is excited by anti-phase but unequal amplitude excitation carriers, 5Vpp and 7.5Vpp, at 50 kHz carrier frequency and 0g acceleration.

Using sinusoid carriers gives a sinusoid gain stage output. The peak-to-peak amplitude of this output is dependent on:

- The amplitude of the excitation carriers. Large amplitude carriers result in a large amplitude gain stage output.
- The frequency of the excitation carriers. Attenuation at carrier frequencies near the corners or outside the flat-band region of the band-pass gain stage significantly diminishes the output.
- The gain factor of the gain stage. Using smaller feedback capacitance $C_f$ gives a larger gain factor.
- The tilt angle of the accelerometer axis with respect to the horizontal. Larger tilt results in larger change in capacitance and hence an enhanced input to the gain stage.

Differential sinusoid inputs to the synchronous demodulator from the gain stage along with an externally supplied CLOCK input generates fully-rectified sinusoids at its outputs.

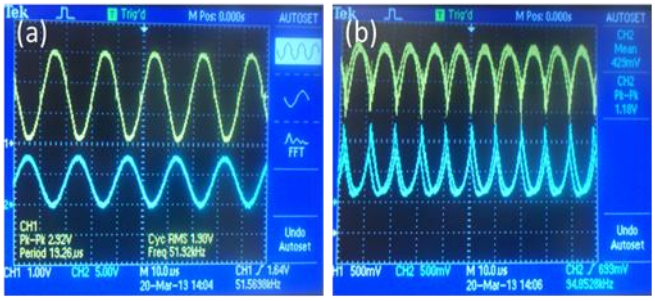



**Fig. 14** (a) The band-pass gain stage output (yellow, upper trace) during the standalone testing of the CMOS readout, when one of the carrier amplitude is 7.5Vpp (blue, lower trace) at 50 kHz frequency and 0g acceleration. (b) Fully-rectified sinusoids at the synchronous demodulator outputs, verifying that the readout is working as intended.

**Vertically Stacked CMOS-on-MEMS Chip - Packaging**

A standard CMOS chip has a passivation layer that is typically over 2µm thick, which can pose problems with thick metal deposition on the MEMS side. The CMOS dies are post-processed, in that the passivation layer is etched in depth controlled manner so that the metal on the MEMS can be easily reached.

The stacking process is illustrated in Figure 15. Alignment marks on the dies aid in orienting the dies properly before stacking. This TSV-less approach of stacking CMOS on top of MEMS results in a simultaneous formation of the hermetic seal-ring and thereby eliminates any need for post-stacking hermetic encapsulation.

The bonded MEMS/CMOS dies are then packed inside 44 pin J-leaded surface mount ceramic chip packages for verifying the functionality of the bonded chips as shown in Figure 16.

**Vertically Stacked CMOS-on-MEMS Chip – Functionality Testing**

The functionality of the bonded MEMS/CMOS microsystem (Figure 17) is verified by conducting the -1g/+1g flip test. The results presented in Figure 18 are obtained using fully-differential sinusoid carriers of 1Vpp amplitude and 50 kHz frequency. The peak-to-peak amplitude of the band-pass gain stage output shows variation that is proportional to the sine of the tilt angle between the accelerometer axis and the horizontal. Using a single-axis accelerometer restricts the total

rotation to 180° (tilt angles between -90° to +90°) that corresponds to an acceleration range of -1g to +1g.

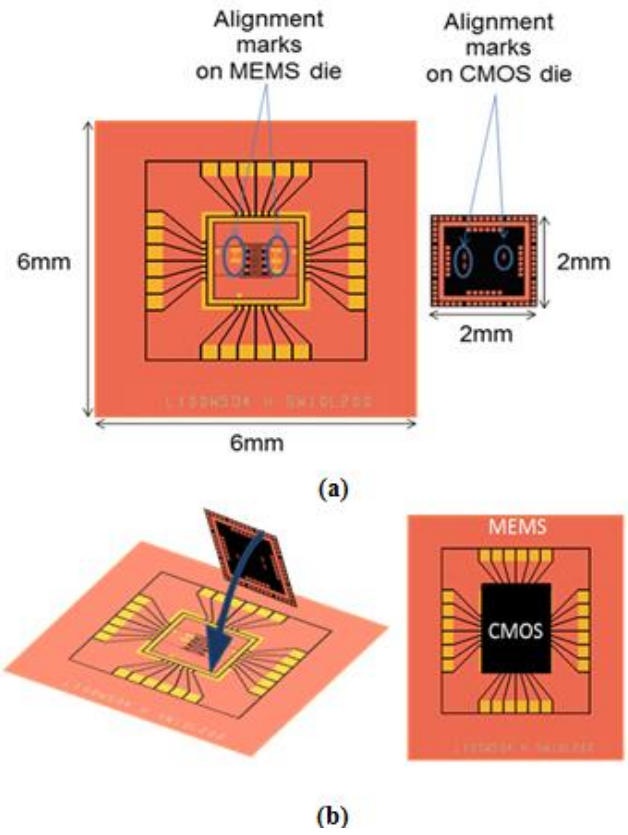



**Fig. 15** (a) The alignment marks on MEMS and CMOS die are used for orienting the dies before stacking. (b) The CMOS die is vertically stacked on top of MEMS die

The minimum amplitude case in Figure 18(a) is when the chip is at 0g orientation. The peak-to-peak amplitude of the gain stage grows out-of-phase and in-phase with respect to carrier in –g and +g flip directions respectively. The mean of the positive rectified sinusoid at the demodulator output is plotted against g at various carrier frequencies in Figure 19. The maximum peak-to-peak amplitudes observed in the two flip directions are roughly equal, thereby implying an approximately symmetrical behavior of the accelerometer.

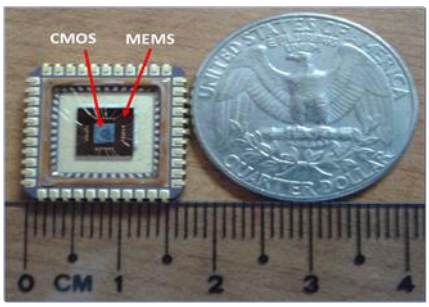



**Fig. 16** The CMOS chip is bonded face-to-face on the MEMS chip. The bonded chip is then wire bonded to the package for electrical testing. The vertically stacked CMOS and MEMS chip has a thickness of 1155µm.

Noise performance of the bonded MEMS/CMOS microsystem was assessed using spectrum analyzer. The analyzer output at 50 kHz carrier frequency and +1g acceleration is shown in Figure 20, when carrier amplitude is 1Vpp. Likewise, the FFT spectrum at other carrier frequencies and flip orientations was used for computing the signal-to-noise ratio (SNR) and output voltage noise. Reduction in SNR at increasing carrier frequencies is due to an increase in the noise floor level and a simultaneous gradual reduction in the gain stage output at higher frequencies (refer to Figures 21 and 22). Other specifications are listed in Table I.

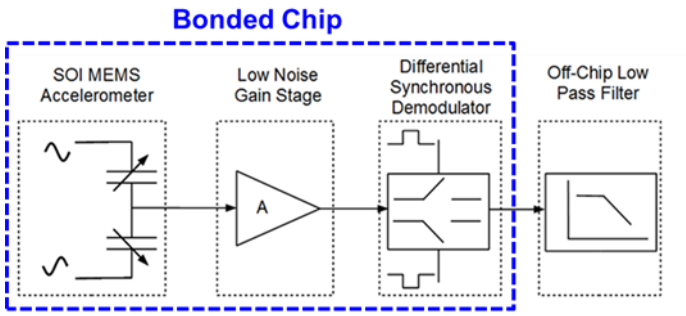



**Fig. 17** System block diagram for the bonded MEMS/CMOS microsystem. The MEMS and CMOS have been seamlessly integrated to form a single bonded chip. There is no wire-bonding from chip to chip. Chip to chip electrical connections are done using direct metal bonding without solder.

**Table I** Summary of the specifications of the vertically bonded MEMS/CMOS chip.

| **Parameters** | **Measured Values** |
|---|---|
| Supply Voltage | 3.3 V |
| Power Consumption | 1.491 mW |
| Input Referred Noise of the readout circuit | 32.663 nV/$\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion | 0.380% at 50 kHz carrier frequency and +1g acceleration |
| Minimum Detection Signal | ± 0.139g |
| Resonant Frequency | 136 kHz |
| Technology | SOI bulk-micromachining for MEMS and AMS 0.35µm (2P4M) for the CMOS readout |

**Vertically Stacked CMOS-on-MEMS Chip – Reliability Testing**

The bonded MEMS/CMOS chip was subjected to 500g mechanical shock test for testing the reliability of the metal-metal contact at the MEMS-CMOS interface. The setup for this test is shown in Figure 23. Under this setup, the bonded chip experiences 10 repetitive vertical vibrations, where each vibration lasts for a short period of 1.03 ms and exerts a maximum vertical acceleration of 503.55g on the chip (Figure 24). This test is in accordance with the industrial standard JESD22-B104C.

The working of the bonded chip was again checked by conducting the -1g/+1g flip test and the chip was still functional after going through the shock test. It can thus be concluded that the low temperature Al-Au contact at the MEMS-CMOS interface remained intact and successfully survived the shock test.

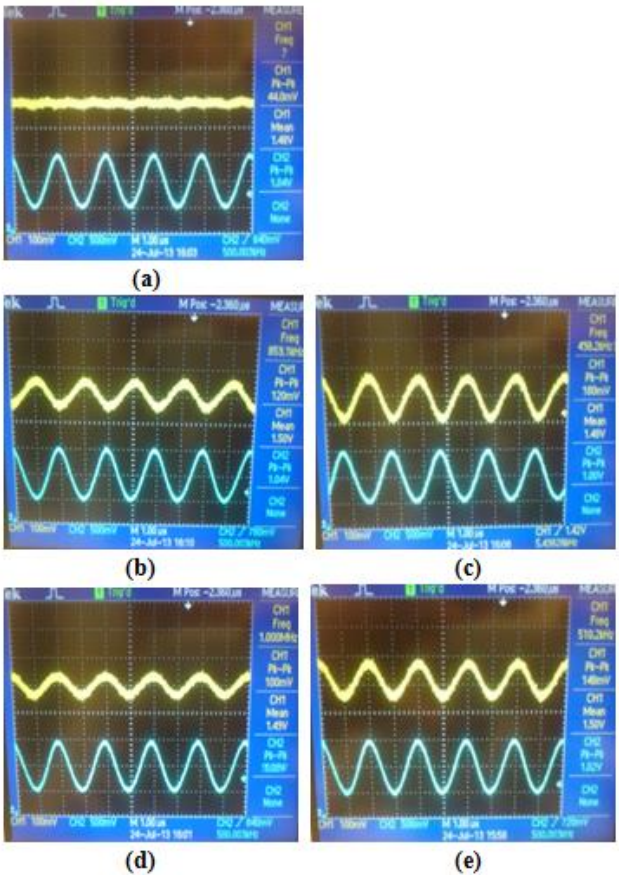



**Fig. 18** The gain stage output (yellow, upper trace) when the excitation carrier amplitude is 1Vpp (blue, lower trace) at 50kHz frequency and the bonded chip is tilted at: (a) 0g, (b) -0.707g, (c) -1g, (d) +0.707g and (e) +1g orientation. Acceleration at a tilt angle θ is given by g sin(θ).

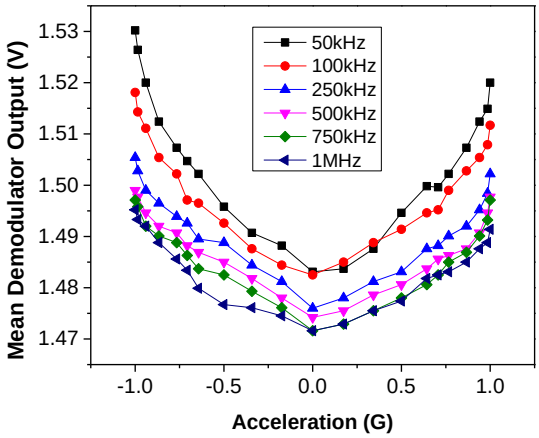



**Fig. 19** Variation in the mean demodulator output with g at various carrier frequencies for the bonded chip.

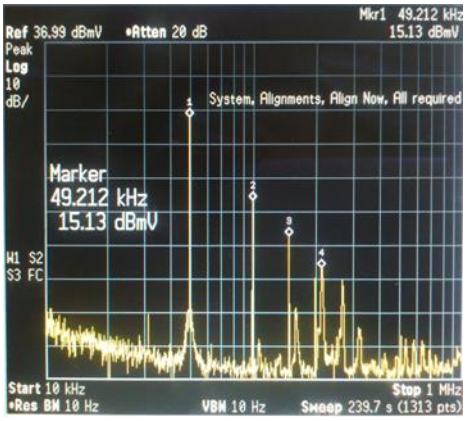



**Fig. 20** FFT spectrum showing fundamental peak at the carrier frequency and higher order harmonics at integer multiples of carrier frequency.

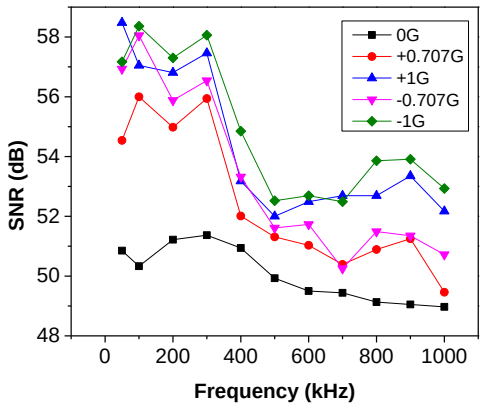



**Fig. 21** SNR as a function of carrier frequency at various g orientations, when carrier amplitude is 1Vpp.

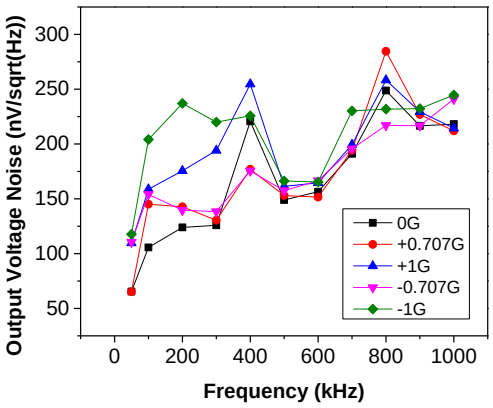



**Fig. 22** Output voltage noise as a function of carrier frequency at various g orientations, when carrier amplitude is 1Vpp.

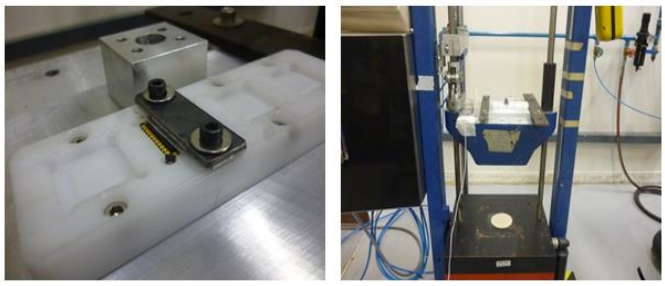


**Fig. 23** Setup for the 500g shock test. The chip is subjected to a maximum vertical acceleration of 503.55g for a short duration of 1.03 ms for a total number of 10 times.

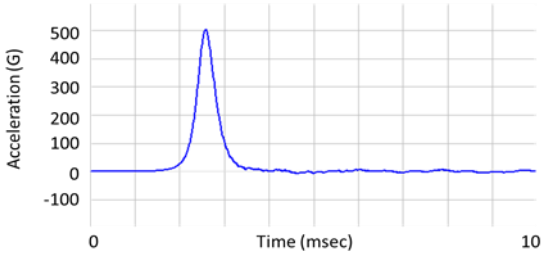



**Fig. 24** General control profile during the 500g and 1 ms mechanical shock test.

## Conclusion

Al-Au thermo-compression bonding have been tested and verified with reasonable results. Helium leak test demonstrates that the samples achieve an acceptable helium leak rate of average $2.7\times10^{-8}$ atm.cc/sec, which is lower than the reject limit of $5\times10^{-8}$ atm.cm3/sec defined by the MILSTD-883E standard. The hermetic test samples are also tested for gross leak and have passed the perfluorocarbon gross leak test. A CMOS readout circuit has been designed in a 0.35μm CMOS process employing chopper stabilization. It has a sensitivity of 5.1mV/g. Working sample of the integrated 3D CMOS-on-MEMS bonded chip using Al-Au thermo-compression has been shock tested and demonstrated that the Al-Au bonding is reliable mechanically. Since Al-Au thermo-compression bonding can provide electrical, mechanical and hermetic bonds in one step, this TSV-less 3D integration method will simplify the fabrication process and improves yield.

## References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