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A source follower based high-speed switched capacitor amplifier for pipelined ADCs

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In this paper, a low power high speed source follower based switched capacitor (SC) amplifier for pipelined analog-to-digital converters (ADCs) is proposed. By using the source follower as the core of the SC amplifier, the power consumption can be significantly reduced whilst obtaining the same linearity and bandwidth. Meanwhile, through replicating the input signal to the drain of input transistor, the channel-length modulation effect can be suppressed, achieving a high linearity (> 60dB). The functionality and linearity of the proposed SC amplifier are verified by simulation results.

Introduction: Pipeline ADCs are long proved candidates for high-speed high-resolution ADCs design. However, the power efficiency is limited when using conventional op-amp based residue amplifier [1] (Figs.1*a*), as the traditional op-amp, shown in Figs.1*b*, is power hungry when targeting high bandwidth and high gain. Recently, several novel techniques have been developed to supersede the power hungry residue amplifiers. In [2], an open-loop amplifier is adopted to replace the op-amp, leading to low power consumption. And in [3], a dynamic source follower amplifier based pipelined ADC is presented, which achieves low power. Unfortunately, it is limited to run at low speed (<100MS/s) and without employing bottom plate sampling, the linearity of the ADC is limited. In this work, a source follower based SC amplifier, of which the V_{gs} of following transistor is nearly constant with given bias current, achieves 250MS/s and linearity of 65.9dB with consuming 1.4mW.

Proposed SC Amplifier: The structure of proposed source follower based SC amplifier is depicted in Figs.1*c*. M1 and M2 are the pseudo differential input pairs, which work as source followers. M3 and M4 duplicate the input signal respectively to the drain of M1 and M2 to suppress channel-length modulation effect [4] and the bulk of M1 and M2 are connected to their source for eliminating bulk effect, both effects of which can degrade the linearity of SC amplifier. To make M1-M4 work in saturation region, the V_{in}+ and V_{in}- should be larger than $V_{th1,2}+V_{ov3,4}+V_{ov1,2}+V_{ov,bias}$. The proposed SC amplifier uses a two phase clocking scheme. During the sample phase Φ_1, both C_1 and C_2 are connected to input and the gate of M1 is connected to common mode voltage V_{CM}, which can be voltage supply V_{dd}. The output common mode voltage is V_{dd}-$V_{gs1,2}$. In the amplification phase Φ_2, the bottom plate of C_2 is connected to reference voltage V_{ref} ($V_{ref,cm}+V_{ref,diff}$) and the bottom plate of C_1 is connected to output. Hence, the transfer function of the SC amplifier can be derived according to charge conservation. The charge on the gate of M1 or M2 during the sample phase is:

$$Q_{\Phi 1} = (C_1 + C_2)\cdot(V_{CM} - V_{in,cm} - \frac{V_{in,diff}}{2}) . \quad (1)$$

For the amplification phase,

$$Q_{\Phi 2} = C_1 \cdot V_{gs1,2} + C_2 \cdot (V_{out} + V_{gs1,2} - V_{ref,cm} - V_{ref,diff}) + C_{gd3,4}\cdot(V_{out} + V_{gs1,2} - V_{dd}) . \quad (2)$$

Since the charge is conserved, setting the equations (1) and (2) equal gives the output common mode

$$V_{out,cm} = \frac{(C_1 + C_2)\cdot(V_{CM} - V_{in,cm} - V_{gs1,2}) + C_2 \cdot V_{ref,cm} - C_{gd3,4}\cdot(V_{gs1,2} - V_{dd})}{C_2 + C_{gd3,4}} . \quad (3)$$

It can be seen in (3) that there is a common mode gain in the SC amplifier. Therefore, common mode feedback block is needed for further implementation in pipelined ADC. The differential output is

$$V_{out,diff} = \frac{C_1 + C_2}{C_2 + C_{gd3,4}} \cdot V_{in,diff} + \frac{C_2}{C_2 + C_{gd3,4}} \cdot V_{ref,diff} . \quad (4)$$

In the case of $C_{gd3,4} << C_{1,2}$, the gain of proposed SC amplifier is

$$G = \frac{V_{out,diff}}{V_{in,diff}} \approx \frac{C_1 + C_2}{C_2} . \quad (5)$$

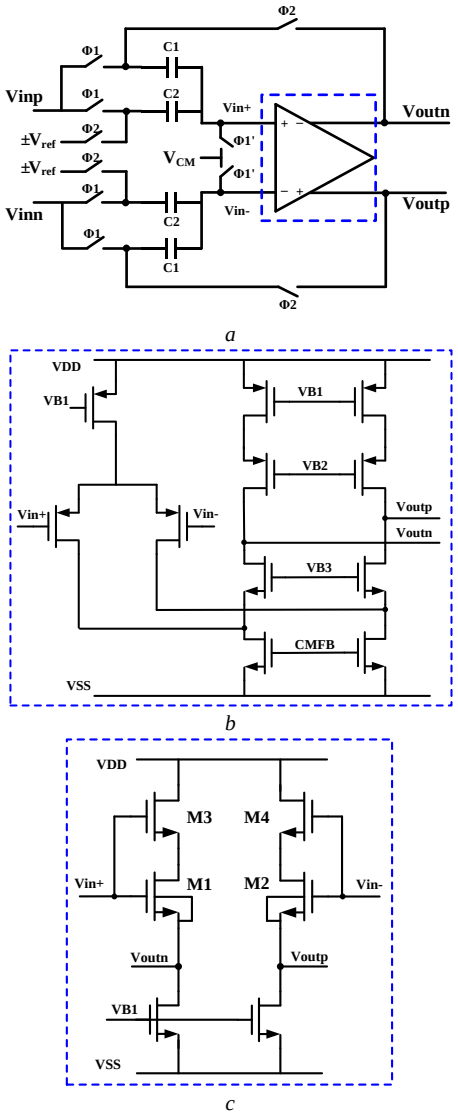

Fig. 1 *Residue amplifier in Pipelined ADC with two different amplifier core*

a Residue amplifier in Pipelined ADC
b Conventional op-amp core
c Proposed source follower based core

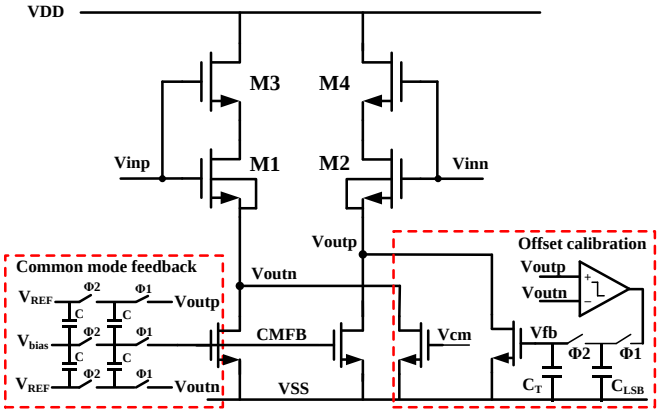

Fig. 2 *The proposed source follower core with offset calibration and common mode feedback*

Actually, a small variation of $V_{gs1,2}$ can be caused by different input voltage, which means $V_{gs1,2}$ is input signal dependent, leading to the nonlinearity of the SC amplifier. Assuming a variation of $\Delta V_{gs1,2}$ in $V_{gs1,2}$, the differential output is now

$$V_{out,diff} = \frac{C_1 + C_2}{C_2 + C_{gd3,4}} \cdot V_{in,diff} \pm \frac{C_2}{C_2 + C_{gd3,4}} \cdot (V_{ref+} - V_{ref-}) + \frac{C_1 + C_2 + C_{gd3,4}}{C_2 + C_{gd3,4}} \cdot \Delta V_{gs1,2} .$$

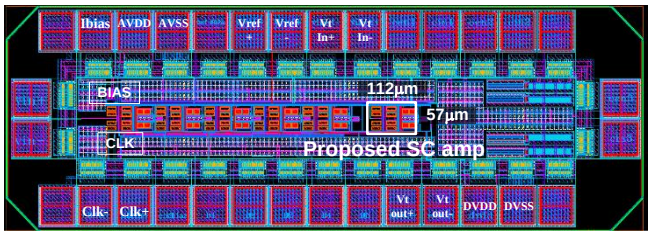

Fig. 3 *A pipeline ADC layout including the proposed SC amplifier*

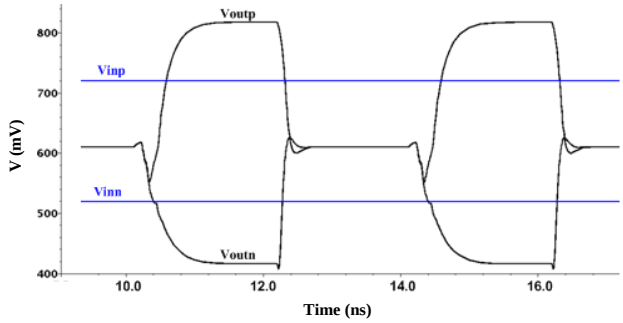

Fig. 4 *Simulated transient response of the proposed SC amplifier with constant differential input*

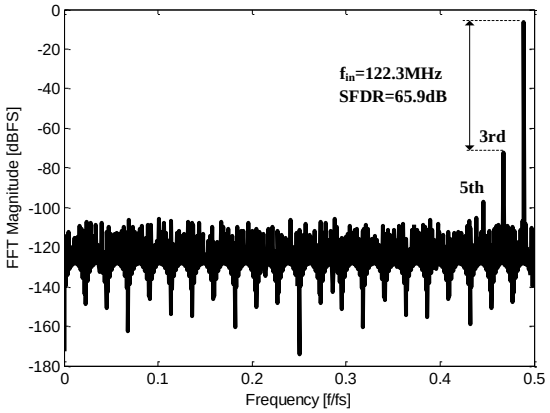

Fig. 5 *Simulated linearity of the source follower core with 122.3MHz $1V_{p-p}$ input and 250MHz sampling frequency*

(6)

The implemented source follower based SC amplifier is shown in Fig. 2, where offset calibration and common mode feedback circuits are included. The concept of switched capacitor common mode feedback technique [5] is adopted. For the offset calibration, the close loop calibration can be fulfilled during the sample phase in every clock cycle. The output of comparator indicates the polarity of offset and tunes accordingly the gate voltage V_{fb} through charge sharing between C_{LSB} and C_T ($C_T >> C_{LSB}$).

Table 1: Performance summary.

Technology	65nm Standard CMOS
Voltage Supply (V)	1.2
Input Common Mode (V)	0.6
Output Common Mode (V)	0.6
Output Swing ($V_{pp-diff}$)	1
Linearity(dB)	65.9
Sampling Capacitor (pF)	0.5
Load Capacitor (pF)	0.5
Power (mW)	1.44

Table 2: Performance in different corners and temperatures, with 122.3 MHz $1V_{p-p}$ input signal.

Corner	Slow		Typical	Fast	
Temp (℃)	-40	125	27	-40	125
SFDR (dB)	70.3	64.9	65.9	69.1	63.0

Table 3: Performance comparison with prior works.

Specification	Traditional [1]	Dynamic SF [2]	This work
Power (mW) (First stage)	~5	~0.2	1.4
Linearity(dB)	>60	~50	65.9
Speed (MS/s)	100	50	250
Technology	90nm CMOS	90nm CMOS	65nm CMOS

Simulation Results: The layout of proposed SC amplifier using standard 65 nm CMOS technology is shown in Fig. 3, which occupies an area of 112µm x 57µm. The simulated transient response of the proposed SC amplifier is given in Fig. 4. With a differential input voltage at 200 mV, the differential output is 400 mV and the settling time is less than 2 ns. The load capacitor is 0.5 pF and the sampling frequency is 250MHz. The total current consumption is 1.2mA. The output spectrum of a 122.3MHz $1V_{p-p}$ input signal is depicted in Fig.5, where the SFDR is 65.9dB, limited primarily by the third harmonic. The specification of proposed SC amplifier is listed in Table 1. The linearity at different process corner and temperature is shown in Table 2, verifying robustness of proposed circuit. And finally the performance comparison with prior works is given in Table 3.

Conclusion: In this paper, a low power high speed source follower based SC amplifier is presented, which achieves 250Ms/s and linearity of 65.9dB with only 1.4mW. The low power SC amplifier can also be used in other applications.

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