<table>
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<tbody>
<tr>
<td>Author(s)</td>
<td>Arulkumaran, Subramaniam; Ng, Geok Ing; Ranjan, Kumud; Kumar, Chandra Mohan Manoj; Foo, Siew Chuen; Ang, Kian Siong; Vicknesh, Sahmuganathan; Dolmanan, Surani Bin; Bhat, Thirumaleshwara; Tripathy, Sudhiranjan</td>
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</tr>
</tbody>
</table>
Record-low contact resistance for InAlN/AlN/GaN High Electron Mobility Transistors on Si with non-gold metal

Subramaniam Arulkumaran1*, Geok Ing Ng2**, Kumud Ranjan1, Chandra Mohan Manoj Kumar1, Siew Chuen Foo1, Kian Siong Ang1 and Sahmuganathan Vicknesh1, Surani Bin Dolmanan3, Thirumaleshwara Bhat3, Sudhiranjan Tripathy3

1Temasek Laboratories, Nanyang Technological University, Singapore 6375532
2School of Electrical & Electronic Engineering, Nanyang Technological University, Singapore 639798
3Institute of Materials Research and Engineering, A*STAR (Agency of Science, Technology and Research), Singapore 117602

E-mail: SArulkumaran@pmail.ntu.edu.sg; eging@ntu.edu.sg

We have demonstrated 0.17-µm gate-length In0.17Al0.83N/GaN high-electron-mobility transistors (HEMTs) on Si (111) substrates using a non-gold metal stack (Ta/Si/Ti/Al/Ni/Ta) with a record-low ohmic contact resistance ($R_c$) of 0.36 Ω-mm. This contact resistance is comparable to the conventional gold-based (Ti/Al/Ni/Au) ohmic contact resistance ($R_c = 0.33$ Ω-mm). A non-gold ohmic contact exhibited a smooth surface morphology with a root mean square surface roughness of ~2.1 nm (scan area of 5×5 µm²). The HEMTs exhibited a maximum drain current density of 1110 mA/mm, a maximum extrinsic transconductance of 353 mS/mm, a unity current gain cutoff frequency of 48 GHz, and a maximum oscillation frequency of 66 GHz. These devices exhibited a very small (<8%) drain current collapse for the quiescent biases ($V_{gs0} = -5$ V, $V_{ds0} = 10$ V) with a pulse width/period of 200 ns/1 ms. These results demonstrate the feasibility of using a non-gold metal stack as a low $R_c$ ohmic contact for the realization of high-frequency operating InAlN/AlN/GaN HEMTs on Si substrates without using recess etching and regrowth processes.
1. Introduction

InAlN/GaN high-electron-mobility transistors (HEMTs) have great advantages over conventional AlGaN/GaN HEMTs owing to their larger band gap discontinuity ($\Delta E_c \sim 0.68$ eV$^1$), which results in a 2–3-times higher two-dimensional electron gas (2DEG) density in the order of $\sim 2.73 \times 10^{13}$ cm$^{-2}$ and in current densities of more than 2 A/mm at room temperature and 3 A/mm at 77 K$^2$. Such devices emerged as a high-power HEMT technology$^3$. Moreover, AlGaN/GaN HEMTs also exhibit strain induced reliability issues owing to the large (~ 18%) lattice mismatch between the AlGaN barrier and the GaN buffer layer$^1$. A lattice-matched In$_x$Al$_{1-x}$N/GaN HEMT ($x \sim 0.17$) mitigates strain-induced reliability owing to the absence of piezoelectric polarization which helps to improve overall device characteristics. By inserting a thin layer of AlN between the InAlN barrier layer and the GaN active buffer layer, alloy disorder scattering is significantly reduced, which in turn enhances the transport properties of the channel$^4$. The optimized heterostructure with gate-length scaling and an efficient process technique can provide improved DC and RF performance characteristics. There are few reports on high $f_T$ in InAlN/AlN/GaN HEMTs on SiC$^{5,6}$ and sapphire$^{7,8}$ substrates. Recently, Yue et al.$^9$ have achieved a very high $f_T/f_{\text{max}}$ of 400/33 GHz with a 30-nm-gate-length InAlN/AlN/GaN HEMT on a SiC substrate using conventional Au-based ohmic contacts with regrown n$^+$-GaN. However, very few reports$^{10-13}$ on InAlN/AlN/GaN HEMTs fabricated on Si substrates are available. Furthermore, most frequently reported InAlN/AlN/GaN HEMTs were fabricated using conventional III–V Au-based ohmic metal stacks that were not compatible with the existing Si process line. Hence, non-gold ohmic contacts with low contact resistance ($R_c$) are essential for InAlN/AlN/GaN HEMTs to be manufacturable in the matured Si process line. Table I shows some of the best reported $R_c$ values for non-gold ohmic contacts for InAlN/AlN/GaN HEMTs$^{14-17}$. Few researchers have utilized non-gold ohmic metal stacks \{Ti/Al/Ni/W$^{14}$, Hf/Al/Ta$^{15}$, Ta/Al/Ta$^{16}$\} to demonstrate a low $R_c$ for InAlN/AlN/GaN HEMTs.
Alomari et al. realized first a very high $R_c$ of 1.6 Ω-mm on InAlN/AlN/GaN HEMTs on sapphire substrates by using a non-gold \{Ti/Al/Ni plus Ta/Cu/Ta\} ohmic metal\textsuperscript{[17]}. Malmros et al. have reported $R_c = 0.64$ Ω-mm obtained using a Ta/Al/Ta metal stack on InAlN/AlN/GaN HEMTs on SiC substrate by annealing at 550 ºC\textsuperscript{[16]}. Recently, Tripathy et al. have reported an $R_c$ of 0.56 Ω-mm in an InAlN/AlN/GaN HEMT structure on a 200-mm–diameter Si substrate obtained by annealing at 900 ºC for 60 s\textsuperscript{[14]}. More recently, we have proposed and demonstrated a non-gold ohmic metal scheme using Ta with a thin layer of Si for AlGaN/GaN HEMTs on Si substrates\textsuperscript{[18]}. In this work, we have achieved a record-low $R_c$ of 0.36 ±0.03 Ω-mm in InAlN/AlN/GaN HEMTs on Si substrates using a work-function-engineered “Ta/Si”–based non-gold metal stack. In addition, we report DC and microwave characteristics of 0.17-µm-gate InAlN/AlN/GaN HEMTs on Si substrates with low (~8%) drain current collapse.

2. Experimental methods

The GaN HEMT structure was grown by metal–organic chemical vapor deposition (MOCVD) with a 9-nm-thick In$_{0.17}$Al$_{0.83}$N barrier, an ~1-nm-thick AlN spacer layer, an ~1000-nm-thick i-GaN buffer layer and an ~100-nm-thick nucleation layer on a high-resistivity Si (111) substrate [see Fig. 1(a)]. The grown structure exhibited a room-temperature 2-DEG mobility of ~796 cm$^2$/V.s, an average sheet resistance of ~381 Ω/☐, and a sheet carrier density of $2.06 \times 10^{13}$ cm$^2$. After mesa isolation by dry etching using BCl$_3$/Cl$_2$ plasma, a Ta/Si/Ti/Al/Ni/Ta (5/5/20/120/40/30 nm) ohmic metal was deposited and annealed at 825 ºC for 30 s in a N$_2$ environment with a rapid thermal annealing (RTA) system. Figure 1 shows the optical microscope images of (b) non-gold ohmic and (c) conventional gold ohmic contacts on InAlN/AlN/GaN HEMTs. The non-gold ohmic metal stack exhibits a smooth surface morphology with good edge definition, which is similar to our previous work on AlGaN/GaN HEMTs on Si substrates\textsuperscript{[18]}. The non-gold ohmic contact exhibits a smooth
surface morphology with an RMS surface roughness of ~2.1 nm (AFM scan area = 5×5 μm²) which is better than that (20-160 nm) of conventional ohmic contacts (Ti/Al/Ni/Au) (20/120/40/50 nm) on AlGaN/GaN HEMTs. Other research groups have also observed similar RMS roughness ranges\(^{19-23}\).

A 0.17 μm Schottky T-gate foot print with a 0.5 μm gate-head was formed with a metal stack of Ni/Au (150/400 nm) using electron beam evaporation. Figure 1(d) shows the cross-sectional high resolution transmission electron microscopy (HR-TEM) image of the T-gate formed on InAlN/AlN/GaN HEMTs. Subsequently, a non-gold Ti/Al/Ta (50/800/30 nm) metal stack was also formed as an interconnect metal. Finally, the devices were passivated with 120-nm-thick PECVD-grown SiN at 300 ºC. The device dimensions used for this study are \(L_{sg}/L_g/L_{gd}/W_g = 0.8/0.17/1.7/(2×75) \mu m\). On-wafer DC and pulsed \(I–V\) characteristics of the HEMTs were measured using an Agilent B1500 semiconductor parameter analyzer and an Accent Diva D265, respectively. Microwave small-signal measurements were also carried out using an HP 8510c vector network analyzer (VNA). To study the interface properties of metal-semiconductor contacts, HR-TEM and energy-dispersive X-ray (EDX) were also carried out and analyzed.

3. Results and discussion

Figure 2(a) shows the current-voltage characteristics of non-gold (Ta/Si/Ti/Al/Ni/Ta) and gold ohmic contacts for InAlN/AlN/GaN HEMTs on Si substrates. Figures 2(b) and 2(c) show the total resistance versus transfer length model (TLM) gap (5 to 80 μm) characteristics of non-gold and gold ohmic contacts, measured across five locations {Centre (C), Top (T), Bottom (B), Left (L), Right (R)} of the 2-inch wafer [see inset of Fig. 2(a)]. The conventional gold ohmic contact the (Ti/Al/Ni/Au) on the InAlN/AlN/GaN HEMT structure exhibited an average \(R_c\) as low as 0.33 ±0.02 Ω-mm and an average specific contact resistivity (\(\rho_c\)) of 3.27x10\(^{-6}\) Ω-cm². The non-gold ohmic contacts exhibited an average \(R_c\) as low as 0.36 ± 0.03 Ω-mm with a \(\rho_c\) of 4.47x10\(^{-6}\) Ω-cm², which is
comparable to that of the gold-based ohmic contacts. Table II shows the best reported $R_c$ values of conventional gold ohmic contacts for InAlN/AlN/GaN HEMTs on Si and SiC substrates. Thus far, the lowest $R_c$ values of 0.15 $\Omega$-mm and 0.16 $\Omega$-mm were obtained using SiCl$_4$ recess etching and regrown n$^+$-GaN on InAlN/AlN/GaN HEMT structures, respectively, on SiC substrates.

We have also achieved low $R_c$ values in AlGaN/AlN/GaN HEMTs by an optimized ohmic-recess etching process. However, these techniques are more complex than our ohmic process reported in this work, which will facilitate the high-volume manufacturing process. Figure 3 shows the cross-sectional (a) HR-TEM image, (b) zoomed EDX area mapping, (c) EDX line scan and (d) zoomed EDX line scan of the annealed non-gold ohmic contact on the InAlN/AlN/GaN HEMT structure. From the results of qualitative EDX analysis, the observed low $R_c$ is possibly due to the formation of a mixture of Ta$_x$Si$_y$ and Ti$_x$Si$_y$ at the interface of metal-semiconductor contacts. Further investigation is required to determine the exact metal alloy at the interface. Recently, we have also realized a low $R_c$ by the intermixing of the Ti$_x$Si$_y$ alloy in the Ta layer on the AlGaN/GaN HEMT structure with a similar non-gold metal stack. The achieved $R_c$ is believed to be the lowest ever reported for non-gold ohmic contacts on InAlN/AlN/GaN HEMTs on Si substrates and is about 56% lower than that of Ta-based non-gold ohmic contacts ($R_c$=0.64 $\Omega$-mm) on InAlN/AlN/GaN HEMTs on SiC substrates. Figure 4(a) shows the two-terminal Schottky gate current-voltage characteristics of InAlN/AlN/GaN HEMTs. The reverse gate leakage current of the device measured at $V_G$ = -15 V was $1.47 \times 10^{-2}$ mA/mm, which is typical for the Ni/Au Schottky gate for InAlN/AlN/GaN HEMTs. The device exhibited a Schottky barrier height ($\phi_B$) of 0.81 eV with an ideality factor ($n$) of 1.38. Figure 4(b) shows the $C-V$ characteristics of the Ni/Au Schottky diodes, measured at 1 MHz. The threshold voltage ($V_{th}$) of the Schottky diodes from the $C-V$ curve is the -2.6 V, which is in agreement with the $V_{th}$ value obtained from the device transfer characteristics. The observed very small hysteresis in the $C-V$ characteristics is believed to be due to the existence of a negligible number of interface traps between Ni and InAlN layers.
Figure 5 shows the typical (a) $I_{DS}-V_{DS}$ and (b) transfer characteristics of 0.17-µm-gate InAlN/AlN/GaN HEMTs on Si substrates. The fabricated HEMTs exhibited a maximum drain current density ($I_{D\text{max}}$) of 1110 mA/mm and a maximum extrinsic transconductance ($g_{m\text{max}}$) of 353 mS/mm with good channel pinch-off. The achieved $I_{D\text{max}}$ is close to the reported 1170 mA/mm, however it is obtained with a small gate length of 50 nm with a small source-drain distance of 1.0 µm\textsuperscript{16}). Moreover, the devices suffer from the short channel effect with high output conductance beyond $V_D = 4$V. Figure 6(a) shows the small-signal microwave performance of InAlN/AlN/GaN HEMTs measured at $V_g = -2.2$V and $V_D = 6$V. The HEMT exhibited an $f_T$ of 48 GHz and an $f_{\text{max}}$ of 66 GHz without de-embedding. Figure 6(b) shows the pulsed $I_{DS}-V_{DS}$ characteristics (width/period=200ns/1ms) of InAlN/AlN/GaN HEMTs on Si substrates under gate-lag ($V_{gs0} = -5$ V, $V_{ds0} = 0$ V) and drain-lag ($V_{gs0} = -5$ V, $V_{ds0} = 10$ V) conditions. A very small (~8%) drain current ($I_D$) collapse was observed from the gate-lag and drain-lag measurements. The observed small $I_D$ collapse in the gate-lag measurement is due to the lattice-matched InAlN/AlN/GaN HEMT structure, thus the absence of piezoelectric polarization. The strain-free InAlN barrier layer has also been verified by Leach et al.\textsuperscript{30}). In addition, the surface-related current collapse is also suppressed by the optimized SiN passivation with (NH\textsubscript{4})\textsubscript{2}S\textsubscript{x} pretreatment\textsuperscript{31,32}).

4. Conclusions

We have demonstrated for the first time 0.17-µm-gate-length InAlN/AlN/GaN HEMTs on Si substrates with promising device performance characteristics using a non-gold metal stack. A Ta/Si-based ohmic contact exhibited the lowest $R_c$ of $0.36 \pm 0.03$ Ω-mm with a smooth surface morphology (RMS roughness~2.1 nm). The measured $R_c$ values of non-gold ohmic contacts are comparable to those of the gold-based ohmic contact on the same device structure. The HEMTs exhibited $I_{D\text{max}} = 1110$ mA/mm, $g_{m\text{max}} = 353$ mS/mm, $f_T = 48$ GHz, and $f_{\text{max}} = 66$ GHz, and $I_D$ collapse < 8%. These results demonstrate the feasibility of using a non-gold metal stack as a low $R_c$ ohmic contact.
contact to achieve good performance submicron-gate InAlN/AlN/GaN HEMTs on Si substrates for high-frequency applications.
Acknowledgments

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References


Solidi C 6, 999 (2009).


Table Captions

**Table I.** State-of-the-art contact resistances value of non-gold ohmic contacts for InAlN/AlN/GaN HEMTs on silicon, sapphire, and SiC substrates.

**Table II.** State-of-the-art contact resistances of gold-based ohmic contacts for InAlN/AlN/GaN HEMTs on SiC and silicon substrates.

Figure Captions

**Fig. 1.** (a) Schematic cross section of InAlN/AlN/GaN HEMT structure, optical microscope images (500X) of (b) non-gold ohmic contact and (c) conventional III–V gold ohmic contact on InAlN/AlN/GaN HEMT structure, and (d) cross-sectional HR-TEM image of T-gate on InAlN/AlN/GaN HEMTs.

**Fig. 2.** (a) Current-voltage characteristics of non-gold and gold ohmic contacts on InAlN/AlN/GaN HEMTs on Si. The inset is a schematic diagram of the 2-in. diameter wafer with different locations of the TLM patterns. Total resistance versus TLM gaps for (b) non-gold and (c) gold ohmic contacts on InAlN/AlN/GaN HEMTs.

**Fig. 3.** (a) Cross-sectional HR-TEM image, (b) zoomed EDX area mapping (c) EDX line scan and (d) zoomed line scan (25 to 60 nm) of alloyed Ta/Si/Ti/Al/Ni/Ta ohmic contacts with InAlN/AlN/GaN HEMTs.

**Fig. 4.** (a) Two-terminal gate-leakage current-voltage (b) C-V characteristics of InAlN/AlN/GaN HEMTs on Si.

**Fig. 5.** (a) $I_{DS}-V_{DS}$ and (b) transfer characteristics of InAlN/AlN/GaN HEMTs $(W_g/L_g/L_{gd}) = (2\times75)/0.17/1.7 \, \mu m$ on Si substrates with non-gold ohmic contacts.

**Fig. 6.** (a) Small-signal characteristics and (b) pulsed $I_{DS}-V_{DS}$ characteristics (pulse width/period=200ns/1ms) of InAlN/AlN/GaN HEMTs.
### Table I

<table>
<thead>
<tr>
<th>Affiliation</th>
<th>Substrate</th>
<th>Ohmic metal</th>
<th>Annealing temp. / time (°C /s)</th>
<th>$R_c$ (Ω-mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMRE [14]</td>
<td>Si</td>
<td>Ti/Al/Ni/W</td>
<td>900/60</td>
<td>0.56</td>
</tr>
<tr>
<td>NUS [15]</td>
<td>Si</td>
<td>Hf/Al/Ta</td>
<td>600/60</td>
<td>0.58</td>
</tr>
<tr>
<td>Chalmers [16]</td>
<td>SiC</td>
<td>Ta/Al/Ta</td>
<td>550/-</td>
<td>0.64</td>
</tr>
<tr>
<td>ULM [17]</td>
<td>Sapphire</td>
<td>Ti/Al/Ni &amp; Ta/Cu/Ta</td>
<td>900/-</td>
<td>1.60</td>
</tr>
<tr>
<td>This work</td>
<td>Si</td>
<td>Ta/Si/Ti/Al/Ni/Ta</td>
<td>825/30</td>
<td>0.36</td>
</tr>
</tbody>
</table>

### Table II

<table>
<thead>
<tr>
<th>Affiliation</th>
<th>Substrate</th>
<th>Ohmic metal</th>
<th>Treatments prior to metallization</th>
<th>Annealing Temp. / time (°C/ s)</th>
<th>$R_c$ (Ω-mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UND[9]</td>
<td>SiC</td>
<td>Ti/Au</td>
<td>Regrown n⁺-GaN by MBE</td>
<td>Non alloyed</td>
<td>0.16</td>
</tr>
<tr>
<td>NTU [10,13]</td>
<td>Si</td>
<td>Ti/Al/Ni/Au</td>
<td>-</td>
<td>825/30</td>
<td>0.33</td>
</tr>
<tr>
<td>ETH [11]</td>
<td>Si</td>
<td>Ti/Al/Au</td>
<td>-</td>
<td>800/30 and 850/30 (Two fold annealed)</td>
<td>0.36</td>
</tr>
<tr>
<td>NIT [12]</td>
<td>Si</td>
<td>Ti/Al/Ni/Au</td>
<td>-</td>
<td>800/30</td>
<td>0.60</td>
</tr>
<tr>
<td>ISSE [24]</td>
<td>SiC</td>
<td>Ti/Al/Ni/Au</td>
<td>SiCl₄ plasma etching (Ohmic recess)</td>
<td>600/-</td>
<td>0.70</td>
</tr>
<tr>
<td>ALCATEL [25]</td>
<td>SiC</td>
<td>Ti/Al/Ni/Au</td>
<td>-</td>
<td>900/30</td>
<td>0.15</td>
</tr>
<tr>
<td>UIUC [26]</td>
<td>SiC</td>
<td>Mo/Al/Mo/Au</td>
<td>SiCl₄ plasma etching (Ohmic-recess)</td>
<td>650/30</td>
<td>0.15</td>
</tr>
<tr>
<td>MIT [27]</td>
<td>SiC</td>
<td>Si/Ge/Ti/Al/Ni/Au</td>
<td>-</td>
<td>820/30</td>
<td>0.35</td>
</tr>
</tbody>
</table>
SiN\textsubscript{x} (120nm)

\begin{itemize}
  \item i-\text{In}_{0.17}\text{Al}_{0.82}\text{N} (9nm)
  \item i-\text{AlN} (1nm)
  \item i-\text{GaN} (1000nm)
  \item AlN (100nm)
  \item Si (111) Substrate
\end{itemize}

\textbf{Fig.1 (Color Online)}
Fig. 2 (Color Online)
Fig. 3 (Color Online)
Fig. 4 (Color Online)

- **(a)**
  - $I_g$ [mA/mm] vs. $V_{gs}$ [V]
  - $\Phi_b = 0.81$ eV
  - $n = 1.38$
  - $1.47 \times 10^{-2}$

- **(b)**
  - Capacitance [F] vs. Voltage [V]
  - Forward and Reverse curves
Fig. 5 (Color Online)
Fig. 6 (Color Online)