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A Thermal Resilient Integration of Many-core Microprocessors and Main Memory by 2.5D TSI I/Os

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Abstract—One memory-logic-integration design platform is developed in this paper with thermal reliability analysis provided for 2.5D through-silicon-interposer (TSI) and 3D through-silicon-via (TSV) based integrations. Temperature-dependent delay and power models have been developed at microarchitecture level for 2.5D and 3D integrations of many-core microprocessors and main memory, respectively. Experiments are performed by general-purpose benchmarks from SPEC CPU2006 and also cloud-oriented benchmarks from Phoenix with the following observations. The memory-logic integration by 3D RC-Interconnected TSV I/Os can result in thermal runaway failures due to strong electrical-thermal couplings. On the other hand, the one by 2.5D transmission-line-interconnected TSI I/Os has shown almost the same energy efficiency and better thermal resilience.

I. INTRODUCTION

Many-core microprocessors with integrated main memory have become the recent interest for the design of high-performance servers. The 2D integration has low bandwidth, long latency and hence poor I/O energy efficiency, since limited data are transferred with long time. On the other hand, the 3D integration [1] by vertical stacking is one promising solution for memory-logic integration by through-silicon-via (TSV), which can significantly reduce the communication latency, improve communication bandwidth and hence result in high I/O energy efficiency.

However, the vertical stacking by TSV results in a long heat dissipation path, which significantly degrades the thermal reliability [2]. From device perspective, due to the isolation material (liner) that surrounds the TSV where the heat is accumulated, it can introduce significant delay [3]. From system perspective, memory-logic integration with high-density DRAMs has significant leakage current, which can be coupled with temperature to form a positive-feedback loop resulting in thermal runaway failure [4].

Instead of stacking memory and logic at different layers with TSV I/Os, the recent introduction of through-silicon-interposer (TSI) [5] provides a 2.5D solution for memory-logic integration. In contrast to TSV which is short RC-interconnect for inter-layer communication, TSI is usually designed as transmission line (T-line) targeted for high-speed long-distance communication between main memory and cores. Compared to the RC-interconnect with repeaters, 2D single-ended T-line (STL) or differential T-line (DTL) [6] with current-mode-logic (CML) buffers [7] have demonstrated better latency, power and bandwidth performance but with large area overhead. However the TSI based T-line can be designed through and under the common substrate, so high performance yet low area overhead memory-logic integration can be achieved. What is more, as memory and logic components are spread on the common substrate that is close to heatsink, the thermal reliability of 2.5D integration by TSI I/Os can be better than 3D integration by TSV I/Os.

In this paper, we build up a memory-logic-integration design platform to evaluate thermal reliability of the integrated many-core microprocessors and main memory by 2.5D TSI-based I/Os and 3D TSV-based I/Os. With consideration of electrical-thermal coupling, detailed delay and power models of 2.5D and 3D I/Os are introduced into microarchitecture-level cycle-accurate simulators. With the use of general-purpose SPEC CPU2006 [8] and cloud-oriented Phoenix [9] benchmarks, the following results are observed. As for energy efficiency, the 2.5D integration shows almost the same efficiency as 3D integration when the temperature is high. Moreover, thermal runaway failure is prone to be observed in 3D integration by TSV I/Os with more than four layers.
formed, when signal voltage is applied across TSV. As such, the existence of liner material around TSV metal, depletion region is linearly dependent on temperature. As shown in Figure 1(c), due to channel is given by resistance $R$ corresponding delay model for one TSV I/O channel with capacitance $C_{TSI}$ may be given as

$$D_{TSI} = \frac{1}{Z_{STL}}$$

where

- $C_{STL}$ and $C_{DTL}$ are mutual inductance and capacitance of DTL.
- $d_0$ and $d_0$ are driver impedance and load capacitance.
- $R_0$ and $C_0$ are resistance and capacitance of TSV or TSI at room temperature $T_0$.
- $\alpha$ is the temperature dependent coefficient for resistance, $\beta_1$, $\beta_2$ are temperature dependent first and second order coefficients of capacitance.

All the coefficients can be characterized from measurement [11].

**B. Temperature-dependent Delay Model of TSV**

A TSV-based 3D I/O channel with buffers at both ends is shown in Figure 2(a). We use the inverter as the buffer for TSV. The corresponding delay model for one TSV I/O channel with capacitance $C_T$ modeled by (2) is shown in Figure 2(b). Based on the TSV resistance $R_T$ and capacitance $C_T$ in (1), the delay of one TSV I/O channel is given by

$$D_{3D-I/O} = R_T C_T = R_0(1 + \alpha(T - T_0)) C_T = R_0(1 - \alpha T_0) C_T + \beta_1 T + \beta_2 T^2$$

where $R_0$ and $C_0$ are resistance and capacitance of TSV or TSI at room temperature $T_0$.

$\alpha$ is the temperature dependent coefficient for resistance, $\beta_1$, $\beta_2$ are temperature dependent first and second order coefficients of capacitance.

The traditional 2D interconnect is modeled as RC-circuit with linear dependence to temperature. As shown in Figure 1(c), due to the existence of liner material around TSV metal, the temperature dependent TSV model can be given as

$$D_{TSV} = \frac{1}{R_T C_{TSV}}$$

where

- $C_{TSV}$ is the temperature dependent coefficient for resistance, $T$ is TSI at room temperature.

$R_T$ and $C_T$ are temperature dependent first and second order coefficients.

Similarly, the bandwidth for TSI with $N$ channels can be given by

$$BW_{TSI} = \frac{N}{2\pi D_{TSI}}$$

The delay of 2.5D TSI has much smaller dependence with temperature than 3D TSV, the impact of temperature on bandwidth and delay is small, which means that a more thermal resilient design can be achieved in 2.5D integration.
IV. 2.5D/3D POWER AND THERMAL MODEL

A. Power Models

As shown in Figure 1, the 2.5D and 3D integrations consist of cores, memory and I/O channel. The power model of each component needs to be studied for thermal analysis.

1) Core and DRAM Power Model: Core power $P_{\text{core\_total}}$ is the sum of dynamic power $P_{\text{core\_dyn}}$ and leakage power $P_{\text{core\_leak}}$.

$$P_{\text{core\_total}} = \eta \cdot C_{\text{core}} \cdot V_{DD} \cdot \Delta V \cdot f + V_{DD} \cdot I_{\text{leakage}}$$  \hspace{1cm} (7)

where

$$I_{\text{leakage}} = A_v \cdot \frac{W_d}{L_d} \cdot v_T \cdot (1 - e^{-\frac{v_{GS} - V_T}{v_T}}) \cdot e^{-\frac{v_{DS}}{v_T}}$$  \hspace{1cm} (8)

with $V_{DD}$ is the supply voltage with $\Delta V$ swing, $C_{\text{core}}$ is the core load capacitance, $\eta$ represents the activity factor and $f$ is the clock frequency, $L_d$ and $W_d$ are the effective device channel length and width, $A_v$ is technology-dependent constant, $v_T$ is the subthreshold swing coefficient and $v_{DS}$ is the thermal voltage.

The dynamic DRAM power with a data array of $N$ identical banks and each bank has $B$ I/O channels can be given as

$$P_{\text{DRAM\_dyn}} = n \cdot B \cdot \eta \cdot C_{\text{channel}} \cdot V_{DD} \cdot f$$  \hspace{1cm} (9)

with $C_{\text{channel}}$ is the channel capacitance.

Assuming that one DRAM memory bank with size of $M$ has leakage current similar to (8), the leakage DRAM power can be given as

$$P_{\text{DRAM\_leak}} = n \cdot M \cdot V_{DD} \cdot I_{\text{leakage}}$$  \hspace{1cm} (10)

It can be observed that the leakage current can vary significantly with temperature in an exponential fashion which may lead to two consequences. Firstly, the leakage power can dominate the total power. Secondly, it may form a positive feedback loop with temperature that can lead to thermal runaway failure.

2) I/O Power Model: The dynamic power of 3D I/O with $N$-channel TSVs and buffers can be given as

$$P_{\text{3d\_io}} = \eta \cdot N \cdot (C_T \cdot C_L) \cdot V_{DD}^2 \cdot f$$  \hspace{1cm} (11)

where $\eta$ represents the activity factor, $C_T$ is the temperature dependent capacitance given in (2), $C_L$ is the load capacitance of the buffer.

Based on (11), for a TSV I/O channel operating at a high temperature, the dynamic power will go up significantly due to the nonlinear temperature dependence of capacitance. The dynamic power of 2.5D I/O with $N$-channel TSIs and buffers can be calculated as [13]

$$P_{\text{2d\_io}} = \frac{\eta \cdot N \cdot V_{DD}^2 \cdot f}{(R_j + R_D)}$$  \hspace{1cm} (12)

where $s$ is the duration of signal pulse, $\eta$ is the activity factor, $Z_0$ is the characteristic impedance from (5), $R_D$ is the driver impedance of CML buffer.

By observing (5) and (12), it can be concluded that the power of TSI I/O channel is less dependent on temperature (with square-root dependence) than TSV I/O channel (with quadratic dependence).

B. Thermal Runaway Failure

The second thermal reliability concern is between power and temperature. Under large bandwidth, it is more liable to form a positive feedback loop resulting in thermal runaway failure. The thermal dynamics with heat-sink heat removal ability is [14]

$$C_{TR} \frac{dT}{dt} = P_{\text{thermal}} - \frac{C_{TR}}{R_T} \cdot T - T_h$$  \hspace{1cm} (13)

where $P_{\text{thermal}}$ is thermal power, $C_{TR}$ is thermal capacitance, $R_T$ is the thermal resistance path from $g$ chips to the heat-sink.

If the thermal source grows much faster than heat removal ability of heat-sink, temperature will increase exponentially. Thermal runaway temperature $T_{\text{threshold}}$ is temperature at which thermal runaway failure happens. To avoid thermal runaway failure, we can place heat-sink closer to processing cores. Since 2.5D integration has a much close heat-removal path to heat-sink, it shows better heat removal ability than 3D integration.

V. EXPERIMENTAL RESULTS

A. Experiment Setup

The system setup for microarchitecture evaluation platform is shown in Table I. The simulation is performed in gem5 [15] with multi-core system set up as 16-core x86 microprocessors. Benchmarks from SPEC CPU2006 [8] and Phoenix [9] are used. The performance results from gem5 are then sent to McPAT [16] to analyze cores scaled at 22nm. CACTI [17] is used to model DRAMs scaled at 32nm. The area estimations are obtained from simulation results.

In addition, the number of I/O channels for both 2.5D and 3D integrations is 64. The length of TSV I/Os is 50μm, which is the distance of adjacent layers. The length of TSI I/Os is 1.5mm, which is the distance between two ICs. Then the total area is about 288mm² for 2.5D integration and 64mm² for 3D integration. Moreover, a thermal simulator [18] is employed to provide temperature profiles for thermal runaway failure observations in both integrations.

**TABLE I: System setup for microarchitecture evaluation platform**

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<tr>
<th>Components</th>
<th>Description</th>
<th>Value</th>
<th>Area Estimation</th>
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<tr>
<td>Core</td>
<td>Frequency</td>
<td>1.0 GHz</td>
<td>2.469 mm²</td>
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<tr>
<td>DRAM</td>
<td>Cacheline size</td>
<td>32 KByte</td>
<td></td>
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<tr>
<td>TSV I/Os</td>
<td>Number of channels</td>
<td>64</td>
<td>32.025 mm²</td>
</tr>
<tr>
<td>TSI I/Os</td>
<td>Length of interconnect</td>
<td>0.5 μm</td>
<td>19 μm²</td>
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</table>
Fig. 5: Delay and power comparison under different temperature for TSV I/Os and TSI I/Os.

Fig. 6: Power breakdown of (a) 2.5D integration at 25°C; (b) 2.5D integration at 120°C; (c) 3D integration at 25°C; (d) 3D integration at 120°C.

Fig. 7: Total power and energy efficiency with different bandwidths: (a) at 25°C; (b) at 100°C.

We now present the power and energy efficiency relation with bandwidth in Figure 7. The bandwidth can be adjusted by varying the number of I/O channels. On average, 2.5D integration consumes 62% more power than 3D integration at 25°C. When the temperature rises to 100°C, it consumes 10% more power. If heat dissipation is not well designed, it will form a positive feedback loop between leakage power and temperature resulting thermal runaway failure. Note that the delay of the TSVs will be greatly affected when the temperature is high, thus decrease the bandwidth. Here the energy efficiency is defined as energy consumption per bit. It can be seen that energy efficiency will decrease as the number of channel increases. On average, 2.5D integration consumes 21% more energy per bit than 3D integration at 25°C. But when the temperature rises to 100°C, 2.5D integration achieves almost the same energy efficiency as 3D integration.

In the following, we will explore the thermal runaway issue in both integrations. The initial temperature is set at 25°C. The heat-sink size is 4.0cm × 4.0cm for 2.5D integration and 2.0cm × 2.0cm for 3D integration, both with heat-removal resistance of 4.6K/W. The system temperature trend is shown in Figure 8. When the temperature goes beyond the threshold temperature (100°C), thermal runaway failure happens. The temperature of 2.5D integration is maintained between 50°C and 70°C. For 3D integration, we vary the number of memory layers to see its heat dissipation performance. We can see that it remains stable below 4 layers. With 5 layers, the temperature rising trends can be observed after 6 millions execution cycles, which rises quickly beyond 100°C. Note that the number of memory layers will affect the system performance. As such, high performance 3D system is more liable to the risk of thermal runaway issue. In this case, 4 layers setting is the best from thermal perspective.

VI. Conclusions

Thermal resilient memory-logic-integration is studied in this paper by 2.5D TSI I/Os with comparison to 3D TSV I/Os. Detailed electrical-thermal coupled delay and thermal models are developed. The 3D TSV RC-interconnect based I/Os show better delay and bandwidth performance but are more sensitive to the temperature when considering poor thermal-conductive isolation layer and leakage-intensive memory. The 2.5D TSI T-line based I/Os have much less electrical-thermal coupling to delay and power, hence are more resilient to temperature-dependent thermal runaway failure. Moreover, the low-area-overhead 2.5D TSI based integration can achieve similar bandwidth and power performance as 3D TSV based integration.

REFERENCES